DESKTOP VIDEO DATA HANDBOOK

1993

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INTEGRATED CIRCUITS

Desktop Video Data Handbook

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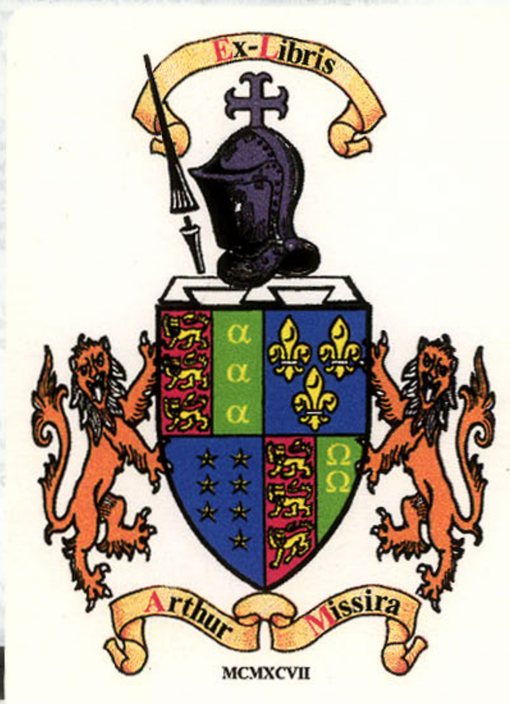
Desktop Video Products



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DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Our appreciation is extended to the following persons for their assistance in the publication of the Desktop Video Handbook:

To: all the Philips factory representatives who supplied updated data sheets at short notice.

also to:

Herb Kniess	Application notes
Leo Warmuth	Application notes
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Digital video now, an introduction

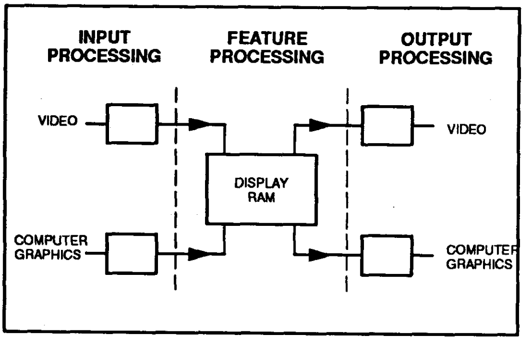
In the old days, if you wanted to see video, you turned to your television set. Nowadays, video is popping out all over--on PCs, workstations, teleconferencing gear, and a spate of medical and test equipment.

WHY?

Because humans live in a real-time, natural color world that machines are just catching up with. Video enhances the effectiveness of education, training, medical diagnosis, and just about any attempt to communicate.

HOW?

People are using digital video processing ICs from Philips Semiconductors-Signetics to facilitate the fusion of video and graphics. Look:



Unfortunately, this simple diagram hides a host of difficulties, including differences in scanning schemes, screen refresh rates, resolution, and color encoding. Fortunately, Philips has been into televisions since Felix was a kitten, and knows how to deliver video that looks good, even under adverse conditions.

WHAT DO YOU NEED?

The system that you select to decode and digitize your video signal must meet the following requirements:
- Support for Standards
- Orthogonal Sampling Structure
- Ease of Implementation

SUPPORT FOR STANDARDS

PAL, NTSC, SECAM

Philips digital video can detect which of the three international broadcast standards it is receiving and automatically switch to decode it!

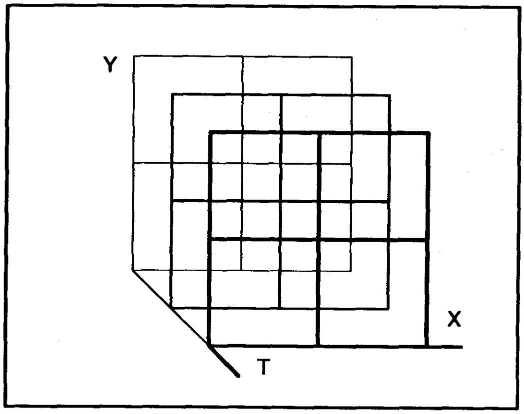
S-VHS

Industrial applications frequently demand the increased performance of Super-VHS. Philips digital video can process S-VHS with the addition of a second analog-to-digital converter to handle the chrominance channel.

CCIR601

CCIR601 is an internationally established standard for digitizing PAL, NTSC, and SECAM. This standard is frequently called D1 in the U.S.

We offer a chip set that is 100% compatible with this standard, as well as other chip sets that address different market requirements.



ORTHOGONAL SAMPLING STRUCTURE

Processing in the horizontal (X), vertical (Y), and time (T) dimensions requires that picture elements are in identical positions in each frame. Philips' unique **line-locked-clock** implementation satisfies this requirement.

Examples of video processing include:
- Filtering in the X-direction: bandpass filter.
- Filtering in the Y-direction: simple comb filter.
- Filtering in the T-direction: noise reduction.

In the Philips digital video system, the sample clock is synchronized with the input's sync signal. An internal discrete time oscillator is used to demodulate the chroma.

This concept combines quartz stability with adaptive handling of video line frequency, and delivers picture elements in each field in identical positions. After all, nobody wants pixels that deviate.

It guarantees robust recovery of the video signal, without jitter, tearing or loss of color, even under the following adverse conditions:
- Time-base errors from
  - VHS or 8mm tape playback
  - Videotape shuttle
  - Videodisc freezeframe
- Poor signal-to-noise ratio from
  - Low signal strength

Digital video now, an introduction

EASE OF IMPLEMENTATION

The Philips digital video system is simple to use:
- No adjustments.
- All 5-volt operation.
- Small form-factor–all parts available in surface mount
- Architecture is partitioned to simplify the addition of features.
- Digital circuitry is constant, reproducible, and not subject to manufacturing variations.
- It is not influenced by variations in supply voltage or aging.
- There are no tolerances and therefore no need for circuit adjustments.
- Digital control is readily implemented via I²C*, without the need for D/As or other interfaces.
- Digital filters are implemented on-chip, and offer linear phase response.
- A single crystal supports different broadcast standards.

THE BUILDING BLOCKS:

INPUT PROCESSING

Analog to Digital Converter (A/D)

We offer a broad range of high performance A/Ds incorporating Philips' unique folding and interpolation architecture (see glossary). Two of these are specially configured for the digital video chip set: the TDA8708 for composite video (CVBS) inputs, and the TDA8709 for chroma inputs in S-VHS applications.

With the TDA8708, one can select one of three composite video signals to input to the system. This IC includes clamping, automatic gain control, and drive for an external low-pass filter. The signal is then fed to an internal eight-bit analog to digital converter, and finally output to the Digital MultiStandard Decoder.

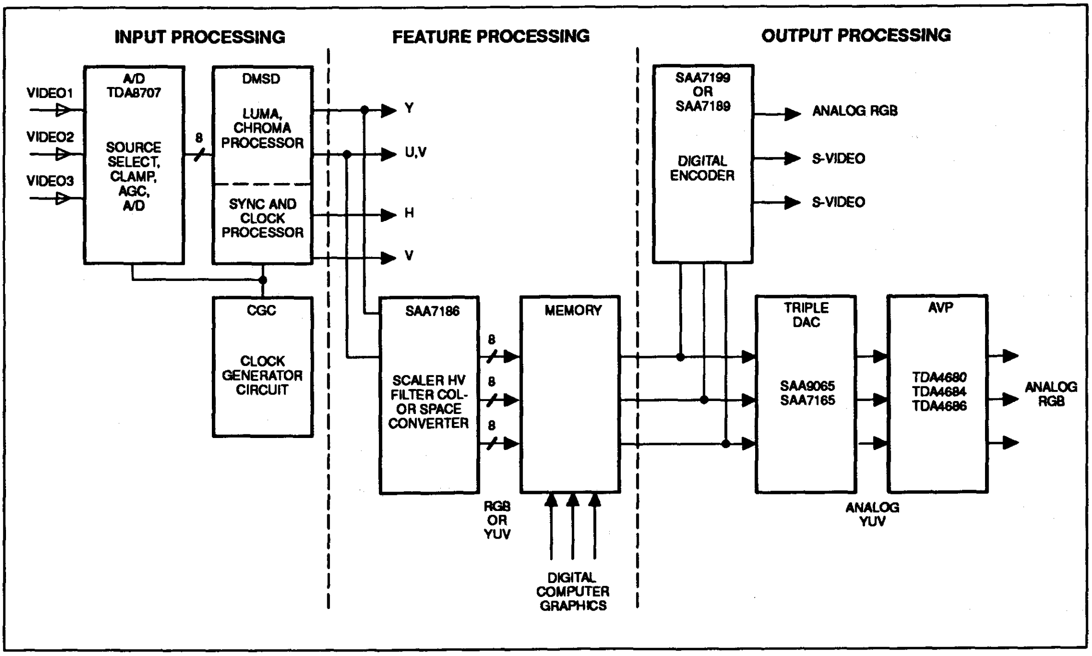
Digital MultiStandard Decoder (DMSD)

The DMSD accepts digitized composite video, performs horizontal and vertical synchronization processing, and outputs Luminance (Y) and Chrominance (U,V) signals. Via I²C (see glossary), one can control color hue and luminance frequency response for optimum performance.

Philips offers four DMSDs:
- SAA9051 for consumer applications:
  7-bits; Y:U:V 4:1:1; 13.5 MHz, 720 pixels/line
- SAA7151 for industrial applications:
  8-bits; Y:U:V 4:2:2; 13.5 MHz, 720 pixels/line
- SAA7191 for computer graphics:
  8-bits; Y:U:V 4:2:2; NTSC 12.27 MHz, 640 pixels/line
  PAL/SECAM 14.75 MHz 768 pixels/line
- SAA7194(6) for computer graphics:
  8-bits; Y:U:V 4:2:2; NTSC 12.27 MHz, 640 pixels/line
  PAL/SECAM 14.75 MHz 768 pixels/line

Clock Generator Circuit (CGC)

This IC works together with the DMSD to lock to the incoming signal's sync and generate the necessary system clocks. Philips offers three CGCs, one for each DMSD.



Digital video now, an introduction

FEATURE PROCESSING

Philips digital video architecture allows the data to be manipulated and freely shifted in time between input and output. Examples of processing which could be implemented here include manipulating the size of the picture, filtering, noise reduction, or data compression.

Digital Color Space Conversion (DCSC)

The SAA7192 digital color space converter connects directly to either the SAA7151 or SAA7191 DMSD. It accepts the Y:U:V data, interpolates samples, digitally converts Y:U:V to R:G:B, and performs inverse gamma correction via an on-chip look-up table. It outputs R:G:B 8:8:8, which can then be manipulated as computer graphics, or directly converted into analog red, green, and blue through a D/A, such as the TDA8702 or SAA7169.

Digital Video Scaler (DVS)

The SAA7186 digital video scaler connects directly to all Philips 8-bit decoders (SAA7151 B,SAA7191 B, and SAA7194/6) DMSD. It accepts the YUV data, interpolates samples, scales the video downward to any desired size, filters the scaled video in both the horizontal and vertical domains and performs digital color space conversion of the YUV data into several formats of YUV and RGB video. It also contains an output buffer with handshaking for ease of interface and an anti-gamma ROM (bypassable).

Digital Decoder and Scaler (DESC)

The SAA7194/6 integrates the functionality of the SAA7191 B digital decoder, SAA7197 clock generator (SAA7196 only) and the SAA7186 scaler IC's. Input processing, and feature processing are integrated into one device.

Digital Encoder (DENC)

The SAA7199B (DENC) is a digital video to analog CVBS or S-Video encoders. This device is multistandard. The 7199B accepts digital RGB, YUV, 8-bit Indexed and digitized composite video as inputs. It also features a digital genlock input to aid in synchronizing the encoding system to other reference sources. The SAA7199 will simultaneously output CVBS (composite) and S-Video into 75 ohm loads.

Video Enhancement and D/A processor (VEDA and VEDA2)

The SAA9065 (VEDA) and SAA7165 (VEDA2) accept YUV data input, upsamples and interpolates and converts the data to analog YUV signals. Both 7-bit 4:1:1 and 8-bit 4:2:2 data formats are possible. Both devices can perform aperture correction and the SAA7165 will perform color transient improvement. Both devices will run at 30 MHz so that non-interlaced video can be supported.

Analog Video Processor (AVP)

The TDA4680,4685 and 4686 include an analog matrix which will covert analog YUV to analog RGB. These devices also accept synchronous external analog RGB signals and switch between these sources at a pixel rate thus allowing overlay capabilities. I^2C control of brightness, contrast and saturation is possible. All three devices are pin compatible, the TDA4686 has higher throughput bandwidth.

GLOSSARY

I^2C Bus

The Inter-Integrated Circuit (I^2C) Bus is a two line, multi-master bus developed by Philips to provide cost-effective control of analog and digital functions among ICs.

I^2C can simplify the manufacturing process by enabling complete calibration and test under computer control. Philips offers a large family of I^2C-capable integrated circuits, including microcontrollers, microprocessors, and audio, video, and telephony ICs.

Folding, Interpolating A/Ds

This term describes the unique technology used in Philips' family of high speed analog to digital converters.

Designers are usually forced to choose between the high performance and high power consumption of bipolar flash A/Ds or the low power consumption and low performance of CMOS A/Ds. By folding comparator inputs and interpolating the outputs, Philips is able to realize an A/D with one quarter the circuitry of a conventional flash converter. That means high performance A/Ds with power consumption as low as 250 mW. In addition to video, these parts are enabling new test and medical imaging applications.

Application configurations

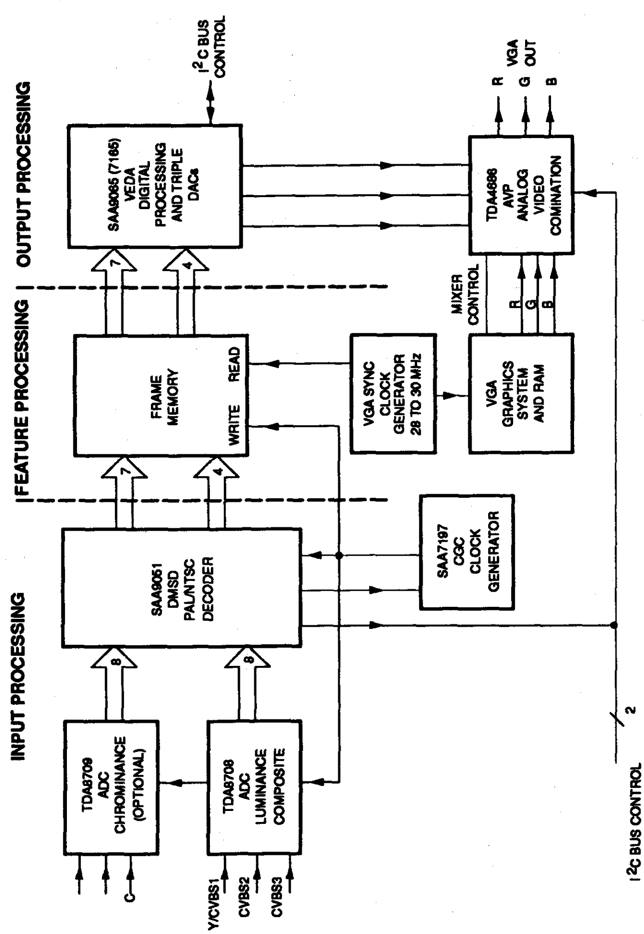


Figure 1. 7-Bit Low Cost Video Frame Grabber with VGA Out

Application configurations

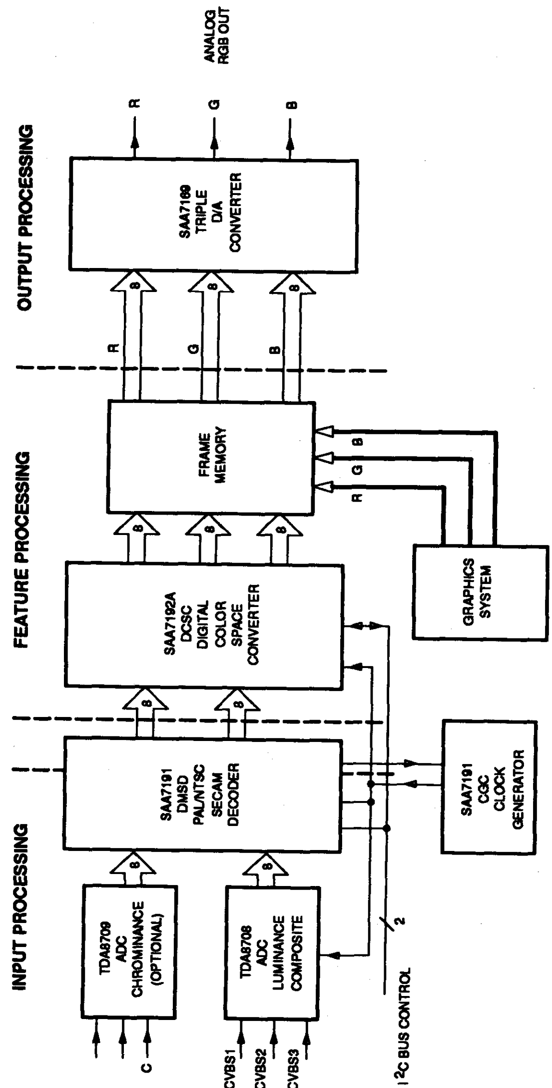


Figure 2. 8-Bit RGB Frame Buffer with Analog RGB Output

Application configurations

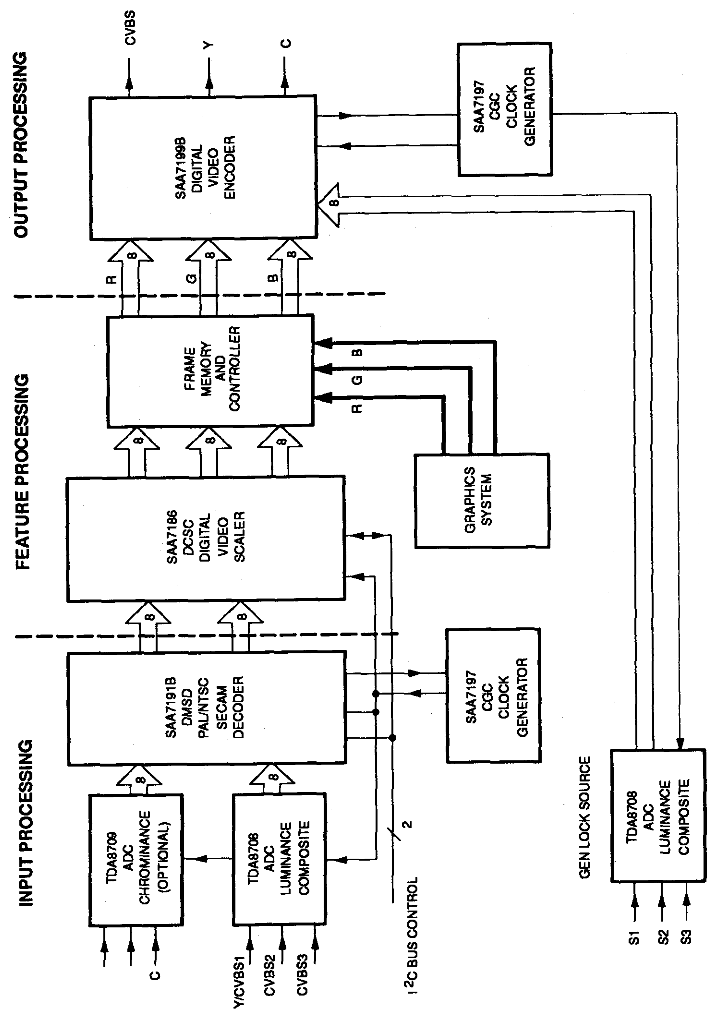


Figure 3. 8-Bit Video Window Graphics with Encoder Gen-Locked to an External Source

Application configurations

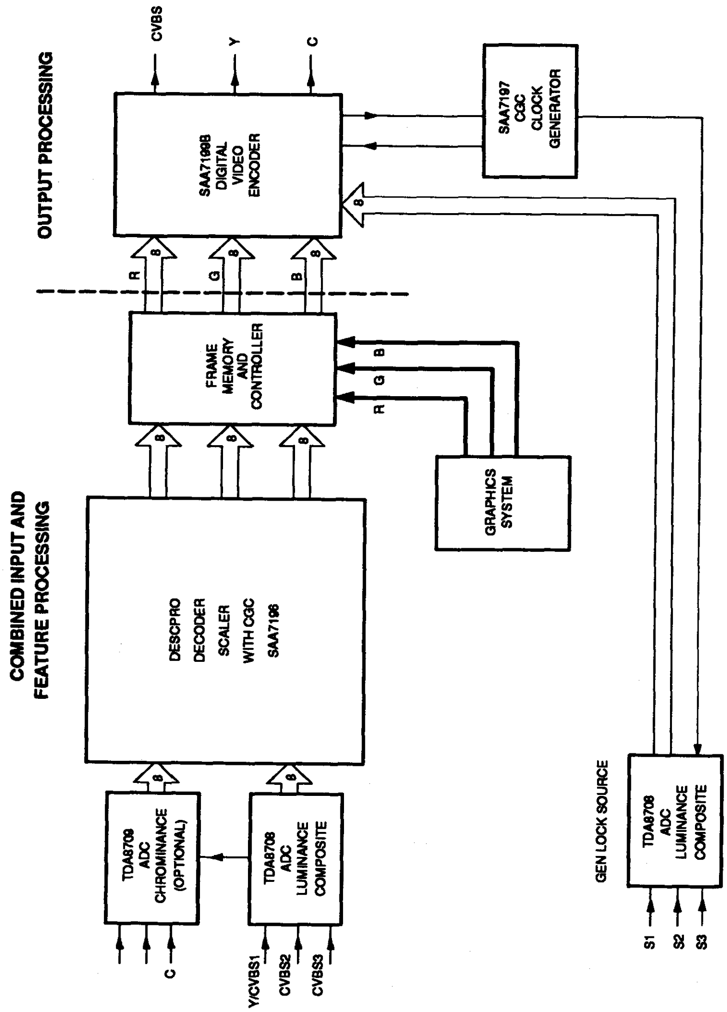


Figure 4. 8-Bit Video Window Graphics with Encoder Gen-Locked to an External Source Using SAA7196 Desco

Application configurations

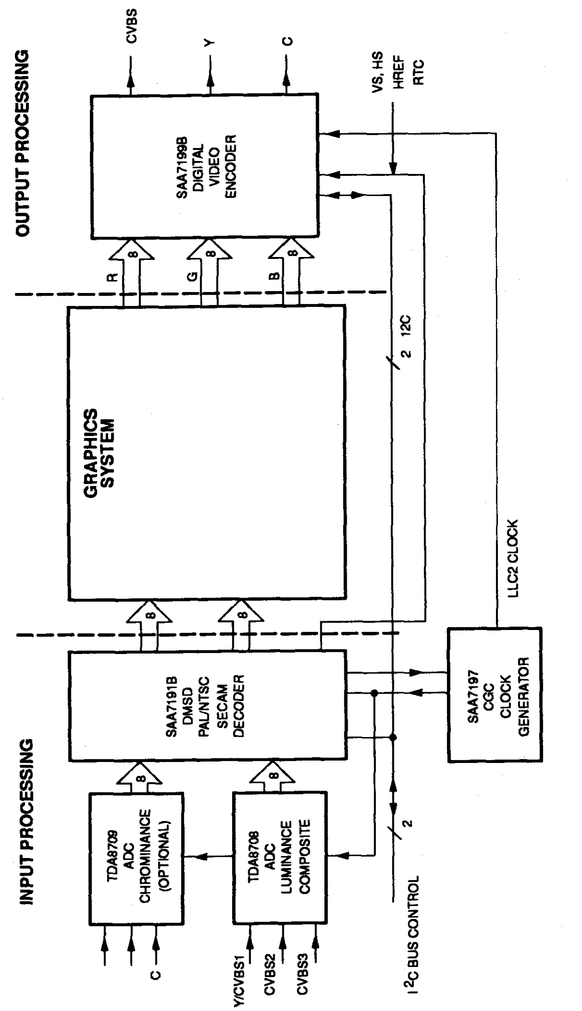


Figure 5. RTC Genlock Mode (Uses Single CGC)

Pro electron type designation code for integrated circuits

Basic type number

This type designation applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick- film and hybrid integrated circuits.

A basic type number consists of three letters followed by a serial number.

FIRST AND SECOND LETTER

Digital family circuits

The first two letters identify the family (see note 1).

Solitary circuits

The first letter divides the solitary circuits into:

S : solitary digital circuits
T : analog circuits
U : mixed analog/digital circuits

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits (see note 2).

Microprocessors

The first two letters identify microprocessors and correlated circuits as follows:

MA : microcomputer
central processing unit
MB : slice processor (see note 3)
MD : correlated memories
ME : other correlated circuits (interface, clock, peripheral controller, etc.)

Charge-transfer devices and switched capacitors.

The first two letters identify the following:

NH : hybrid circuits
NL : logic circuits
NM : memories
NS : analog signal processing, using switched capacitors
NT : analog signal processing, using change-transfer device
NX : imaging devices
NY : other correlated circuits

THIRD LETTER

The third letter indicates the operating ambient temperature range. The letters A to G give information about the temperature:

A : temperature range not specified below (see note 4)
B : 0 to + 70 °C
C : –55 to +125 °C
D : –25 to + 70 °C
E : –25 to + 85 °C
F : –40 to + 85 °C
G : –55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example : the range 0 to +75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

Version letter(s)

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack (2 leads)
G : for flat pack (4 leads)
H : for quadrature flat pack (OFP)
L : for chip on tape (foil)
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Pro electron type designation code for integrated circuits

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : cylindrical
D : dual-in-line (DIL)
E : power DIL (with external heatsink)
F : flat (leads on 2 sides)
G : flat (leads on 4 sides)
H : quadrature flat pack (QFP)
K : diamond (TO-3 family)
M : multiple-in-line (except dual-, triple-, quadruple-in-line)
Q : quadruple-in-line (QIL)
R : power QIL (with external heatsink)
S : single-in-line
T : triple-in-line
W : lead chip-carrier (LCC)
X : leadless chip-carrier (LLCC)
Y : pin grid array (PGA)

SECOND LETTER: Material

C : metal-ceramic
G : glass-ceramic (cerdip)
M : metal
P : plastic

To avoid confusion when the serial number ends with a letter, a hyphen is used preceding the suffix.

Examples (see note 5)

PCF1105WP	: Digital IC, PC family, operational temperature range −40 to +85 °C, serial number 1105, plastic leaded chip-carrier.
GMB74LS00A-DC	: Digital IC, GM family, operational temperature range 0 to +70 °C, company number 74LSS00A, ceramic DIL package.
TDA1000P	: Analog circuit, no standard temperature range, serial number 1000, plastic DIL package.
SAC2000	: Solitary digital circuit, operational temperature range −55 to +125 °C.

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).

2. The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added (e.g. SH for Bubble-memories).

3. By 'slice processor' is meant: a functional slice of microprocessor.

4. In the case of two same types with two different temperature ranges not specified below, one type should use the letter 'A' as the third letter and the other, the letter 'X'.

5. Some companies have been using version letters and/or two letter-suffix, which differ from the Pro Electron definitions. In case of confusion Pro Electron may be contacted.

Handling MOS devices

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

Video glossary

DEFINITION OF TERMS

AC-COUPLED – A means by which the constant, or DC component, of a signal is removed, usually by passing the signal through a capacitor.

AM – Amplitude Modulation (AM) is a modulation process by which the amplitude of the carrier signal is scaled in proportion to the modulation signal (which is the signal which carries the content). AM modulation is used for the video portion of the transmitted TV signal for both NTSC and PAL standards.

Anti-Top Flutter Pulse – Disables the phase detector during equalization and framing times.

APL – Average Picture Level. The mean or average signal level during the active video period. It is expressed as a percentage of the difference between blanking and peak white (O and 100 IRE).

AV – Audio Video

Back Porch – That section of the video waveform between the end of horizontal sync and the beginning of active video. The color burst signal is inserted during this period.

Bandwidth – The frequency range over which an input signal of uniform amplitude will be passed with uniform output (within a specified limit).

Baseband Video – Same as Composite Video (CVS or CVBS)

Black Burst – Black Burst (Color Black) is a composite video signal containing sync information, color reference (burst) and setup information (in the case of NTSC). Black Burst is often used as the studio reference to facilitate synchronization of all the devices in the system.

Black Level – The signal level which represents black picture intensity. For NTSC, this level is 7.5 IRE (also called Setup) and for PAL this level is 0 IRE.

Black Level Noise – Very similar to a white spot noise spike except it is in the opposite or black level direction.

Blanking Level – The video level immediately preceding or following horizontal sync exclusive of the active video region. The video level for blanking is defined as 0 IRE. In the case of PAL, blanking level and black level are the same.

Breezeway – That portion of the Back Porch between the end of horizontal sync and the beginning of the color burst.

Color Difference Signals – The chrominance information of a video signal, expressed as the combination of two orthogonal axis signals, B-Y (also called U or Cb) and R-Y (also called V or Cr). These signals contain no luminance (Y) information.

Composite Video – Composite video (CVS/CVBS) signal carries video picture information for color, brightness and synchronizing signals for both horizontal and vertical scans. Sometimes referred to as "Baseband Video".

CTV – Color Television

CVBS or CVS – Same as composite video.

Data Slicing – The process of extracting digital data from an incoming, non-TTL signal.

DC Coupled – An electrical connection passing both the DC component as well as the AC component of a signal.

DC Restoration – The process of setting the DC level of a video signal to a defined level. DC restoration is generally applied during the back porch region of the video signal by means of a clamp pulse applied to the restoration circuit at that point of the signal.

Demodulation – The process by which the original signal content is recovered from the modulated carrier. In color television, demodulation may additionally refer to the recovery of the color difference signals from the modulated chroma subcarrier.

Equalization Pulses – The pulses existing before and after the vertical pulse during the vertical interval. These are half horizontal in length and are inserted to effect the half-line offset in vertical sync required for interlace.

Field – For interlaced video the total picture is divided into two fields, one even and one odd each containing one half of the total vertical information. Each field takes one sixtieth of a second (one fiftieth for PAL) to complete. Two fields make a complete frame of video.

FM – Frequency modulation is the method by which the modulation signal which contains the information is used to vary the frequency of the carrier. For NTSC and PAL video, FM modulation is used to transmit the sound portion of the program.

Frame – One frame (two fields) of video contains the full vertical interlaced information content of the picture. For NTSC this consists of 525 lines and for PAL a frame is consisted of 625 lines.

Front Porch – The section of the video signal that lies between the end of active video and the beginning or leading edge of horizontal sync.

Full Field Teletext – In this mode, Teletext information is transmitted over, virtually, all available TV lines.

Gamma – Cathode ray tubes (CRTs) do not have a linear relationship between brightness and the input voltage applied. To compensate for this non-linearity, a pre distortion or gamma correction is applied, generally at the camera source. A value of gamma equal to 2.2 is typical, but can vary for different CRT phosphors.

Genlock – Two composite video signals can by phase locked to each other by synchronizing both the composite sync and color burst of the two signals. This process is called genlock.

Ghost Rows – These are the rows that are specified by the "row address field" of the "page header" but do not get displayed. These are rows 24 to 31. Sometimes referred to as "Extension Packets", these rows carry miscellaneous control information. (Page extension for Telesoftware, linked pages, higher display level, etc.)

Harmonic Distortion – A distortion added to a signal which consists of multiples or harmonics of that signal which were not present in the original. System non-linearity can contribute to this distortion.

Horizontal Blanking – The sum of the front porch, horizontal sync and back porch periods, i.e. the entire period from the end of active video to the beginning of active video on a line.

Horizontal Sync – A negative active pulse of 287mv amplitude (300mv for PAL) inserted in the composite video signal. This pulse is extracted by the monitor (or receiving system) and used to horizontally synchronize or define the left hand side of the image.

Hue – Tint or color such as red, pink, yellow, etc.

Hum – An undesirable superimposition of 60Hz (50Hz in Europe) power energy into the signal content.

Intercarrier Sound – The means by which sound is separated from the modulated television signal by the use of a sound carrier to beat against the video carrier. This produces a 4.5MHz signal which contains the audio portion of the television signal.

Interlace – A method to give a higher apparent number of lines on the television CRT screen. One television frame is written on the CRT with television lines of the "even field" placed in between those of the "odd field".

Video glossary

IQ Signals – Similar to the color difference signals (R-Y), (B-Y) but using different vector axis for encoding or decoding. Used by some USA TV and IC manufacturers for color decoding.

IRE – 1/140 of a volt which is the peak to peak amplitude of a video signal from the bottom of sync to the top of peak white. Sync and burst amplitude is defined as 40 IRE units, while active video is 100 IRE Max. The unit was originally defined by the Institute of Radio Engineers, hence the name.

Linear Distortion – Distortions which are independent of amplitude.

Luminance – The brightness or black and white content of a picture. No hue or saturation components exist. Luminance is also referred to by the letter Y and is defined as a sum of scaled red, green and blue primaries by the formula: Y=.30R+.59G+.11 B.

Modulation – The process whereby a signal containing information is used to vary some characteristic of a carrier. In the case of AM the carrier amplitude is varied, in the case of FM the carrier frequency is varied and in the case of chroma modulation, the phase of the carrier (called subcarrier in this case) is modulated.

NABTS – North American Broadcasting Teletext *Specifications.* ***Note that this is not a standard.***

This document specifies both the acquisition protocol and the display format. The display format is NAPLPS.

NAPLPS – North American Presentation Level Protocol Syntax. Again, this is not a display standard. It applies to both Teletext and Videotex services.

Non-Linear Distortion – These are distortions which are amplitude dependent. Differential gain and phase measurements are used to measure these distortions.

NTSC – National Television Standards Committee (USA).

Page Header – This is equivalent to Row 0. Carry Control information about this page.

PAL – Phase Alternate Line. A television standard used in Europe and other countries which alternates the relationship of the color axes on a line by line basis so that color modulation errors can be canceled out.

Peak White – Maximum amplitude signal corresponding to the maximum brightness of the video screen.

Peritel – An audio/video connector standard for European TV receivers. Serves the same purpose as AV connector on some of the newer American TV sets.

Quadrature AM – Refers to the process by which two different modulation signals each modulate carriers of the same frequency but which are 90 degrees out of phase. The summed signals can be added together for transmission and can be recovered at the receiver end if they are demodulated 90 degrees apart. This is the process used to modulate chrominance information onto the color subcarrier of a video signal.

Quadrature Distortion – Distortion which results if the sidebands of a vestigial sideband transmission are uneven or asymmetrical. If synchronous decoding is used instead of envelope detection, this distortion can be minimized.

RF Video – System used on standard Television transmissions via an antenna or cable system. Baseband video is amplitude modulated on an RF carrier.

RGB – Three separate signals of Red, Green and Blue used to produce a color image.

R-Y, G-Y, B-Y – Red, Green or Blue signals without the luminance (-Y).

Sandcastle Pulse – Multilevel pulse generated by the horizontal processor and the vertical deflection circuit. This pulse contains gating pulse and blanking signal information for use by the color decoder and the video control circuits.

Saturation – A characteristic describing color amplitude or intensity. A color of a given hue may consist of low or high saturation value which relates to the vividness of the color.

SECAM – Sequential Color and Memory system. TV color system used primarily in France and the USSR.

Setup – A video level which, for NTSC, defines black level and which is 7.5 IRE above blanking. Pal does not have setup.

SRM – Service Reference Model of NAPLPS. It is a skeleton NAPLPS, specifying a low level type display in order to allow for easy implementation (256h × 200v pixels).

Subcarrier – The carrier used to convey chroma information within the composite video signal. The R-Y and B-Y color difference signals are modulated onto the subcarrier by a process of quadrature AM modulation. The frequency of the subcarrier signal is related to the odd half-line multiples of the horizontal frequency in such a manner as to allow the chrominance frequency spectrum to co-exist or interleave within the luminance spectrum.

Synchronous Detection – A process by which demodulation is performed by multiplying the signal by another signal generated by a oscillator which is locked to the original carrier. This is the method preferred over envelope detection.

Teletext – One way broadcast of digital information.

Termination – Unless proper source and termination impedance's are presented to a transmission line, such as a co-ax cable, undesirable reflections and ringing can occur. Video transmission cable typically has a characteristic impedance of 75 ohms and should be terminated by same.

Unmodulated – Refers to the pure carrier frequency with no AM, FM, or Phase modulation imposed upon it. Also referred to as CW or continuous wave.

Vectorscope – An oscilloscope specifically designed to demodulate and display chroma as an x-y display of the decoded color with respect to the R-Y and B-Y (or I and Q) axis. Hue is displayed as the angle around the display, and saturation as the amount of displacement from the center.

Vertical Blanking Interval (VBI) – The time it takes the beam to fly back to the top of the screen in order to retrace the opposite field (odd or even). VBI is in the order of 20 TV (25 for PAL) lines. Teletext information is transmitted over 4 of these lines (lines 14-17).

Videotex – A two-way interactive system through which the user can communicate to a large, organized and secure, database through a telephone line using the TV as the display medium.

Waveform Monitor – An oscilloscope designed to measure the specific timings of a video signal.

World System Teletext (WST) – World System Teletext is based on the British teletext standard in which a one-to-one correspondence exists between transmitted characters,page memory, word addresses and the display screen character locations. Over 98% of the world's teletext decoders are WST compatible.

Y Signal – Luminance. Determines the brightness of each spot (pixel) on CRT screen either color or B/W systems, but not the color.

Alphanumeric index of products

Section 2
Application Notes and Materials

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High-performance 8-bit video data converters

Wherever there's a need to display a picture on a video screen, there's an attendant demand to enhance the image. This requires the analog video signals to be converted into digital information before the enhancement techniques can be applied. Unfortunately, although integrated 8-bit full-parallel flash ADCs are available for converting high-frequency video signals, the complex circuitry they contain to achieve the required high level of performance makes them too expensive and power consuming and, paradoxically, even restricts their performance for many applications.

We have overcome this problem by developing our innovative TDA87xx range of 20 MSPS to 50 MSPS, or even 100 MSPS 8-bit data converters and fabricating them in a standard high-volume bipolar process (SUBILO-N). This advanced process offers high speed, high packing density and excellent element matching, all of which are crucial factors for integrating high-performance data converters.

INNOVATIVE TECHNIQUE REDUCES COST AND POWER CONSUMPTION

The secret of the success of our TDA87xx data converters lies in an innovative folding and interpolating technique which reduces the number of on-chip components to such an extent that cost is reduced by up to 90%, and power consumption cut by up to 70%. A unique added benefit is that the impressive reduction of chip area we have achieved allows us to offer TDA87xx data converters not only in DIL packages but also in SO packages for surface mounting.

PROFESSIONAL PERFORMANCE AT A CONSUMER PRICE

Despite the remarkable reductions of power consumption and price we have achieved for our TDA87xx range, there is no sacrifice of performance. For example, our 75 MSPS 8-bit flash ADC type TDA8714 consumes as little as 325 mW, has a minimum differential linearity error of only 1/2 LSB, and a signal-to-noise ratio of 70 dB resulting in a resolution of 7.6 effective bits with an input frequency of 4.43 MHz (75 MHz clock). This compares well with the 6 effective-bit resolution offered by expensive bipolar professional ADCs and far outstrips the 3 or 4 effective-bit resolution obtainable with MOS ADCs for consumer video applications.

The outstanding video frequency performance of our TDA87xx converters, combined with their low cost and power dissipation, makes them ideal for reducing costs without degrading performance in professional and military applications and, for the first time, brings affordable high-performance data conversion to a host of consumer video applications.

High-performance 8-bit video data converters

A TO D CONVERSION TECHNIQUES

Full-parallel conversion is complex and power-hungry

Most currently available high-performance 8-bit ADCs use the full-parallel implementation shown in simplified form in Fig.1. In this configuration, 255 comparators simultaneously compare the level of the applied analog input signal with 255 different reference levels derived from a resistor ladder. On the occurrence of each sampling clock pulse, 255 latches store the output states of the 255 comparators and a 255 to 8-line encoder converts the latch outputs into an 8-bit code. Obviously, this full-parallel system is inefficient because much of the information stored in the latches is redundant. For example, since each sample of a full-scale input voltage ramp falls within the transition range of only one of the comparators, only one of the latches has to change its output state for each sample. Moreover, the 255 latches at the analog to digital interface cause kick-back noise which disturbs the sensitive analog circuitry. The complex circuitry and immense number of signal interconnections occupy a very large area of silicon, restrict operating speed and dissipate considerable power. Also, the analog signal sampling process and attendant aliasing effects impose stringent demands on the distortion and noise behaviour of the analog circuitry

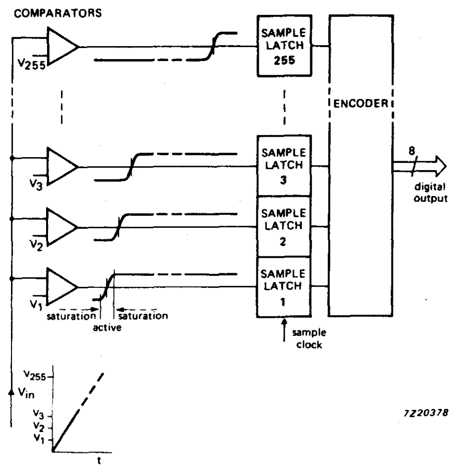

Fig.1 8-bit full-parallel ADC. At the sample clock, an array of 255 latches decides whether the output from each of 255 comparators is 1 or 0. The usage of the latches is inefficient - each has only to make one decision over the entire full-scale input range

Folding and interpolating reduces on-chip components and power consumption

An elegant method of reducing the complexity of the full-parallel ADC circuitry, is to reduce the number of latches and simplify the encoding logic by combining the outputs from several of the comparators and feeding the resultant signal to a single latch.

This "folding" technique is practical as long as the comparators which have their outputs combined are sufficiently far apart on the reference resistor ladder to ensure that any input sample falls within the transition range of only one of them.

The next logical step is to reduce the number of comparators and combining circuits (folding amplifiers), thereby also simplifying the precision reference resistor ladder. This is done by eliminating groups of intermediate comparators fed by consecutive taps on the reference resistor ladder and using a resistor ladder at the remaining comparator outputs to interpolate the missing signals.

Reducing the number of latches by folding the analog input signal

Figure 2 shows one of the sixteen identical sections of a "folding" 8-bit ADC with waveforms for sampling a full-scale input voltage ramp. Here, the outputs from every 16th comparator along the reference resistor ladder are alternately "folded" up and down by sixteen 16-input analog gating circuits (folding amplifiers), the output from each of which is sampled by a single latch. The number of latches required for a complete 8-bit ADC is thus reduced from 255 to 16, and the 255 to 8-line encoder is simplified to a 16 to 8-line circuit. Because the signal distribution problems

High-performance 8-bit video data converters

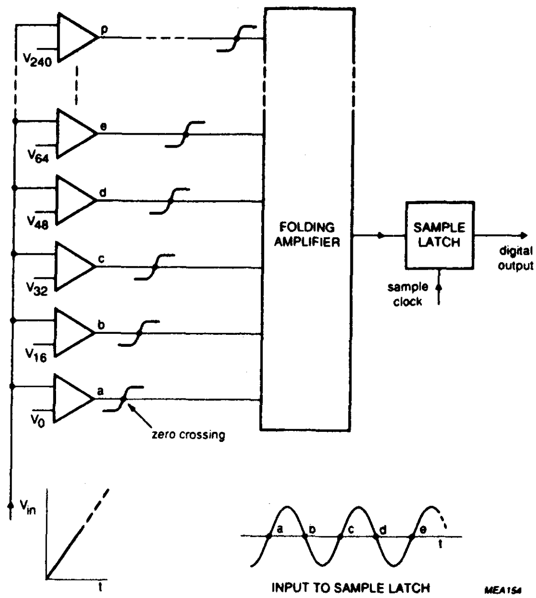

Fig.2 One of 16 identical sections of an 8-bit folding ADC. Folding the outputs of 16 comparators to one latch reduces the number of latches needed from 255 to 16

and chip area for this ADC configuration are also considerably reduced, its overall performance actually improves. Furthermore, since it has only 16 connections between the analog and digital circuitry instead of 255, kick-back noise is much reduced.

Because the output code generated by the 16 latches after folding (fine conversion) is repeated eight times during a full-scale input voltage ramp, a simple, easy to implement 3-bit coarse converter is needed to determine which of the eight output code cycles is the current one. It is also necessary to equalize the delays introduced by the coarse and fine conversion to ensure that the accuracy of the final data stream is equal to that of the fine converter.

Reducing the number of comparators by interpolating their outputs

The folding technique was used to reduce the number of latches required for an 8-bit ADC and simplify the encoding logic, thereby reducing chip area, power consumption and signal distribution paths without compromising performance. We will now show how an interpolation technique is used to further this aim by reducing the number of comparators and consequently the number of taps on the precision reference resistor ladder and the number of folding amplifiers. This interpolation technique exploits the fact that a comparator output signal doesn't change state instantly when the input exceeds the reference level, but follows the input signal linearly over the first part of the transition range.

Figure 3 shows outputs V_0 and V_4 from two of the comparators of the 8-bit folding ADC which are separated by three taps on the reference resistor ladder. It is clear that, since the transition ranges of these two comparators overlap considerably, the three intermediate outputs (V_1 V_2 and $V_{3)}$ can be derived by interpolation using a simple 3-tap resistor ladder connected between outputs V_0 and V_4 as shown in Fig.4. The distortion introduced by the interpolation is unimportant because only the zero crossings are of interest for setting the sampling latch.

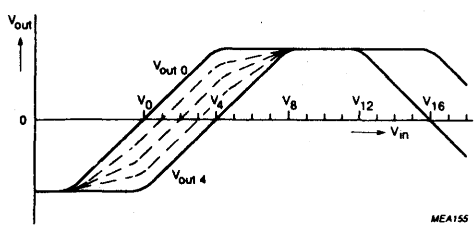

Fig.3 Interpolated zero crossings for three out of four comparator outputs

High-performance 8-bit video data converters

By using this interpolation technique, three out of every four comparators are eliminated, thereby reducing the number required for an 8-bit folding and interpolating ADC from 255 to 64. The interpolation technique also reduces the number of taps required on the precision reference resistor ladder from 255 to 64 and reduces the number of folding amplifiers required from 16 to 4.

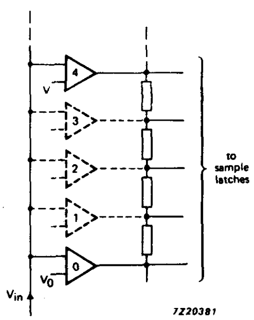

Fig.4 Interpolation of three out of every four comparator outputs with a resistor ladder reduces the number of comparators needed for an 8-bit ADC from 255 to 64

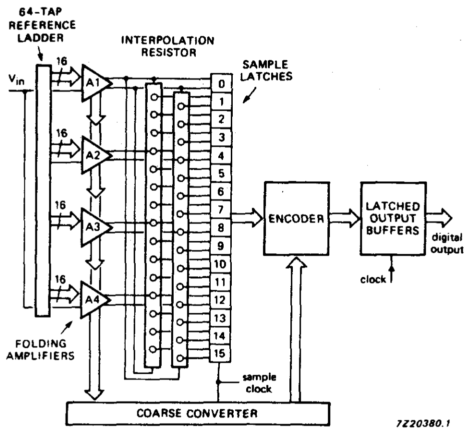

Fig.5 Block diagram of a complete folding and interpolating ADC. Although, in practice, interpolation takes place after folding of the comparator output signals instead of before as explained for clarity in the main text, the result is the same. The folding amplifier blocks each contain 16 comparators and a folding amplifier

The complete 8-bit folding and interpolating ADC

Figure 5 is a simplified block diagram of a complete 8-bit folding and interpolating ADC. In this diagram, each of the folding amplifier blocks contains 16 comparators and a folding amplifier. Also, although the interpolation is performed by resistor ladders at the outputs of the folding amplifiers, the principle remains the same as that described for interpolating at the comparator outputs.

Number of internal components for 8-bit full-parallel ADCs compared with those required for folding and interpolating ADCs

	conventional full-parallel ADC	folding and interpolating ADC
reference resistor taps	255	64
comparators	255	64
interpolation resistor taps	0	24
latches	255	16
encoder stages	255	16
simple 3-bit coarse converter	0	1
clock driver fan-out	255	24
output buffers	8	8

High-performance 8-bit video data converters

APPLICATIONS FOR VIDEO ADCs

The high performance combined with the low cost and power consumption of our TDA87xx range of video data converters make them suitable for applications ranging from costly professional equipment requiring the highest performance, to consumer equipment where cost is the major factor.

To quote just a few examples, transportable medical equipment, such as ultrasonic scanners, demands high performance combined with low power consumption. High performance is also essential for converters in sensitive high-frequency test and measuring equipment such as oscilloscopes and spectrum analyzers. The rapidly expanding market for desk-top video is another application area. In the consumer world of home entertainment systems, TV set manufacturers and broadcast authorities are meeting the demand for more TV channels and enhancement of picture quality by using digital signal processing techniques. For example, low-cost converters are needed for decoding MAC-encoded multi-channel TV and sound information from broadcast satellites, and for use in the new TV sets with memory-based features that are appearing on the market.

High-performance 8-bit video data converters

HOW WE MEASURE THE PERFORMANCE OF OUR ADCs

For an ADC specification to be useful to an equipment manufacturer, it must fully characterize the dynamic performance of the IC. Figures relating to integral and differential linearity at low frequencies are of little use as figures of merit because they have to be laboriously converted into more useful figures for many applications. Output signal-to-noise ratio (SNR), provided it is related to input frequency, is a much better and more versatile figure of merit for an ADC because the "noise" includes both the quantization error and the harmonic distortion. Moreover, a simple formula can be used to convert SNR into "effective bits". However, the SNR of an ADC is not easy to measure, and additional specific data relating to Total Harmonic Distortion (THD) is often required as well. This is why we have developed a special Measurement Bench for accurate determination of the static and dynamic performance of our present and future ADCs.

ADC measurement bench

Our ADC measurement bench is arranged as shown in Fig.6. It is for use in a laboratory to determine the static and dynamic characteristics of present and future ADCs with up to 12 digital outputs and conversion rates up to 100 MSPS. The following characteristics can be measured:

- signal-to-noise ratio (SNR)
- total harmonic distortion (THD)
- differential non-linearity (DNL)
- integral non-linearity (INL)
- data timing.

A PC is used to control the measurement bench and to acquire the sampled input signal to test the ADC. The acquired signal is converted into a data file that is used by a test program, developed with scientific Forth-language software called ASYST, to create histograms, graphs and a Fast Fourier Transformation (FFT) which facilitate analysis of the ADC output data to determine its operating characteristics.

Analog input signal

For accurate and complete determination of ADC characteristics, it's necessary to test all of the possible quantization levels. It's also necessary to meet the requirements of the Nyquist sampling theorem that states that it's only possible to fully define an analog waveform digitally if the sampling interval is not more than half the bandwidth of the analog signal.

Although it's possible to use an analog input signal with a triangular or sawtooth (ramp) waveform (theoretically infinite bandwidth), we use a full-scale sinusoidal signal because it has only one frequency component and is comparatively easy to synthesize at high frequencies.

Sampling method

At the start of a sinewave period, the slope of the signal is maximum and equal to $A2\pi f_{in}$ v/s, where A is the peak amplitude. The amplitude to be defined by 1 LSB of the ADC is therefore $2A/2^N$ volts, where N is the number of data outputs from the ADC. To acquire every quantization level by real-time sampling, 2^N samples must be taken during the period of one half cycle (one peak-to-peak sweep) of the input signal which is t_{in}/π. The time available to

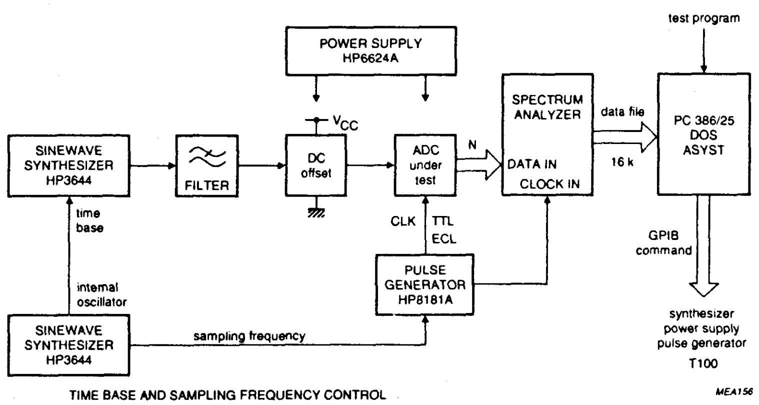

Fig.6 Block diagram of the measurement bench

High-performance 8-bit video data converters

describe 1 LSB is therefore $t_{in}/2^N\pi$, leading to a required conversion rate of $2^N\pi f_{in}$. For an 8-bit ADC with an input frequency of 5 MHz, the conversion rate would therefore have to be 4 GSPS, which is far above the maximum conversion rate specified for any of our ADCs.

Instead of using real-time sampling, our measurement bench therefore uses the multi-beat frequency method of sampling illustrated in Fig.7.

Multi-beat frequency sampling uses the principle of "aliasing" to convert the high frequency input sinewave into a lower frequency sinewave from which it is easier to acquire all the quantization levels for analysis.

Instead of acquiring all the samples during the period of half an input cycle by sampling at $f_s = 2^N\pi f_{in}$, the required number of samples (N_0) are now acquired over several cycles of the input signal and used to reconstruct a sinewave which is a lower frequency aliased version of the input signal

The ADC under test samples the sinewave input at a rate offset by a small amount from an integer multiple of the input frequency. The small frequency offset is chosen so that the ADC output only changes by one LSB at the point of maximum slope of each consecutive cycle of the input sinewave. Since an LSB period at the point of maximum slope of a sinewave is $t_{in}/2^N\pi$, the minimum number of samples that must be acquired to fully test all the quantization levels is $N_0 > 2^N\pi$, in which N_0 must be rounded to an integer. For an 8-bit converter, N_0 must be at least 805.

Under these conditions, the minimum sampling period (time to acquire all samples during one input cycle) is $t_s min = t_{in}/N_0$ which gives a maximum sampling frequency of $f_s max = f_{in}N_0$. This maximum frequency is too high to be practical and must be reduced to $f_s = f_s max/K_0$ ($t_s = t_s min K_0$)

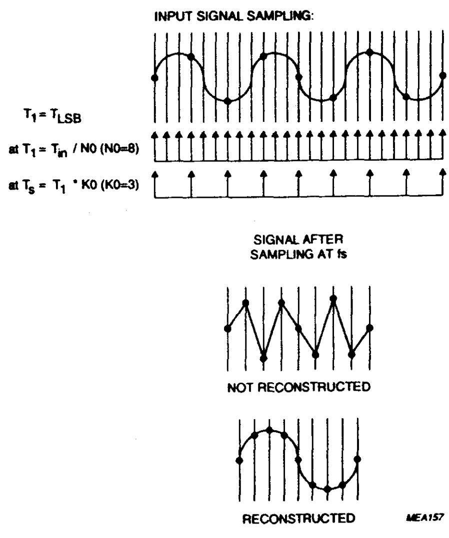

Fig.7 Principle of multi-beat frequency sampling

where the difference between K_0 and N_0 are relative primes. To minimize the sample acquisition time, the value of K_0 should however be the minimum permitted by the maximum conversion rate specified for the ADC under test.

The measurement bench uses every K_0th output from the ADC under test to compile a sampled sinewave acquired data file. The information in the data file, which is effectively a reconstruction of a sinewave which is a lower frequency aliased version of the input signal, is then analyzed to determine the ADC characteristics.

Measuring effective bits and harmonic levels

To determine the signal-to-noise ratio (SNR) and harmonic levels of our ADCs on the measurement bench, the data in the acquired sinewave file is transformed into the frequency domain with a fast Fourier transformation (FFT).

The levels of the signal, its harmonics and the noise can now be clearly seen and easily computed. The FFT is analyzed by the computer to determine $SNR = P_{signal}/P_{noise}$.

Instead of specifying SNR, it's possible to specify effective bits (b) which are defined as $b = (SNR - 1.76)/6.02$ where SNR is the calculated value in dB when a full-scale sinewave is analyzed.

By determining SNR as a function of input frequency, it's easy to determine the N-bit resolution bandwidth of an ADC which is equal to the input frequency at which the effective bits have decreased to N–0.5. For an 8-bit ADC, this occurs when the SNR is 46.9 dB.

High-performance 8-bit video data converters

Differential and integral non-linearity

Differential non-linearity (DNL) is a measure of the maximum amount by which the distance between the midpoints of adjacent steps on the ADC transfer function (quantized output level as a function of input level) differs from the width of one LSB. It is measured with a statistical test in which the acquired sinewave file is used to generate a histogram of the digitized signal with a number H(i) for each output code (i). The probability of obtaining each code is calculated and the ratio of the number of acquired samples of each code H(i) to the total No of samples (N_0) represents the differential non-linearity.

Integral non-linearity (INL) is a measure of the deviation of the ADC transfer function from the ideal. Since it is equal to the maximum difference between the measured and ideal quantization levels, it can be calculated from the histogram used to calculate DNL. Since INL(0) = DNL(0)/2. INL can be calculated for each step (i) of the transfer function as INL(i) = INL(i−1) + DNL(i)/2. The maximum value thus obtained is the integral non-linearity of the ADC.

Data timing

The relative timing of the output bits of the ADC can be displayed on the screen of the PC that forms part of the measurement bench. Acquisition of the timing data can be either synchronized with the ADC clock pulses at frequencies up to 1 GHZ, or asynchronous at frequencies up to 2 GHz.

APPLICATION SUPPORT

When designing data converters into a system, it is essential to pay careful attention to a number of circuit details to ensure that the high performance of our ICs is fully exploited. Correct PCB layout is particularly important, with particular emphasis on track widths, avoidance of ground loops and minimization of crosstalk between the analog and digital circuitry. Care must also be taken to understand the relative timing of the sampled and output data. Other important details include decoupling for noise reduction and stability of internal reference levels, decoupling and harmonic suppression for clock signals, and power supply filtering.

Line-locked digital colour decoding

Ton Nillesen – CAB-Elcoma, N.V. Philips, Eindhoven (The Netherlands)

On présente dans cet article une méthode de décodage numérique des signaux vidéo couleur basée sur des fréquences d'échantillonnage verrouillées sur la ligne. La fréquence d'échantillonnage est synthétisée à partir de la fréquence d'un cristal. On génère une fréquence stable de sous-porteuse en utilisant la fréquence variable d'échantillonnage par contrôle direct à partir du synthétiseur.

A digital colour decoding principle involving line-locked sample frequencies is presented. The sampling frequency is synthesized from a crystal frequency. A stable subcarrier frequency is generated from the variable sampling frequency by forward control from the synthesizer.

To digitally decode PAL or NTSC composite video signals in a TV receiver, it is advantageous for the sampling rate to be related to the colour subcarrier frequency because this simplifies the demodulator and the chroma filters. However after colour decoding, the component video signals for luminance and colour difference are available and the colour subcarrier is then no longer relevant. Line-locked sampling is then a better choice.
In fact, for video processing and conversion to other scanning frequencies, line-locked sampling is a natural choice because it results in orthogonal sampling, which simplifies video signal processing with line and field memories [1].

WHY LINE LOCKED ?

Standard conversion to other scanning frequencies might be used for instance for reduction of large area flicker by means of field rate conversion to higher frequencies. Another type of conversion is compression of the signals for features such as picture in picture and multi picture-in-picture, whereas expansion of the signals is required for picture enlargement or C-MAC decoding, etc..

Line-locked digital colour decoding

Some other examples of signal processing using line or field memories are :

- cross colour and cross luminance reduction with line-, field- or frame-combfilters,
- noise reduction by an integrating temporal filter,
- resolution enhancement by a peaking spatial filter.

Furthermore, a line-locked sample frequency is a must for matrix displays such as LCDs, the index tube and dot matrix printers and it is also a necessity for display of good quality characters.
And last but not least, the circuitry for processing line-locked component video signals is substantially independent of transmission standards.

APPLICATION OF SAMPLE RATE CONVERTER

If a subcarrier-locked colour decoder is used, line-locked samples can be obtained by sample rate conversion. An obvious approach for a Sample Rate Converter (SRC) is via digital-to-analog (DA) and analog-to-digital (AD) conversion. The subcarrier-locked samples are then converted to analog signals and re-sampled with the line-locked sample frequency (fig. 1a). Although this is a straigtforward method, using well-known techniques, it is not attractive because it is expensive. It requires ADCs and DACs, three of each for the three component signals, including the reconstruction filters, and a second clock generator. Furthermore, the additional conversion step degrades signal quality. A second approach is a SRC in the digital domain, the line-locked samples being calculated from surrounding subcarrier-locked samples by means of interpolating algorithms (fig. 1b). Both approaches require two clock generators coupled to the video signal, one burst-locked and the second line-locked.

However, it is not necessary to have the line-locked clock available with equidistant clock transitions. Transfer and processing of the samples with amplitude information belonging to line-locked sampling positions can be done with a gated version of the original clock (fig. 1c). The gated clock should then have a constant number of clock transitions per line period. However a reverse sample rate conversion is then required before DA-conversion. This second SRC is eliminated if the line-locked clock is physically available. DA-conversion is then done with the line-locked clock. However the most complex part of the sample rate conversion is the interpolating algorithm required [2].

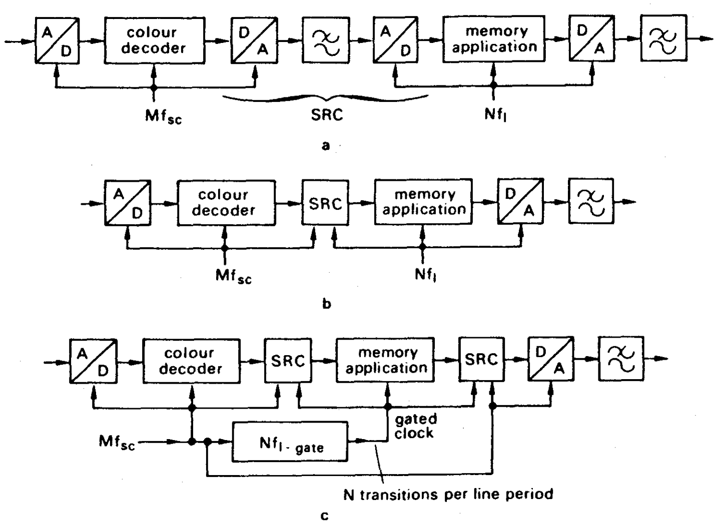

Fig. 1. Application of sample rate converters : a. anolog sample rate converter, b. digital sample rate converter and two clocks coupled to video signal, c. two digital sample rate converters and single clock.

Line-locked digital colour decoding

INTERPOLATION OF SAMPLES

In principle, interpolation is done by low-pass filtering. The low-pass filter should reject the sidebands of the original subcarrier-locked samples, including at harmonics of the sampling frequency, but should pass the baseband spectrum containing the desired signal with a flat frequency- and linear phase-characteristic. Linear interpolation is certainly not sufficient, neither in the passband nor in the stopband, to preserve good signal quality. Each new sample should therefore be calculated from several surrounding original samples with proper weighting factors. The weighting factors should be of sufficient number and sufficient accuracy to generate new samples with a timing accuracy of about 0.2 ns, if the resulting signal should have a bandwidth of 5 MHz and 8-bit quantization (fig. 2).

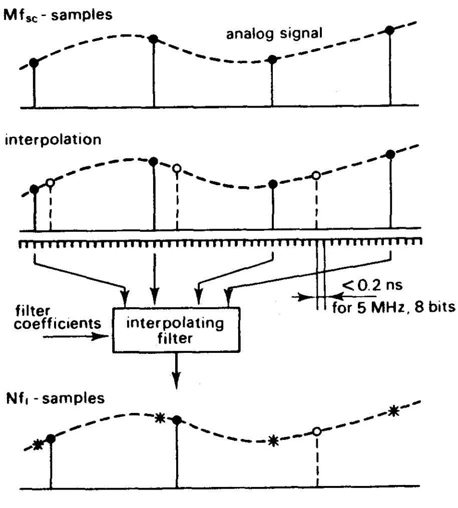

Fig. 2. Principle of sample rate conversion.

For compatibility with non-standard video signals with variable line frequencies, the conversion rate cannot be expressed as a simple ratio of small prime integers but is irrational and time-varying. As a consequence the interpolating filters will be complex with a large set of filter coefficients. A digital SRC will therefore require a relatively large chip area. These are the reasons for considering line-locked colour decoding which produces line-locked samples of the luminance and the colour difference signals directly.

COLOUR DECODING PRINCIPLE

The NTSC and PAL colour systems use suppressed-carrier amplitude modulation with quadrature subcarriers (fig. 3). The chroma signal can be demodulated by multiplying it by the correctly-phased subcarrier sine and cosine waves. This gives the colour difference signals plus some high frequency components,

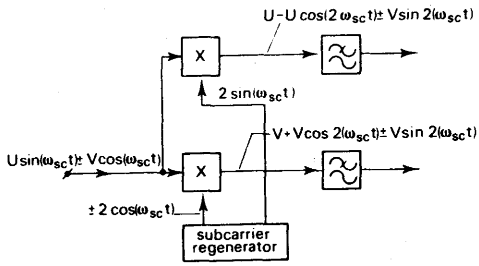

Fig. 3. Colour decoding principle for PAL system.

the latter being removed by filtering. For digital signals, the chroma signal has to be multiplied by the sampled subcarrier waves. If the sample rate is four times the subcarrier frequency, with the correct phase, the multiplications simplify to multiplication by 1, 0, −1 and 0 of successive samples. With line-locked or other sample frequencies asynchronous with the subcarrier, real four-quadrant multipliers are required for demodulation with the asynchronously-sampled subcarrier [3].
In the subcarrier regenerator (fig. 4) the subcarrier phase is coupled to the received colourbust. In order to reduce the effects of noise, the phase information extracted from several bursts is averaged by means of a narrow filter which in general is implemented as a phase locked loop (PLL). In analog circuits, the phase detector normally consists of a multiplier and the loop filter in a second order loop delivers an output signal which is partly proportional to the phase detector output signal and partly an integrated version of that signal. So digitally these blocks can be realised with adders, multipliers and an integrator.

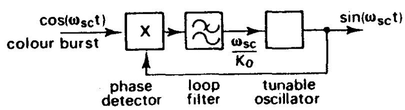

Fig. 4. Schematic diagram of the analog subcarrier regenerator.

Line-locked digital colour decoding

The tunable oscillator is normally a voltage controlled oscillator with an oscillator control sensitivity of K_0 ($rd \cdot s^{-1} \cdot V^{-1}$). So for an output frequency of ω_{sc}, the subcarrier frequency, the loop filter has to deliver a control voltage of ω_{sc}/K_0. For sinewave oscillators the instantaneous output is $\sin(\omega_{sc}t)$. As a consequence, the oscillator transfers the input signal ω_{sc}/K_0 to the output signal $\sin(\omega_{sc}t)$ which, apart from the sine function and the constant K_0, is an integrating action. The sine function prevents saturation of the output by the ever increasing value of the instantaneous phase. With the sine function the output phase follows the instantaneous phase modulo 2 π radians.

THE DISCRETE TIME OSCILLATOR (DTO)

The integrating and modulo function of the oscillator can be realised digitally with an accumulator consisting of an adder and D-flip-flops (fig. 5a). The multibit output of the adder is applied to its input via D-flip-flops which are clocked with the clock frequency f_{cl}. At the second input of the adder, a constant multibit value p is applied. So at each clock period the previous content of the accumulator is incremented by p until overflow occurs at the value q. The next value will then be the previous value plus p modulo q. So the output resembles a time discrete quantised sawtooth signal whose period is set by p. Obviously the ratio between p and q equals the ratio between the clock period and the period of the output signal f_0. So the control value p should be $f_0/f_{cl} \cdot q$. If the overflow value is defined as being 1, then the input value simplifies to $p = f_0/f_{cl}$ (fig. 5b).

That brings us to our definition of a discrete time oscillator (DTO) also known as ratio counter or rate multiplier or accumulator or numerically controlled oscillator. The input value should equal the ratio between the desired output frequency and the clock frequency. Its modulo 1 output indicates from zero to one the instantaneous phase within a single preriod (fig. 6).

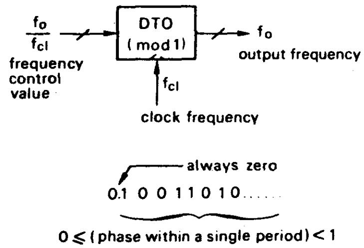

Fig. 6. The discrete time oscillator.

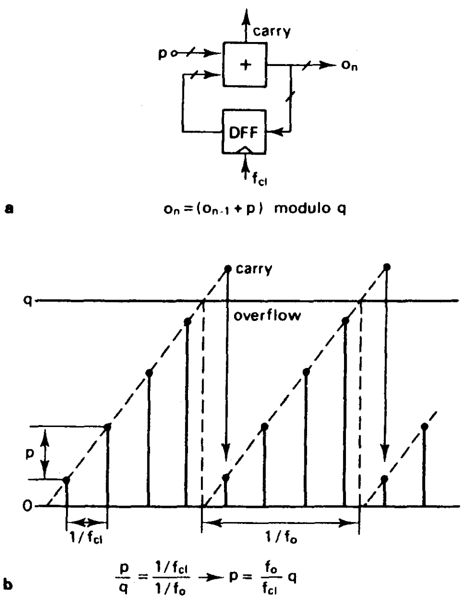

Fig. 5. Principle of the discrete time oscillator.

Note that the ratio f_0/f_{cl} at the input is dimensionless, indicating the phase increment per clock period, whereas the output of the DTO is the instantaneous phase modulo 1, which in principle is varying. Both signals can, in binary notation, be approximated to the required accuracy. However if the clock frequency is not constant whereas a constant subcarrier frequency should be generated, then the frequency control value should be corrected accordingly to the desired accuracy. As a consequence, the line-locked clock should be known with sufficient accurary and has therefore to be generated with a crystal frequency as reference.

Nf_l GENERATOR

It is a logical step to generate the line-locked sample frequency from a crystal frequency by means of a DTO. The DTO is clocked with the crystal frequency f_c and the desired output frequency is Nf_l, so the loop

Line-locked digital colour decoding

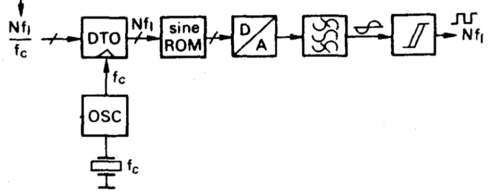

Fig. 7. Generation of line-locked sampling frequency (Nf_l) with crystal accuracy.

filter in the horizontal phase locked loop should deliver the numerical value Nf_l/f_c (fig. 7).
The DTO delivers then a quantised sawtooth signal with frequency Nf_l but in the discrete time domain sampled with the crystal clock f_c. However the sample frequency should be available as a continuous signal so that it can be used as the system clock. Therefore the DTO output signal is converted from digital to analog after a conversion from sawtooth to sinewave via a sine-ROM. The reconstruction filter delivers then an analog sinewave with no undesired harmonics or mixing products. That sinewave is then converted to the proper logical signal levels.
If this sample frequency generator is used in the horizontal phase locked loop, then the relationship between instantaneous sampling frequency and the crystal controlled reference frequency is known. As a consequence, the generated frequency control value Nf_l/f_c from the horizontal phase locked loop can be used to correct the DTO in the subcarrier loop for variations in Nf_l.

FORWARD CONTROL (DIVIDER)

Figure 8 shows the subcarrier phase locked loop with the burst phase detector, the loop filter, the DTO and the sine plus cosine ROM which delivers the demodulating sine and cosine waves. Between the loop filter and the DTO the correction is done for the varying clock frequency.

Since the subcarrier DTO operates with the line-locked clock, a value f_{sc}/Nf_l should be applied to its input as frequency control value. This value is obtained via an arithmetical divider (A/B) which divides the intermediate control value at the output of the subcarrier loop filter by Nf_l/f_c from the horizontal PLL. The intermediate control value should therefore be f_{sc}/f_c, the ratio between the subcarrier frequency and the crystal frequency. Apart from long-term variations, this ratio remains constant regardless of the clock frequency. Consequently, the subcarrier loop filter can be designed for narrow noise bandwidth, optimised for subcarrier regeneration. The inaccuracy of the forward control due to the limited wordlength of the signals is handled by the loop as internally-generated noise and can be chosen at a sufficiently low level.

LINE-LOCKED COLOUR DECODER

A complete block diagram of a line-locked colour decoder is presented in figure 9. For simplicity, several functions such as automatic colour control, colour killer, compensating delays etc. have been omitted in the block diagram. The signal-flow in the horizontal and subcarrier PLLs are indicated in heavy lines as is the correction circuit (A/B) which corrects the subcarrier DTO for varying line frequencies. The left-hand part of the circuit operates with the crystal controlled clock frequency f_c and generates the line-locked sampling frequency Nf_l with which the rest of the circuit operates. The coupling between these two parts is via the resynchronisation register R which delivers the control value Nf_l/f_c to the DTO.

In the synchronisation processing part, the Nf_l sample frequency is divided down to the line frequency f_l. The division ratio N can be made selectable to adapt the sample frequency to the bandwith of the video signal or to different line frequencies. The counter drives a state decoder which delivers several control

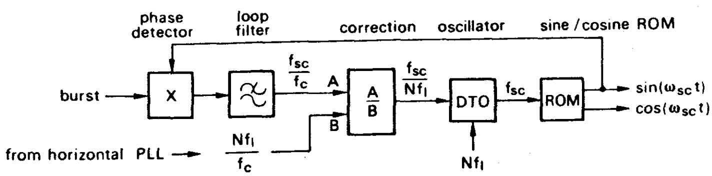

Fig. 8. Forward control of subcarrier DTO operating with line-locked clock.

Line-locked digital colour decoding

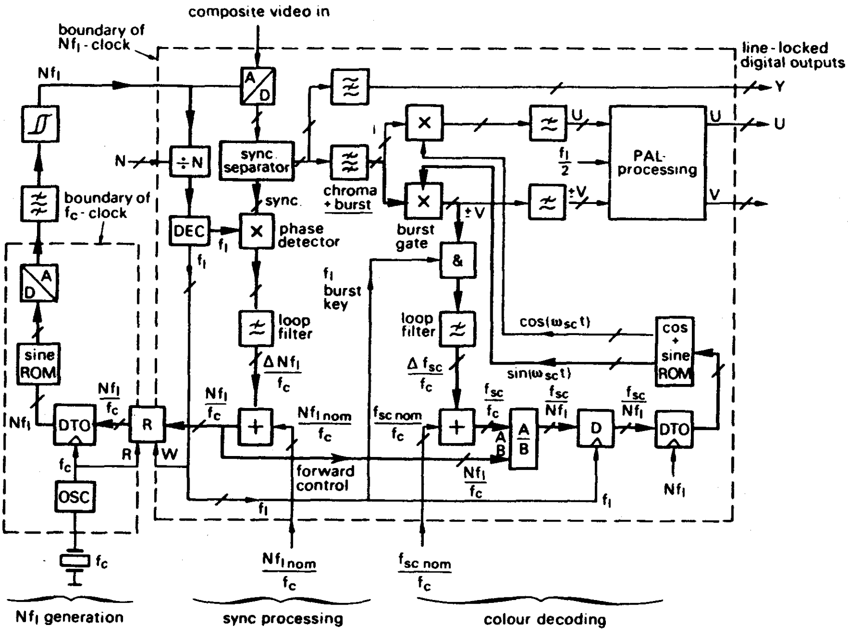

Fig. 9. Simplified block diagram of line-locked digital colour decoder.

signals at line frequency. One of these line frequency signals is applied to the horizontal phase detector where its phase is compared with the phase of the separated synchronisation signal. The result is applied to the loop filter and then added to the nominal input value ($Nf_{l\,nom}/f_c$) for the DTO. As a consequence the loop filter has only to deliver the error on the nominal value and the nominal value can be made selectable to accomodate different line frequencies or different numbers of samples per line.
The frequency control value has only to be updated once per line period. However updating the sample frequency also requires a new correction of the subcarrier DTO input value. For that reason the control values to both DTOs are effectuated on command of a line frequency signal f_l when both control values have been calculated. In fact the subcarrier DTO is updated somewhat later than the Nf_l-DTO to compensate for the delay of the video signals from ADC to demodulator. The synchronisation signal f_l acts as write clock for the resynchronisation buffer R. The new data is then clocked with f_c and applied to the input of the Nf_l-DTO. In the subcarrier DTO the new value becomes availables as soon as the D-flip-flops in front of the subcarrier DTO are clocked with a line frequency signal.

In the subcarrier loop the demodulated burst signal is used as actual phase information for subcarrier regeneration. For PAL the average V-phase of the burst is zero if the subcarrier phase is correct. So the V-demodulator together with the burstgate, consisting of a multiple input AND-gate, forms the phase detector. After passage through the loop filter, the result is added to the nominal frequency control value ($f_{sc\,nom}/f_c$) and divided by Nf_l/f_c. After the division, which takes several clock cycles, the result is applied to the DTO via the D-flip-flops.

To prevent side-locking, the loop filter output $\Delta f_{sc}/f_c$ should be limited so that the regenerated subcarrier remains close enough to the nominal value. The nominal value can be altered to accommodate the subcarrier frequency in different standards. This gives this system a clear advantage over conventional decoders. Although only a single crystal frequency f_c is present, any subcarrier can be regenerated with the proper accuracy only by changing the nominal frequency control value $f_{sc\,nom}/f_c$.

Let us consider now the analog part of the clock generation circuitry. The reconstruction filter and wave shaper for the Nf_l clock frequency can be implemented with an analog PLL. The advantages of this are :

- the filter curve tracks the input frequency so that the bandwidth can be smaller than with a fixed filter : this allows fewer bits to be used in the DA-converter ;

- several line-locked frequencies can be generated if the PLL is provided with dividers ;

- the entire circuit can be integrated.

Line-locked digital colour decoding

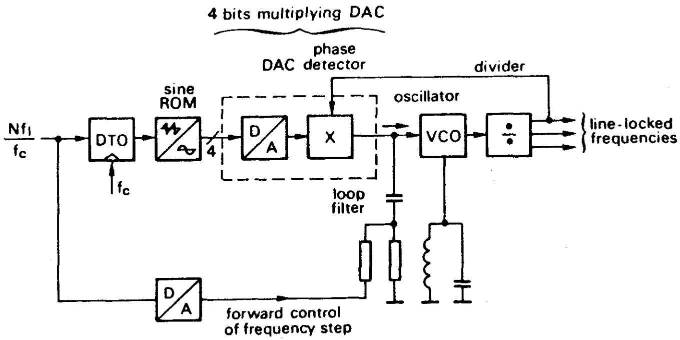

Fig. 10. Analog PLL as reconstruction filter.

Such an implementation is indicated in figure 10. The analog PLL is indicated with a charge pump phase detector, a loop filter, a voltage controlled oscillator (VCO) and the divider which delivers several line-locked frequencies. As a consequence the first part of the circuit can also operate on a subharmonic of the actual sample frequency.
The phase detector is driven by the DA-converter so that these functions can be combined in form of a multiplying DAC. Good results have been obtained with a 4 bit DAC so that this function can be very small in chip area. The required accuracy of the DAC of course is dependent on the quality of the reconstruction filter. A smaller filter bandwidth requires fewer bits for the DAC. However a narrow noise bandwidth of the PLL results in a slower response on frequency steps and consequently larger phase errors. That response can be improved by forward control of the oscillator to the required frequency. That information is available at the input of the Nf_l-DTO and could be used via DA-conversion for pre-correction of the VCO-frequency.

The factor N, which determines the sample frequency, can have any appropriate value. An attractive choice *is* $N=858$ for 60 Hz TV systems and $N=864$ for 50 Hz systems. The sampling frequency will then be 13.5 MHz which is in accordance with the CCIR recommendation for digital processing in studio equipment. The number of active samples per line period is then 720 for all TV standards.

CONCLUSION

In this presentation, the principle and the main advantages of line-locked colour decoding have been shown :

- owing to the orthogonal samples, line-locked decoding is optimized for the growing use of picture processing [4, 5] ;
- the system in principle is sample-rate-invariant so that it has excellent multi-standard capabilities and it enables the choice of a common clock for all standards ;
- for applications somewhat further in the future, it is quite important that the principle is directly applicable with matrix displays.

This article is written as a lecture (for ICCE 85 in Chicago).

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Digital interfaces for component video signals — AN ETV/IR89126

Author: A. H. Nillesen

Several coding parameters have to be specified for interconnecting the digital component video signals YD, UD and VD between several devices. For the digital studio environment the CCIR has made two recommendations on these parameters.

CCIR Recommendation 601 describes an extensive family of clock frequencies and the signal amplitudes, timing codes and auxiliary data for digital video component signals common to the 525- and 625-line TV standards. CCIR Recommendation 656 describes the means of interconnecting digital television equipment complying with the 4:2:2 encoding parameters as defined in Recommendation 601.

In the early eighties the basic sampling clock of digital circuits for TV receivers has been chosen, by Philips, Siemens and others, in accordance with the digital component studio standard CCIR Rec. 601, due to obvious benefits of having that parameter in common with the broadcasting side (e.g. MAC-decoding and descrambling). However with respect to signal amplitudes and multiplexing format a different choice was made. Possible benefits from the recommendations on these parameters were not seen, or considered as imaginary, whereas the drawbacks were considered as serious. This paper addresses the signal amplitudes and the multiplexing format which have been chosen for digital YUV interfaces in the TV receiver, including the extensions and revisions from later dates.

1. THE CONVERSION FACTOR

To express the amplitudes of the digital component signals, the conversion factor CF is defined as being the ratio between the digital and the normalized representation of the signal. Normalization is done to Red=Green=Blue=1 at peak white and the digital signals are represented on a scale of 256 (8 bits).

$$CF = \text{Conversion-Factor} = \frac{\text{digital signal amplitude on 8 bits scale}}{\text{normalised signal amplitude } (R_{max} = G_{max} = B_{max} = 1)}$$

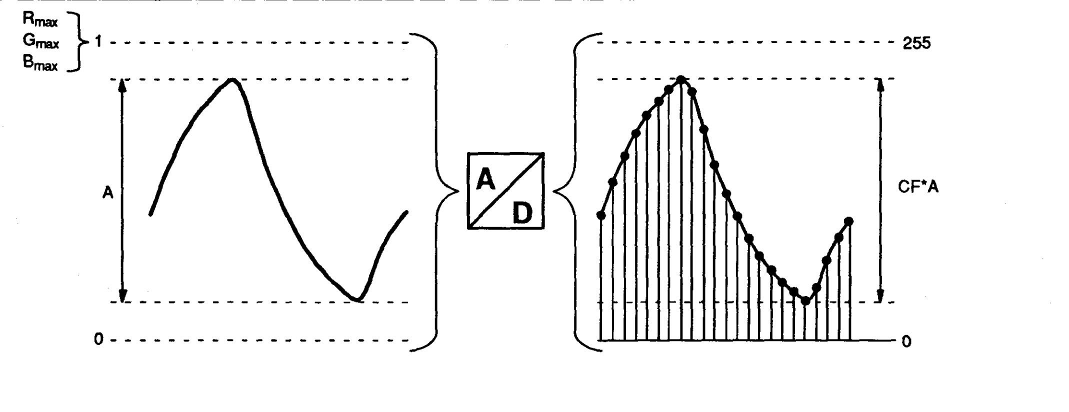


Figure 1. Definition of Conversion Factor CF

2. MAXIMUM AMPLITUDE OF NORMALIZED SIGNALS

With normalized signals the colour separation signals red, green and blue are unity at peak white: $R_{max}=G_{max}=B_{max}=1$.

The colour equations for broadcast signals are based on the NTSC primaries as specified in CCIR Report 624-2. The resulting equation for the luminance signal is:

$$Y=0.299*R+0.587*G+0.114*B \qquad (2.1)$$

which gives: Yp-p=1

|B-Y| is maximum for R,G,B=0.0,1 (=blue)
or R,G,B=1,1,0 (=yellow=white minus blue)
which gives: (B-Y)p-p=2*(1-0.114)=1.772

|R-Y| is maximum for R,G,B=1,0,0 (=red)
or R,G,B=0,1,1 (=cyan=white minus red)
which gives: (R-Y)p-p=2*(1-0.299)=1.402

maximum amplitudes of normalized signals
$Y_{p-p}=1$, $(B-Y)_{p-p}=1.772$, $(R-Y)_{p-p}=1.402$

(2.2)

3. MAIN CODING PARAMETERS OF CCIR REC. 601/656

The digital component signals according to CCIR Rec. 601 have been chosen such that, coded in straight binary

- digital levels 0 and 255 are reserved for synchronization data.
- the luminance signal is to occupy only 220 quantisation levels, to provide working margins, and that black is at level 16.
- the colour difference signals are to occupy 225 quantisation levels and that the zero level is to be level 128 in order to cope with the bipolar nature of the colour difference signals.

The conversion factors follow from these limits on the digital signal range and the maximum peak-to-peak value of the normalized signals:

$$signal_{p-p} * CF = digital\text{-}limit$$

luminance: $Y_{p-p} * CF_y = 219$, which gives $CF_y = 219$

colour difference: $(B-Y)_{p-p} * CF_u = 224$, $CF_u = 126$
$(R-Y)_{p-p} * CF_v = 224$, $CF_v = 160$

The resulting digital component signals CY, CU, CV are: [1]

CCIR digital YUV:		
CY=219*Y+16	} binary coded	(3.1)
CU=126*(B-Y)+128		(3.2)
CV=160*(R-Y)+128		(3.3)

- the data words 0 and 255 are reserved for data identification
- the video data words are conveyed (CCIR Rec. 656) as a 27Mwords/second multiplex in the following order:
  CU,CY,CV,CY,CU,CY,CV, etc.

in which the word sequence CU,CY,CV, refers to cosited luminance and colour-difference samples and the following word, CY, corresponds to the next luminance sample.

4. PARAMETERS TO BE CONSIDERED FOR TV RECEIVERS

Without doubt the characteristics of analog or digital video component signals at broadcasting side and receiving end are quite different due to the large differences in environment and cost/performance. As a consequence the coding characteristics of digital interface signals are influenced differently by several parameters. Regarding signal amplitudes:

- maximum digital resolution should be balanced against:
- margin for static and dynamic amplitude changes, i.e. tolerances and multiplicative noise (echo, tilt).
- margin for additive noise.
- margin for filter overshoots
- probable limit on saturation

Also on the ratio between signal amplitudes some criteria should be considered:

- simple gain correction to normalized signals e.g. matrixing.
- simple correction between digital decoder and interface.

The list can be extended with requirements from EMC, limitations or advantages of certain IC technologies, application specific requirements etc. Although no choice is best in all cases, consensus is required on the major coding characteristics, due to obvious benefits of standardization. The agreement on this subject between system engineers from the Consumer-Electronics and the Components divisions of Philips (and others) will be explained in the following chapters.

5. MAIN CODING PARAMETERS FOR DIGITAL TV

The component video signals for digital TV are specified as:

digital TV signals:		
YD=192*Y+16	straight binary	(5.1)
UD=3/4*192*(B-Y)	} two's-complement	(5.2)
VD=192*(R-Y)		(5.3)

- multiplex formats are specified for sampling ratios of 4:1:1 and 4:2:2

1) CCIR recommendations use different nomenclature: Y, C_B, C_R.

The colour difference signals are coded in two's complement in order to fit directly to digital arithmetic functions. The difference with the offset binary coding of the CCIR signals (3.1-3.3) is an inversion of the MSB. Concerning the specified conversion factors it will be shown that several criteria on the coding parameters are fulfilled simultaneously:

- digital resolution is practically optimum for 75% colour difference amplitudes.
- signal amplitudes fit conveniently to D2MAC decoders, taking into account 30% headroom for noise.
- UD/VD ratio fits conveniently to the required gain matching ratio for PAL/NTSC colour difference signals.
- amplitude margin is in accordance with the amplitude tolerance of analog decoded signals.
- matrixing to colour selection signals is simple

6. PEAK AMPLITUDE RATIOS

The amplitude ratios should be chosen such that

- the maximum amplitudes are more or less equal in order to maximize digital resolution
- simple gain ratios are required for matrixing
- required correction of the decoded signals is simple

in which 'simple' means that the required gain can be realized with very few additions.

6.1. Probable Maximum Saturation

Due to the gamma of the picture tube the displayed saturation will be higher than the electrical saturation except at 100%. Saturation is less than 100% if the displayed colour has a certain white content, which means that none of the the RGB signals then becomes zero but have a minimum non-zero value. That minimum value becomes relatively smaller if it is displayed via the gamma of the picture tube.

The electrical saturation can be expressed as $\frac{E_{max} - E_{min}}{E_{max}} = 1 - \frac{E_{min}}{E_{max}}$

from which follows: $\text{displayed saturation} = 1 - \left[\frac{E_{min}}{E_{max}}\right]^{gamma}$

in which Emin is the minimum value of the RGB signals in coloured areas
Emax is the maximum value of the RGB signals in coloured areas
gamma is the gamma of the drive-to-output display characteristic.

As a consequence a minor reduction of the maximum displayed saturation will result in a significant reduction of the maximum amplitude of the colour difference signals, e.g. only 5% reduction of the maximum displayed saturation at maximum intensity results from 30% reduction of the electrical saturation at gamma=2.4.

Therefore it is important to take into account that it is most unlikely that natural scenes contain fully saturated colours at maximum intensity. PAL and NTSC have been specified such that at maximum saturation the modulated subcarrier would never swing 'blacker-than-black' by more than 33%. As a consequence the composite signal reaches 100% amplitude at 1/1.33=75% amplitude of saturated colours (yellow and cyan in 100.0.75.0 EBU colour bars). On the same ground also D2MAC colour difference signals are specified for only 77% maximum electrical amplitude. Furthermore the most common luminance step colour bar signals used as test signal result in colour difference signals at 75% of their theoretical maximum amplitude [1].

For these reasons it is supposed that the colour difference signals will most probably not exceed 75% of their theoretical maximum value, which corresponds to 96% maximum displayed saturation at a practical value of gamma=2.4. [2)]

6.2. Ratio of Conversion Factors

For equal amplitudes of the digital signals the ratio of the conversion factors should be inversely proportional to the analog amplitudes. As a consequence the ratio of the conversion factors for equal peak amplitudes at 75% maximum electrical saturation is given by

$$CF_Y : CF_U : CF_V = \frac{1}{Y_{p-p}} : \frac{1}{0.75 \cdot (B-Y)_{p-p}} : \frac{1}{0.75 \cdot (R-Y)_{p-p}}$$

Substitution of (2.2) gives CF_Y:CF_U:CF_V=1.0.75:0.95 which, after rounding to simple integers, results in:

$$\boxed{CF_Y : CF_U : CF_V = 4:3:4} \qquad (6.2)$$

2) It should be noted that the gamma of TV cathode ray tubes is about 2.4 whereas the 'transmitted' gamma is nominally 2.8 which results in an overall gamma of 1.2.

With these simple factors, which will lead to simple (digital) matrixing for R and B, the probable maximum amplitudes of the digital signals are practically equal which gives optimum digital resolution.

6.3. U/V Gain Matching for PAL and NTSC

In NTSC and PAL the colour difference signals U=(B-Y)' and V=(R-Y)' used to modulate the subcarrier are reduced in amplitude with respect to the normalized signals:

$$U=0.493*(B-Y) \quad (6.3)$$

$$V=0.877*(R-Y) \quad (6.4)$$ [3]

As a consequence gain correction is required to obtain normalized signal amplitudes from the demodulated U and V signals. The required gain matching ratio, derived from (6.3) and (6.4), equals 0.493/0.877=9/16. Therefore the ratio $CF_U/CF_V=3/4$ fits very conveniently to the required gain matching ratio for U/V from decoded PAL or NTSC signals. If the decoded V signal is first reduced with 3/4 (one adder) then the remaining 'error' is 3/4, being the desired CF_U/CF_V. The final correction of 3/4, which will result in equal conversion factors, should then be applied just before or just after DA-conversion to obtain analog colour difference signals with normalized amplitudes, which is common practice for TV receivers.

7. DIGITAL SIGNAL AMPLITUDES

The worst case margins required for noise and amplitude tolerances are quite large. Linear or statistical addition of these margins would lead to insufficient digital resolution at quantisation in 8 bits. As an example, statistical addition of

- 30% headroom for noise (subchapter 7.1)
- 18% tolerance on transmitted burst-to-chrominance ratio [2]
- 2dB gain tolerance of analog decoders (subchapter 7.2)

would require a total range for the colour difference signals of more than two times the nominal value. Therefore the conversion factors have been chosen such

- that there is sufficient margin in amplitude to handle the tolerance of analog decoders

and

- that the margin is according to the 'headroom' for additive noise as proposed by the EBU for D2MAC signals.

If, for certain applications, the margin is considered as insufficient then a kind of gain control should be applied. Gain control on the CVBS signal in front of the digital decoder is already common practice (TDA8708). However automatic gain correction of component signals, i.e. signals originating from external RGB (SCART) or analog decoders, is far more complicated. Detection and control of the amplitudes should then be done on the three component signals simultaneously.

7.1. noise

The criterion for noise handling capability in this context is the probability that signal quality is degraded by noise clipping due to signal quantisation. A probability of one sample per line (about 10^{-3}) seems a reasonable measure for good noise behavior. Assuming that the noise has a Gaussian distribution (white noise), the peak value to be taken into account is then approximately three times the rms value, six times for the peak-to-peak value.

Signal-to-noise-ratios below 0dB are normal operating conditions in the design of TV circuits. E.g. for burst processing it is common practice to design the subcarrier regenerator for stable output (less than 5 degree rms phase noise) at S/N=-10dB ($CVBS_{p-p}/Noise_{rms}$) [3]. In that case the required margin for noise amplitude would be approximately twenty times larger then the CVBS signal amplitude.

Although it is unlikely that such a margin is present in the analog prestages at nominal CVBS amplitude, it is obvious that a compromise is necessary between quantisation noise and the margin for external noise. Therefore the worst probable case of S/N for D2MAC reception is used as a guideline [4].

In the D2MAC system the carrier is frequency-modulated by the baseband signal [5]. In FM systems there is a rather sharp threshold between carrier-to-noise ratios for 'good' and 'bad' S/N of the demodulated signal. Therefore the assumption is made that the worst probable S/N for D2MAC reception occurs at a carrier-to-noise ratio of 11dB, just above the threshold. That results in an unweighted noise level of about -26dB (=0.05) [4,6] for the demodulated signal (depending on the filter response of the prestages). That means that 6*0.05=30% headroom has to be taken into account for additive noise.

7.2. MAC Decoder

MAC decoding in principle is time-demultiplexing. Therefore the MAC decoder is transparent (no internal gain) with respect to digital amplitudes. If the MAC (mid-range) clamping level is referred to as zero and if the peak-to-peak range is unity, then the MAC signals according to the D2-MAC specification [5] are transmitted as:

$$Ym=Y-0.5,\ Um=0.733*(B-Y)\ \text{and}\ Vm=0.927*(R-Y) \quad (7.1)$$ [4]

It is supposed that regarding DC level:

3) In NTSC the vectors I and Q are also derived from (B-Y)' and (R-Y)'.

– the digitized grey clamping level equals 128 (analog 'zero' becomes digital 128)

and regarding AC input:
– the ratio between the nominal digital peak-to-peak amplitude and the maximum range (256) of the ADC equals MR (Modulation Range).

then the corresponding digital component signals will be (See Fig. 2):

```
MY=128+MR*256*(Y-0.5)                    (7.2)
MU=128+MR*256*0.733*(B-Y)                (7.3)
MV=128+MR*256*0.927*(R-Y)                (7.4)
```

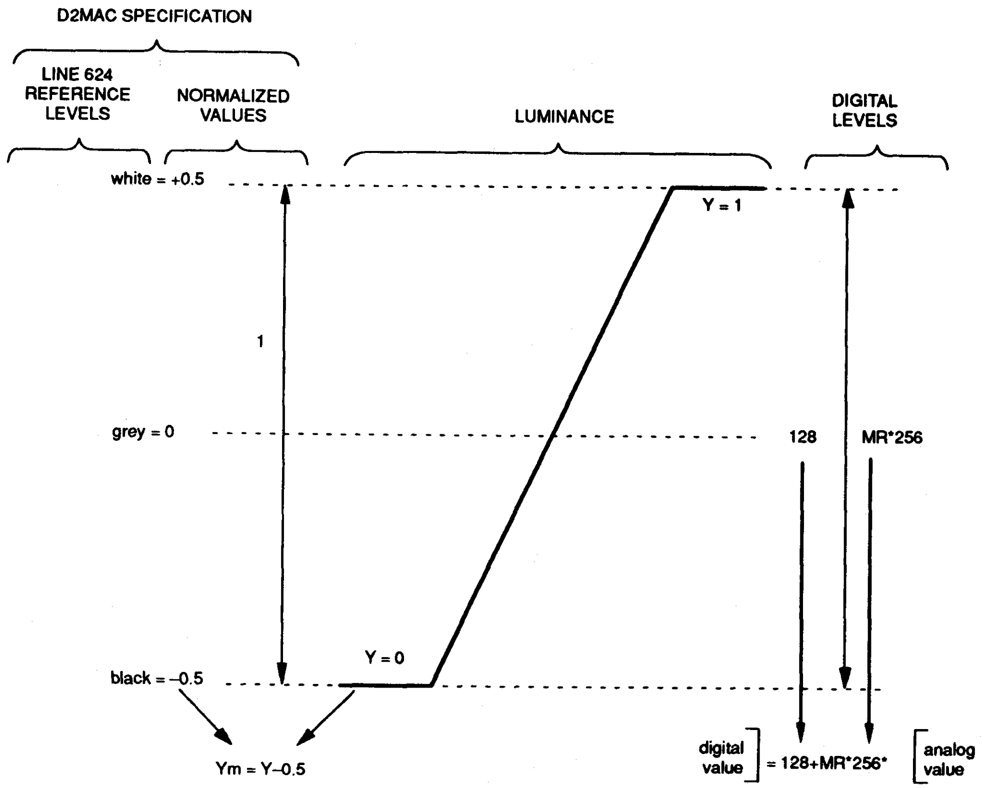


Figure 2. Relation Between Analog and Digital D2MAX Baseband Signals

4) The colour difference signals in the D2MAC multiplex are scaled to unity amplitude at 77% of their maximum value. As a consequence the scale factors for B-Y and R-Y are 1/(0.77*1.772)=0.733 and 1/(0.77*1.402)=0.927 respectively.

With 30% headroom for additive noise (MR=0.77) the decoded signals (7.2)-(7.4) and the resulting conversion factors become:

$MY=197*Y+29 \quad CF_Y=197$ (7.5)
$MU=144*(B-Y)+128 \quad CF_U=3/4*192$ (7.6)
$MV=183*(R-Y)+128 \quad CF_V=183=192/1.05$ (7.7)

Consequences for interfacing:
- luminance black level should be corrected to 16 (one adder).
- error on CFy results in an acceptable saturation error
- V-signal has to be corrected with 192/183w17/16*63/64 (two adders)
- no correction is needed for the U-signal

7.3. Analog Decoder

An accepted value for the specified tolerance on the output signals of analog colour decoders (e.g.TDA4555) is +/-2dB (0.8-1.25). With a fixed digital black level of 16 the available range for luminance is 255-16+1=240. Reduction with 2dB, rounded to the nearest multiple of 4 (resulting in an integer value for CFu), gives a nominal range of 192. That means that the digital interface signals (CF_Y=192) can also handle the amplitude tolerance of analog decoders.

7.4. Digital PAL Decoder

In PAL and NTSC decoders the amplitude of the demodulated U and V signals is, via action of Automatic Colour Control (ACC), directly related to the amplitude of the colour burst. For PAL the relation can be derived from

BP=peak burst amplitude=3/7

Substitution in in (6.3) and (6.4) gives

$U=1.15*BP*(B-Y)$ and $V=2.05*BP*(R-Y)$ (7.8)

If the burst peak amplitude in the digital PAL decoder is kept at BP=125 and the amplitude of the V signal is reduced with 3/4 then the resulting UD and VD signals become:

$UD=1.15*125*(B-Y)=3/4*192*(B-Y)$ (7.9)
$VD=3/4*2.05*125*(R-Y)=192*(R-Y)$ (7.10)

which is in accordance with the desired interface signals (5.1)-(5.3).

7.5. Digital Matrixing

For certain applications, e.g. gamma correction for LCD, it might be required to operate on colour separation signals rather than colour difference signals. With six adders the YD, UD and VD signals can be matrixed to digital luminance, red and blue signals normalized to a conversion factor of 216.

luminance:	216*Y=9/8*YD	(one adder)	(7.11)
red:	216*R=9/8*YD+3/2*UD	(three adders)	(7.12)
blue:	216*B=9/8*(YD+VD)	(two adders)	(7.13)

These signals cover 90% (216) of the total range from black (16) to maximum (255).

8. DATA MULTIPLEXING

The video interface signal according to CCIR Rec.656 is based on 4:2:2 sample ratio. For digital TV the 4:1:1 sample ratio is an attractive alternative, in particular for memory based processing of video originating from decoded CVBS signals. Therefore data formats have been specified for 4:1:1 and 4:2:2 The luminance and colour difference signals are conveyed as separate data with identical clock rate according to the luminance sample rate, 13.5MHz or 27MHz in case of frequency doubling. Luminance data is transferred on eight data lines, whereas the colour difference signals are multiplexed on four or eight data lines.

The 4:2:2 multiplex format is chosen such that it can simply be made from the multiplexed data according to CCIR Rec.656. In the 4:1:1 format the UD and VD signals are multiplexed on separate data lines. The multiplex formats of the colour difference samples are given in the following tables together with the cosited luminance sample.

'4:2:2' format

dataline	samplebits	
Y7 Y6 ... Y0	T7 Y6 ... Y0	next Y
C7 C6 ... C0	U7 U6 ... U0	V7 V6 ... V0
time-slot	0	1

'4:1:1' format

dataline	samplebits			
Y7 76 ... Y0	Y7 Y6 ... Y0	next Y-samples		
C7 C6 C5 C4	U7 U6 V7 V6	U5 U4 V5 V4	U3 U2 V3 V2	U1 U0 V1 V0
time-slot	0	1	2	3

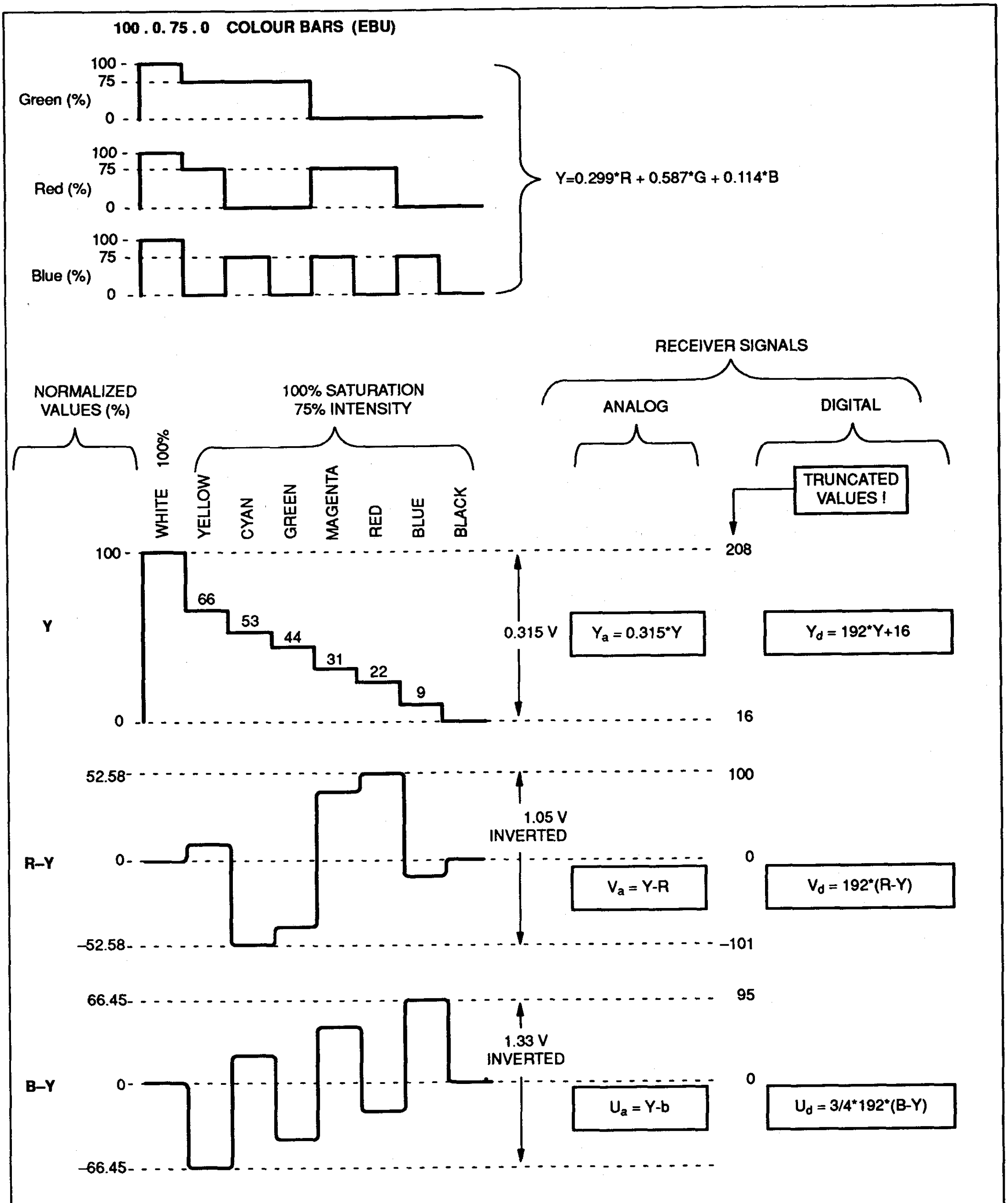
The start of the multiplex frame is identified by the positive going edge of a control signal (BLN or HREF or MUX, depending on the integrated circuit used as source).

9. CONCLUSION

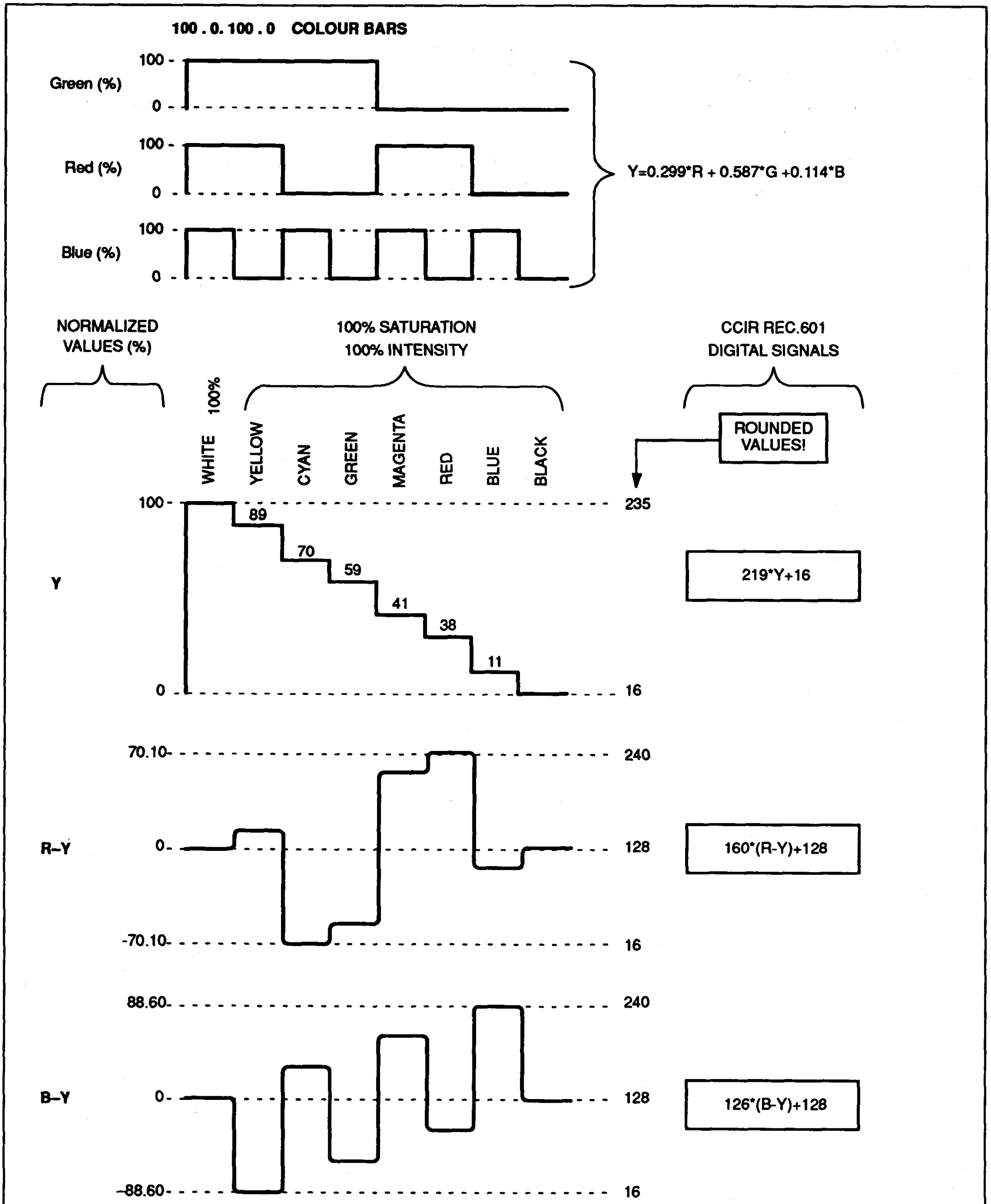
Signal amplitudes and multiplexing formats for digital component video signals as used for interconnecting TV receiver functions are based on receiver specific requirements. Concerning amplitudes the following criteria are fulfilled:

- digital resolution is practically optimum for 75% colour difference amplitudes.
- signal amplitudes fit conveniently to D2MAC decoders, taking into account 30% headroom for noise.
- UD/VD ratio fits conveniently to the required gain matching ratio for PAL/NTSC colour difference signals.
- amplitude margin is in accordance with the amplitude tolerance of analog decoded signals.
- matrixing to colour selection signals is simple Data multiplexing parameters are specified for:
- 4:2:2 as well as 4:1:1 sample frequency ratio to cope with different bandwidths, in particular for memory applications
- clock frequency equal to luminance sample frequency for application with or without frequency doubling

The following figures give the characteristic amplitudes of the digital component video signals according to the specifications for application in TV receivers and according to CCIR Rec.601.



TV Receiver Signals for 100.0.75.0 Colour Bars



Digital Component Video Signals According to CCIR Rec. 601 for 100.0.100.0 Colour Bars

REFERENCES

[1] CCIR Recommendation 471-1; "Nomenclature and description of colour bar signals"

[2] IBA Technical Review, part 2 Technical Reference Book, July 1974

[3] Donald Richman; Proc. IRE, vol. 43, 1954; "Colour-carrier reference phase synchronization accuracy in NTSC colour television"

[4] Appendix to part 2 of [5]; "Guidelines for system implementation"

[5] EBU Technical centre; Tech.3258-E; October 1986; "Specification of the systems of the MAC/packet family"

[6] Arno Neelen, Philips Components division, PCALE; private communication.

RECOMMENDATION 601-2

ENCODING PARAMETERS OF DIGITAL TELEVISION FOR STUDIOS*

(Question 25/11, Study Programmes 25G/11, 25H/11)

(1982-1986-1990)

The CCIR,

CONSIDERING

(a) that there are clear advantages for television broadcasters and programme producers in digital studio standards which have the greatest number of significant parameter values common to 525-line and 625-line systems;

(b) that a world-wide compatible digital approach will permit the development of equipment with many common features, permit operating economies and facilitate the international exchange of programmes;

(c) that an extensible family of compatible digital coding standards is desirable. Members of such a family could correspond to different quality levels, facilitate additional processing required by present production techniques, and cater for future needs;

(d) that a system based on the coding of components is able to meet some, and perhaps all, of these desirable objectives;

(e) that the co-siting of samples representing luminance and colour-difference signals (or, if used, the red, green and blue signals) facilitates the processing of digital component signals, required by present production techniques,

UNANIMOUSLY RECOMMENDS

that the following be used as a basis for digital coding standards for television studios in countries using the 525-line system as well as in those using the 625-line system:

1. Component coding

The digital coding should be based on the use of one luminance and two colour-difference signals (or, if used, the red, green and blue signals).

The spectral characteristics of the signals must be controlled to avoid aliasing whilst preserving the passband response. When using one luminance and two colour-difference signals as defined in Table I of RECOMMENDS 4, suitable filters are defined in Annex III, Figs. 1 and 2. When using the E'_R, E'_G, E'_B signals or luminance and colour-difference signals as defined in Table II of Annex I, a suitable filter characteristic is shown in Fig. 1 of Annex III.

* Main digital television terms used in the Recommendation are defined in Report 629.

Encoding parameters of digital television for studios — CCIR REC. 601-2

2. Extensible family of compatible digital coding standards

The digital coding should allow the establishment and evolution of an extensible family of compatible digital coding standards.

It should be possible to interface simply between any two members of the family.

The member of the family to be used for the standard digital interface between main digital studio equipment, and for international programme exchange (i.e. for the interface with video recording equipment and for the interface with the transmission system) should be that in which the luminance and colour-difference sampling frequencies are related in the ratio 4 : 2 : 2.

In a possible higher member of the family the sampling frequencies of the luminance and colour-difference signals (or, if used, the red, green and blue signals) could be related by the ratio 4 : 4 : 4. Tentative specifications for the 4 : 4 : 4 member are included in Annex I (see Note).

Note – Administrations are urgently requested to conduct further studies in order to specify parameters of the digital standards for other members of the family. Priority should be accorded to the members of the family below 4 : 2 : 2. The number of additional standards specified should be kept to a minimum.

3. Specifications applicable to any member of the family

3.1 Sampling structures should be spatially static. This is the case, for example, for the orthogonal sampling structure specified in § 4 of the present Recommendation for the 4 : 2 : 2 member of the family.

3.2 If the samples represent luminance and two simultaneous colour-difference signals, each pair of colour-difference samples should be spatially co-sited. If samples representing red, green and blue signals are used they should be co-sited.

3.3 The digital standard adopted for each member of the family should permit world-wide acceptance and application in operation; one condition to achieve this goal is that, for each member of the family, the number of samples per line specified for 525-line and 625-line systems shall be compatible (preferably the same number of samples per line).

4. Encoding parameter values for the 4 : 2 : 2 member of the family

The following specification (Table I) applies to the 4 : 2 : 2 member of the family, to be used for the standard digital interface between main digital studio equipment and for international programme exchange.

Encoding parameters of digital television for studios — CCIR REC. 601-2

TABLE I – *Encoding parameter values for the 4 : 2 : 2 member of the family*

Parameters	525-line, 60 field/s (1) systems	625-line, 50 field/s (1) systems
1. Coded signals: Y, C_R, C_B	These signals are obtained from gamma pre-corrected signals, namely: E'_Y, $E'_R - E'_Y$, $E'_B - E'_Y$ (Annex II, § 2 refers)	
2. Number of samples per total line: – luminance signal (Y) – each colour-difference signal (C_R, C_B)	 858 429	 864 432
3. Sampling structure	Orthogonal, line, field and frame repetitive. C_R and C_B samples co-sited with odd (1st, 3rd, 5th, etc.) Y samples in each line	
4. Sampling frequency: – luminance signal – each colour-difference signal	13.5 MHz (2) 6.75 MHz (2) The tolerance for the sampling frequencies should coincide with the tolerance for the line frequency of the relevant colour television standard	
5. Form of coding	Uniformly quantized PCM, 8 bits per sample, for the luminance signal and each colour-difference signal	
6. Number of samples per digital active line: – luminance signal – each colour-difference signal	 720 360	
7. Analogue-to-digital horizontal timing relationship: – from end of digital active line to 0_H	16 luminance clock periods	12 luminance clock periods
8. Correspondence between video signal levels and quantization levels: – scale – luminance signal – each colour-difference signal	 0 to 255 220 quantization levels with the black level corresponding to level 16 and the peak white level corresponding to level 235. The signal level may occasionally excurse beyond level 235 225 quantization levels in the centre part of the quantization scale with zero signal corresponding to level 128	
9. Code-word usage	Code-words corresponding to quantization levels 0 and 255 are used exclusively for synchronization. Levels 1 to 254 are available for video	

(1) See Report 624, Table I.

(2) The sampling frequencies of 13.5 MHz (luminance) and 6.75 MHz (colour-difference) are integer multiples of 2.25 MHz, the lowest common multiple of the line frequencies in 525/60 and 625/50 systems, resulting in a static orthogonal sampling pattern for both.

Encoding parameters of digital television for studios — CCIR REC. 601-2

ANNEX I

TENTATIVE SPECIFICATION OF THE 4:4:4 MEMBER OF THE FAMILY

This Annex provides for information purposes a tentative specification for the 4 : 4 : 4 member of the family of digital coding standards.

The following specification could apply to the 4 : 4 : 4 member of the family suitable for television source equipment and high quality video signal processing applications.

TABLE II – *A tentative specification for the 4 : 4 : 4 member of the family*

Parameters	525-line, 60 field/s systems	625-line, 50 field/s systems
1. Coded signals: Y, C_R, C_B or R, G, B	These signals are obtained from gamma pre-corrected signals, namely: E'_Y, $E'_R - E'_Y$, $E'_B - E'_Y$ or E'_R, E'_G, E'_B	
2. Number of samples per total line for each signal	858	864
3. Sampling structure	Orthogonal, line, field and frame repetitive. The three sampling structures to be coincident and coincident also with the luminance sampling structure of the 4 : 2 : 2 member	
4. Sampling frequency for each signal	13.5 MHz	
5. Form of coding	Uniformly quantized PCM. At least 8 bits per sample	
6. Duration of the digital active line expressed in number of samples	At least 720	
7. Correspondence between video signal levels and the 8 most significant bits (MBS) of the quantization level for each sample:		
– scale	0 to 255	
– R, G, B or luminance signal (1)	220 quantization levels with the black level corresponding to level 16 and the peak with level corresponding to level 235. The signal level may occasionally excurse beyond level 235	
– each colour-difference signal (1)	225 quantization levels in the centre part of the quantization scale with zero signal corresponding to level 128	

(1) If used.

ANNEX II

DEFINITION OF SIGNALS USED IN THE DIGITAL CODING STANDARDS

1. Relationship of digital active line to analogue sync. reference

The relationship between 720 digital active line luminance samples and the analogue synchronizing references for 625-line and 525-line systems is shown below.

TABLE III

525-line, 60 field/s systems	122 T	720 T	16 T	
0_H (leading edge of line syncs., half-amplitude reference)		Digital active-line period	0_H	Next line
625-line, 50 field/s systems	132 T	720 T	12 T	

T: one luminance sampling clock period (74 ns nominal).

The respective numbers of colour-difference samples can be obtained by dividing the number of luminance samples by two. The (12, 132) and (16, 122) were chosen symmetrically to dispose the digital active line about the permitted variations. They do not form part of the digital line specification and relate only to the analogue interface.

2. Definition of the digital signals Y, C_R, C_B, from the primary (analogue) signals E'_R, E'_G and E'_B

This section describes, with a view to defining the signals Y, C_R, C_B, the rules for construction of these signals from the primary analogue signals E'_R, E'_G and E'_B. The signals are constructed by following the three stages described in § 2.1, 2.2 and 2.3 below. The method is given as an example, and in practice other methods of construction from these primary signals or other analogue or digital signals may produce identical results. An example is given in § 2.4.

2.1 *Construction of luminance (E'_Y) and colour-difference ($E'_R - E'_Y$) and ($E'_B - E'_Y$) signals*

The construction of luminance and colour-difference signals is as follows:

$$E'_Y = 0.299E'_R + 0.587E'_G + 0.114E'_B \qquad \text{(See Note)}$$

whence:

$$\begin{aligned}(E'_R - E'_Y) &= E'_R - 0.299E'_R - 0.587E'_G - 0.114E'_B \\ &= 0.701E'_R - 0.587E'_G - 0.114E'_B\end{aligned}$$

and:

$$\begin{aligned}(E'_B - E'_Y) &= E'_B - 0.299E'_R - 0.587E'_G - 0.114E'_B \\ &= -0.299E'_R - 0.587E'_G + 0.886E'_B\end{aligned}$$

Note. – Report 624 Table II refers.

Taking the signal values as normalized to unity (e.g., 1.0 V maximum levels), the values obtained for white, black and the saturated primary and complementary colours are as follows:

TABLE IV

Condition	E'_R	E'_G	E'_B	E'_Y	$E'_R - E'_Y$	$E'_B - E'_Y$
White	1.0	1.0	1.0	1.0	0	0
Black	0	0	0	0	0	0
Red	1.0	0	0	0.299	0.701	−0.299
Green	0	1.0	0	0.587	−0.587	−0.587
Blue	0	0	1.0	0.114	−0.114	0.886
Yellow	1.0	1.0	0	0.886	0.114	−0.886
Cyan	0	1.0	1.0	0.701	−0.701	0.299
Magenta	1.0	0	1.0	0.413	0.587	0.587

2.2 *Construction of re-normalized colour-difference signals (E'_{C_R} and E'_{C_B})*

Whilst the values for E'_Y have a range of 1.0 to 0, those for $(E'_R - E'_Y)$ have a range of +0.701 to −0.701 and for $(E'_B - E'_Y)$ a range of +0.886 to −0.886. To restore the signal excursion of the colour-difference signals to unity (i.e. +0.5 to −0.5), coefficients can be calculated as follows:

$$K_R = \frac{0.5}{0.701} = 0.713; \; K_B = \frac{0.5}{0.886} = 0.564$$

Then:

$$E'_{C_R} = 0.713\,(E'_R - E'_Y) = 0.500E'_R - 0.419E'_G - 0.081E'_B$$

and:

$$E'_{C_B} = 0.564\,(E'_B - E'_Y) = -0.169E'_R - 0.331E'_G + 0.500E'_B$$

where E'_{C_R} and E'_{C_B} are the re-normalized red and blue colour-difference signals respectively (see Notes 1 and 2).

Note 1 – The symbols E'_{C_R} and E'_{C_B} will be used only to designate re-normalized colour-difference signals, i.e. having the same nominal peak-to-peak amplitude as the luminance signal E'_Y, thus selected as the reference amplitude.

Note 2 – In the circumstances when the component signals are not normalized to a range of 1 to 0, for example, when converting from analogue component signals with unequal luminance and colour-difference amplitudes, an additional gain factor will be necessary and the gain factors K_R, K_B should be modified accordingly.

2.3 *Quantization*

In the case of a uniformly-quantized 8-bit binary encoding, 2^8, i.e. 256, equally spaced quantization levels are specified, so that the range of the binary numbers available is from 0000 0000 to 1111 1111 (00 to FF in hexadecimal notation), the equivalent decimal numbers being 0 to 255, inclusive.

In the case of the 4 : 2 : 2 system described in this Recommendation, levels 0 and 255 are reserved for synchronization data, while levels 1 to 254 are available for video.

Given that the luminance signal is to occupy only 220 levels, to provide working margins, and that black is to be at level 16, the decimal value of the luminance signal, $\overline{Y}$, prior to quantization, is:

$$\overline{Y} = 219\,(E'_Y) + 16,$$

and the corresponding level number after quantization is the nearest integer value.

Similarly, given that the colour-difference signals are to occupy 225 levels and that the zero level is to be level 128, the decimal values of the colour-difference signals, $\overline{C}_R$ and $\overline{C}_B$, prior to quantization are:

$$\overline{C}_R = 224\,[0.713\,(E'_R - E'_Y)] + 128$$

and:

$$\overline{C}_B = 224\,[0.564\,(E'_B - E'_Y)] + 128$$

which simplify to the following:

$$\overline{C}_R = 160\,(E'_R - E'_Y)] + 128$$

and:

$$\overline{C}_B = 126\,(E'_S - E'_Y)] + 128$$

and the corresponding level number, after quantization, is the nearest integer value.

The digital equivalents are termed Y, C_R and C_B.

2.4 *Construction of* Y, C_R, C_B *via quantization of* E'_R, E'_G, E'_B

In the case where the components are derived directly from the gamma pre-corrected component signals E'_R, E'_G, E'_B, or directly generated in digital form, then the quantization and encoding shall be equivalent to:

$$E'_{R_D}\text{ (in digital form)} = \text{int}\,(219\,E'_R) + 16$$

$$E'_{G_D}\text{ (in digital form)} = \text{int}\,(219\,E'_G) + 16$$

$$E'_{B_D}\text{ (in digital form)} = \text{int}\,(219\,E'_B) + 16$$

Then:

$$Y = \frac{77}{256}\,E'_{R_D} + \frac{150}{256}\,E'_{G_D} + \frac{29}{256}\,E'_{B_D}$$

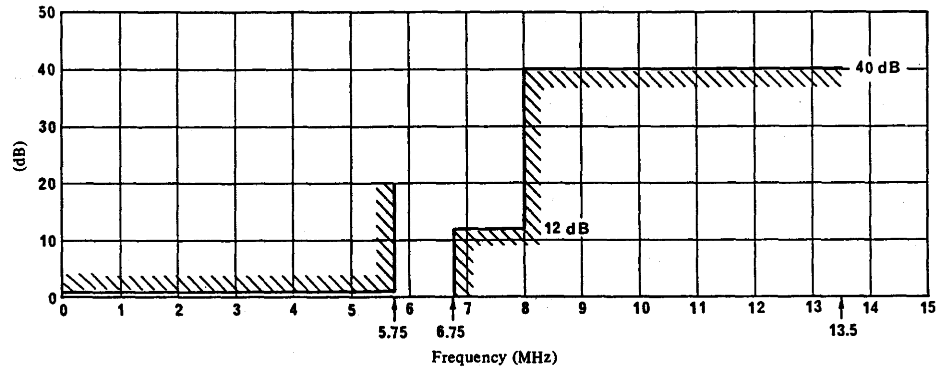
$$C_R = \frac{131}{256}\,E'_{R_D} - \frac{110}{256}\,E'_{G_D} - \frac{21}{256}\,E'_{B_D} + 128$$

$$C_B = -\frac{44}{256}\,E'_{R_D} - \frac{87}{256}\,E'_{G_D} + \frac{131}{256}\,E'_{B_D} + 128$$

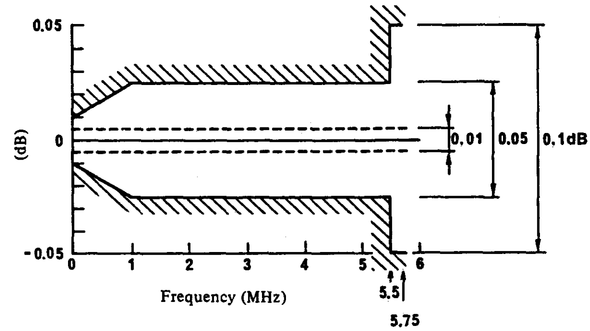
taking the nearest integer coefficients, base 256. To obtain the 4 : 2 : 2 components Y, C_R, C_B, low-pass filtering and sub-sampling must be performed on the 4 : 4 : 4 C_R, C_B signals described above. Note should be taken that slight differences could exist between C_R, C_B components derived in this way and those derived by analogue filtering prior to sampling.

ANNEX III

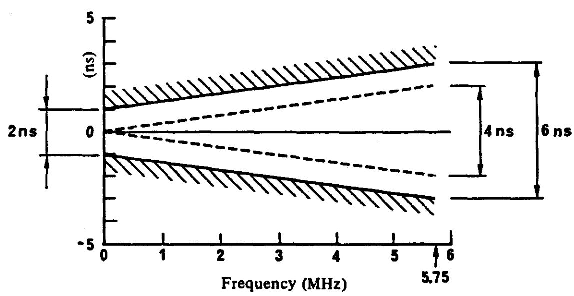
FILTERING CHARACTERISTICS



a) Template for insertion loss/frequency characteristic



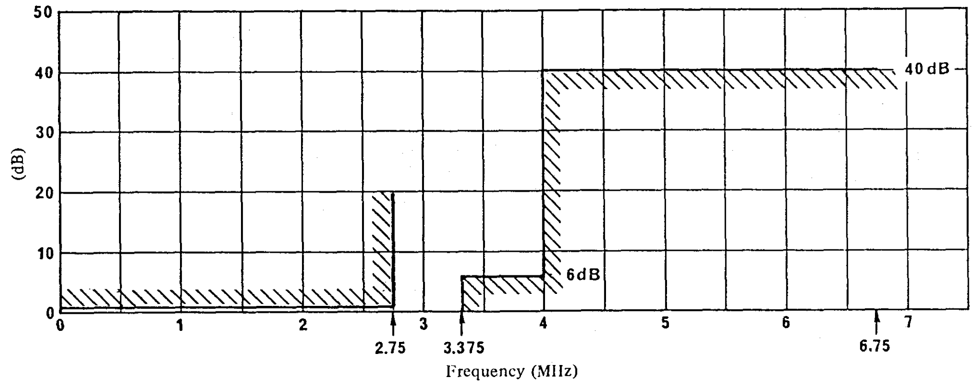
b) Passband ripple tolerance



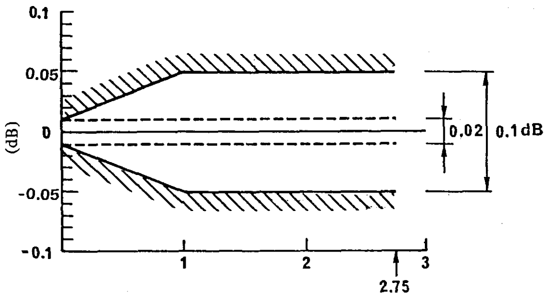
c) Passband group-delay tolerance

FIGURE 1 – *Specification for a luminance or RGB signal filter used when sampling at 13.5 MHz*

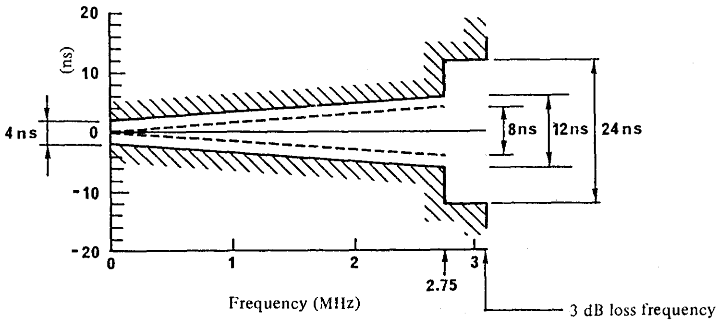
Note – The lowest indicated values in *b)* and *c)* are for 1 kHz (instead of 0 MHz).



a) Template for insertion loss/frequency characteristic



b) Passband ripple tolerance

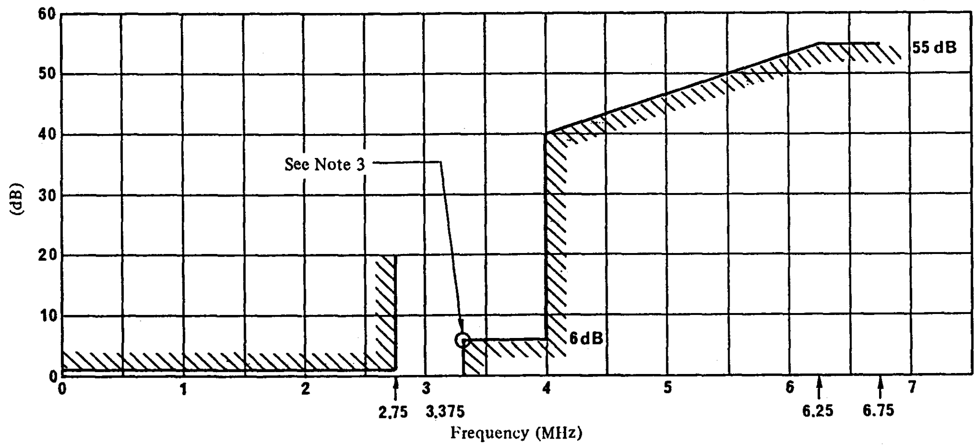


c) Passband group-delay tolerance

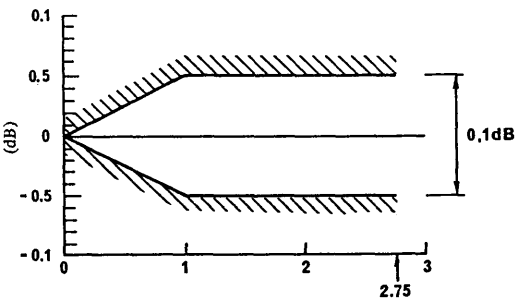
FIGURE 2 – *Specification for a colour-difference signal filter used when sampling at 6.75 MHz*

Note – The lowest indicated values in *b)* and *c)* are for 1 kHz (instead of 0 MHz).

Encoding parameters of digital television for studios — CCIR REC. 601-2



a) Template for insertion loss/frequency characteristic



b) Passband ripple tolerance

FIGURE 3 – *Specification for a digital filter for sampling-rate conversion from 4 : 4 : 4 to 4 : 2 : 2 colour-difference signals*

Notes to Figs. 1, 2 and 3:

Note 1 – Ripple and group delay are specified relative to their values at 1 kHz. The full lines are practical limits and the dashed lines give suggested limits for the theoretical design.

Note 2 – In the digital filter, the practical and design limits are the same. The delay distortion is zero, by design.

Note 3 – In the digital filter (Fig. 3), the amplitude/frequency characteristic (on linear scales) should be skew-symmetrical about the half-amplitude point, which is indicated on the figure.

Note 4 – In the proposals for the filters used in the encoding and decoding processes, it has been assumed that, in the post-filters which follow digital-to-analogue conversion, correction for the (sin x/x) characteristic of the sample-and-hold circuits is provided.

RECOMMENDATIONS OF THE CCIR, 1990 CCIR 656

(ALSO RESOLUTIONS AND OPINIONS) VOLUME XI — PART 1
BROADCASTING SERVICE (TELEVISION)

CCIR

1. The International Radio Consultative Committee (CCIR) is the permanent organ of the International Telecommunication Union responsible under the International Telecommunication Convention "...to study technical and operating questions relating specifically to radiocommunications without limit of frequency range, and to issue recommendations on them..." (International Telecommunication Convention, Nairobi 1982, First Part, Chapter I, Art. 11, No. 83).[1]
2. The objectives of the CCIR are in particular:

a. to provide the technical bases for use by administrative radio conferences and radiocommunication services for efficient utilization of the radio-frequency spectrum and the geostationary-satellite orbit, bearing in mind the needs of the various radio services;

b. to recommend performance standards for radio systems and technical arrangements which assure their effective and compatible interworking in international telecommunications;

c. to collect, exchange, analyze and disseminate technical information resulting from studies by the CCIR, and other information available, for the development, planning and operation of radio systems, including any necessary special measures required to facilitate the use of such information in developing countries.

1. See also the Constitution of the ITU, Nice, 1989, Chapter 1, Art. 11, No. 84.

Rec. 656

RECOMMENDATION 656

INTERFACES FOR DIGITAL COMPONENT VIDEO SIGNALS IN 525-LINE AND 625-LINE TELEVISION SYSTEMS

(1986)

The CCIR,

CONSIDERING

a. that there are clear advantages for television broadcasting organizations and programme producers in digital studio standards which have the greatest number of significant parameter values common to 525-line and 625-line systems;

b. that a world-wide compatible digital approach will permit the development of equipment with many common features, permit operating economies and facilitate the international exchange of programmes;

c. that to implement the above objectives, agreement has been reached on the fundamental encoding parameters of digital television for studios in the form of Recommendation 601;

d. that the practical implementation of Recommendation 601 requires definition of details of interfaces and the data streams traversing them;

e. that such interfaces should have a maximum of commonality between 525-line and 625-line versions;

f. that in the practical implementation of Recommendation 601 it is desirable that interfaces be defined in both serial and parallel forms;

g. that digital television signals produced by these interfaces may be a potential source of interference to other services, and due notice must be taken of No. 964 of the Radio Regulations,

UNANIMOUSLY RECOMMENDS

that where interfaces are required for component-coded digital video signals in television studios, the interfaces and the data streams that will traverse them should be in accordance with the following description, defining both bit-parallel and bit-serial implementations.

1. Introduction

This Recommendation describes the means of interconnecting digital television equipment operating on the 525-line or 625-line standards and complying with the 4 : 2 : 2 encoding parameters as defined in Recommendation 601.

Part I describes the signal format common to both interfaces.

Part II describes the particular characteristics of the bit-parallel interface.

Part III describes the particular characteristics of the bit-serial interface.

PART I

COMMON SIGNAL FORMAT OF THE INTERFACES

1. General description of the interfaces

The interfaces provide a unidirectional interconnection between a single source and a single destination.

A signal format common to both parallel and serial interfaces is described in § 2 below.

Rec. 656

The data signal are in the form of binary information coded in 8-bit words. These signals are:

- video data;
- timing reference codes;
- ancillary data;
- identification codes.

2. Video data

2.1 *Coding characteristics*

The video data is in compliance with Recommendation 601, and with the field-blanking definition shown in Table 1.

TABLE I — *Field interval definitions*

			625	525
V-digital field blanking				
	Field 1	Finish (V = 0)	Line 624	Line 1
		Start (V = 1)	Line 23	Line 10
	Field 2	Start (V = 1)	Line 311	Line 264
		Finish (V = 0)	Line 336	Line 273
F-digital field identification				
	Field 1	F = 0	Line 1	Line 4
	Field 2	F = 1	Line 313	Line 266

Note 1 — Signals F and V change state synchronously with the end of active video timing reference code at the beginning of the digital line.

Note 2 — Definition of line numbers is to be found in Report 624. Note that digital line number changes state prior to 0_H as shown in Fig. 1.

2.2 *Video data format*

The data words 0 and 255 (00 and FF in hexadecimal notation) are reserved for data identification purposes and consequently only 254 of the possible 256 words may be used to express a signal value.

The video data words are conveyed as a 27 Mwords/s multiplex in the following order:

C_B, Y, C_R, Y, C_B, Y, C_R, etc.

where the word sequence C_B, Y, C_R, refers to co-sited luminance and colour-difference samples and the following word, Y, corresponds to the next luminance sample.

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2.3 *Timing relationship between video data and the analogue synchronizing waveform*

2.3.1 Line interval

The digital active line begins at 244 words (in the 525-line standard) or at 264 words (in the 625-line standard) after the leading edge of the analogue line synchronization pulse, this time being specified between half-amplitude points.

Figure 1 shows the timing relationship between video and the analogue line synchronization.

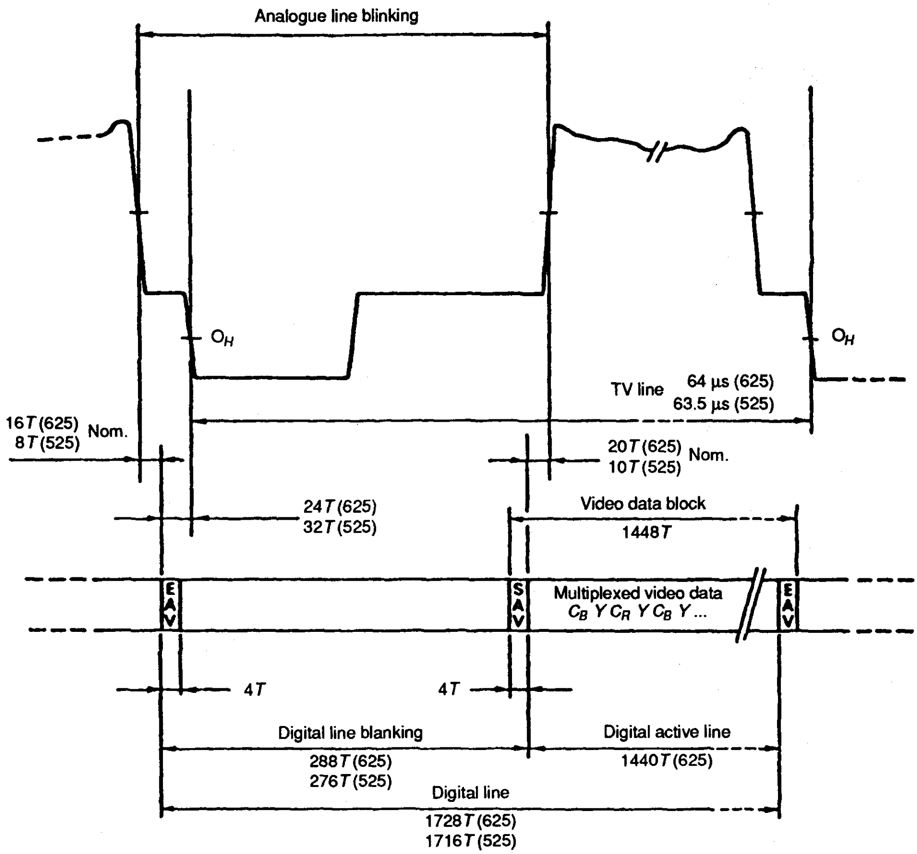

FIGURE 1 – *Data format and timing relationship with the analogue video signal*

T: clock period 37 ns nom.
SAV: start of active video timing reference code
EAV: end of active video timing reference code

2.3.2 *Field interval*

The start of the digital field is fixed by the position specified for the start of the digital line: the digital field starts 32 words (in the 525-line systems) and 24 words (in the 625-line systems) prior to the lines indicated in Table I.

2.4 *Video timing reference codes (SAV, EAV)*

There are two timing reference codes, one at the beginning of each video data block (Start of Active Video, SAV) and one at the end of each video data block (End of Active Video, EAV) as shown in Fig. 1.

Each timing reference code consists of a four word sequence in the following format: FF 00 00 XY. (Values are expressed in hexadecimal notation. Codes FF, 00 are reserved for use in timing reference codes.) The first three words are a fixed preamble. The fourth word contains information defining field 2 identification, the state of field blanking, and the state of line blanking. The assignment of bits within the timing reference code is shown below in Table II.

TABLE II — *Video timing reference codes*

Word	Bit No.							
	7 (MSB)	6	5	4	3	2	1	0 (MSB)
First	1	1	1	1	1	1	1	1
Second	0	0	0	0	0	0	0	0
Third	0	0	0	0	0	0	0	0
Fourth	1	F	V	H	P_3	P_2	P_1	P_0

F = 0 during field 1
1 during field 2

V = 0 elsewhere
1 during field blanking

H = 0 in SAV
1 in EAV

P_0, P_1, P_2, P_3 : protection bits (see Table III).
MSB: most significant bit
LSB: least significant bit

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Table I defines the state of the V and F bits.

Bits P_0, P_1, P_2, P_3, have states dependent on the states of the bits F, V and H as shown in Table III. At the receiver this arrangement permits one-bit errors to be corrected and two-bit errors to be detected.

TABLE III — *Protection bits*

Bit No.	7	6	5	4	3	2	1	0
Function	Fixed 1	F	V	H	P_3	P_2	P_1	P_0
0	1	0	0	0	0	0	0	0
1	1	0	0	1	1	1	0	1
2	1	0	1	0	1	0	1	1
3	1	0	1	1	0	1	1	0
4	1	1	0	0	0	1	1	1
5	1	1	0	1	1	0	1	0
6	1	1	1	0	1	1	0	0
7	1	1	1	1	0	0	0	1

2.5 *Ancillary data*

Provision is made for ancillary data to be inserted synchronously into the multiplex during the blanking intervals at a rate of 27 Mwords/s. Such data is conveyed by one or more 7-bit words, each with an additional parity bit (LSB) giving odd parity.

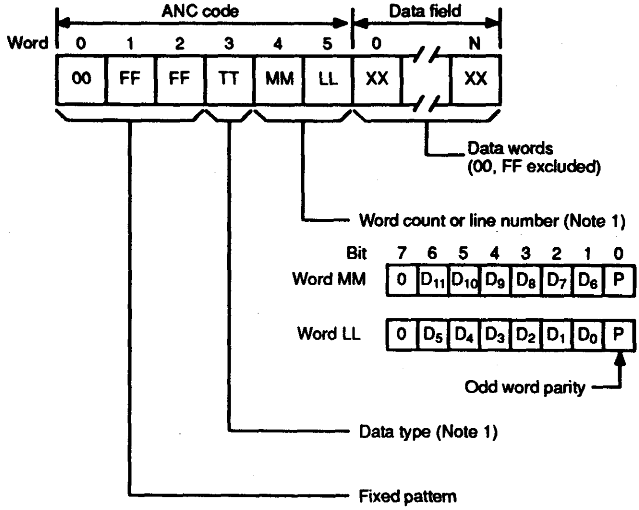
Each ancillary data block, when used, should be constructed as shown in Table IV from the timing reference code ANC and a data field.

2.6 *Data words during blanking*

The data words occurring during digital blanking intervals that are not used for the timing reference code ANC or for ancillary data are filled with the sequence 80, 10, 80, 10, etc. (values are expressed in hexadecimal notation) corresponding to the blanking level of the C_B, Y, C_R, Y signals respectively, appropriately placed in the multiplexed data.

Rec. 656

TABLE IV — *Ancillary data block*



"Word count" specifies the length of the data field and lies in the range 1 to 1434. If word TT specifies a line number then D_{11} to D_0 contain the binary equivalent of the line number and the word count is assumed to be zero. The ancillary data block(s) may be transmitted when time is available during horizontal or vertical blanking following the EAV timing reference signal.

Note 1 — The precise location of the ancillary data blocks and the coding of words 3, 4 and 5 require further study.

PART II

BIT-PARALLEL INTERFACE

1. General description of the interface

The bits of the digital code words that describe the video signal are transmitted in parallel by means of eight conductor pairs, where each carries a multiplexed stream of bits (of the same significance) of each of the component signals, C_B, Y, C_R, Y. The eight pairs also carry ancillary data that is time-multiplexed into the data stream during video blanking intervals. A ninth pair provides a synchronous clock at 27MHz.

The signals on the interface are transmitted using balanced conductor pairs. Cable lengths of up to 50 m (≅ 160 feet) without equalization and up to 200 m (≅ 650 feet) with appropriate equalization (see § 6) may be employed.

The interconnection employs a twenty-five pin D-subminiature connector equipped with a locking mechanism (see § 5).

For convenience, the eight bits of the data word are assigned the names DATA 0 to DATA 7. The entire word is designated as DATA (0-7). DATA 7 is the most significant bit.

Video data is transmitted in NRZ form in real time (unbuffered) in blocks, each comprising one active television line.

2. Data signal format

The interface carries data in the form of 8 parallel data bits and a separate synchronous clock. Data is coded in NRZ form. The recommended data format is described in Part I.

3. Clock signal

3.1 *General*

The clock signal is a 27 MHz square wave where the 0-1 transition represents the data transfer time. This signal has the following characteristics:

Width: 18.5 ± 3 ns

Jitter: Less than 3 ns from the average period over one field.

3.2 *Clock-to-data timing relationship*

The positive transition of the clock signal shall occur midway between data transitions as shown in Fig. 2.

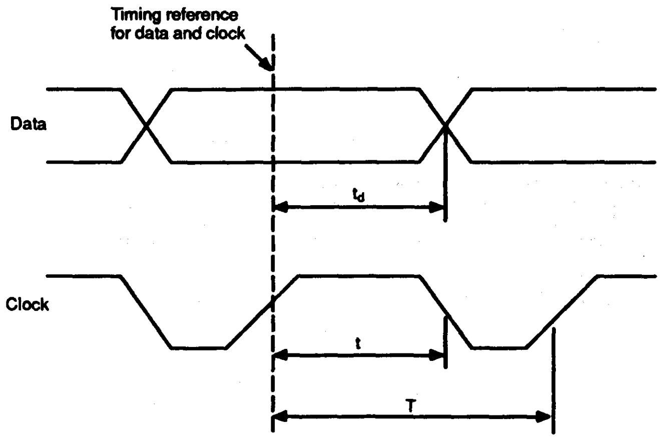


FIGURE 2 — *Clock-to-data timing (at source)*

Clock period (625):	$T = \frac{1}{1728 f_H} = 37 ns$
Clock period (525):	$T = \frac{1}{1716 f_H} = 37 ns$
Clock pulse width:	$t = 18.5 \pm 3 ns$
Data timing – sending end:	$t_d = 18.5 \pm 3 ns$

f_H: line frequency

4. Electrical characteristics of the interface

4.1 *General*

The interface employs nine line drivers and nine line receivers.

Each line driver (source) has a balanced output and the corresponding line receiver (destination) a balanced input (see Fig. 3).

Although the use of ECL technology is not specified, the line driver and receiver must be ECL-compatible, i.e. they must permit the use of ECL for either drivers or receivers.

All digital signal time intervals are measured between the half-amplitude points.

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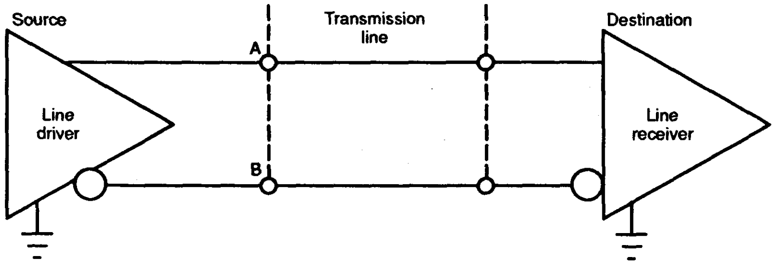

FIGURE 3 — *Line driver and line receiver interconnection*

4.2 *Logic convention*

The A terminal of the line driver is positive with respect to the B terminal for a binary 1 and a negative for a binary 0 (see Fig. 3).

4.3 *Line driver characteristics* (source)

4.3.1 *Output impedance:* 110 Ω maximum

4.3.2 *Common mode voltage:* –1.29 V ± 15% (both terminals relative to ground).

4.3.3 *Signal amplitude:* 0.8 to 2.0 V peak-to-peak, measured across a 110 Ω resistive load.

4.3.4 *Rise and fall times:* less than 5 ns, measured between the 30% and 80% amplitude points, with a 110 Ω resistive load. The difference between rise and fall times must not exceed 2 ns.

4.4 *Line receiver characteristics*

4.4.1 *Input impedance:* 110 Ω ± 10 Ω.

4.4.2 *Maximum input signal:* 2.0 V peak-to-peak.

4.4.3 *Minimum input signal:* 185 mV peak-to-peak.

However, the line receiver must sense correctly the binary data when a random data signal produces the conditions represented by the eye diagram in Fig. 4 at the data detection point.

4.4.4 *Maximum common mode signal:* ± 0.5 V, comprising interference in the range 0 to 15 kHz (both terminals to ground).

4.4.5 *Differential delay:* Data must be correctly sensed when the clock-to-data differential delay is in the range between ± 11 ns (see Fig. 4).

5. Mechanical details of the connector

The interface uses the 25 contact type D subminiature connector specified in ISO Document 2110-1980, with contact assignment shown in Table V.

Connectors are locked together by a one-piece slide lock on the cable connectors and locking posts on the equipment connectors. Connectors employ pin contacts and equipment connectors employ socket contacts. Shielding of the interconnecting cable and its connectors must be employed (see Note).

Note — It should be noted that the ninth and eighteenth harmonics of the 13.5 MHz sampling frequency (nominal value) specified in Recommendation 601 fall at the 121.5 and 243 MHz aeronautical emergency channels. Appropriate precautions must therefore be taken in the design ad operation of interfaces to ensure that no interference is caused at these frequencies. Emission levels for related equipment are given in CISPR Recommendation: "Information technology equipment – limits of interference and measuring methods" Document CISPR/B (Central Office) 16. Nevertheless, No. 964 of the Radio Regulations prohibits any harmful interference on the emergency frequencies.

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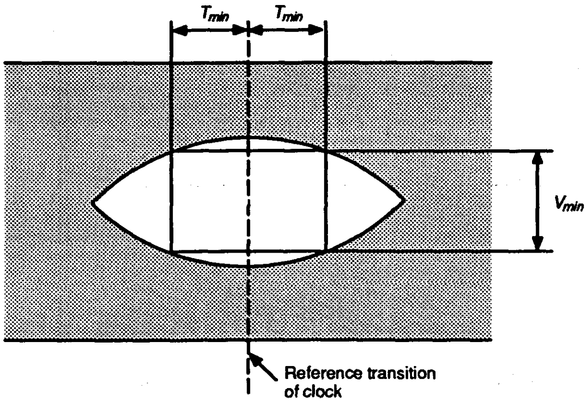


FIGURE 4 — *Idealized eye diagram corresponding to the minimum input signal level*

T_{min} = 11 ns

V_{min} = 100 mV

Note — The width of the window in the eye diagram, within which data must be correctly detected comprises ±3 ns clock jitter, ±3 ns data timing (see § 3.2), and ±5 ns available for differences in delay between pairs of the cable.

TABLE V — *Contact assignments*

Contact	Signal line	Contact	Signal line
1	Clock A	14	Clock B
2	System ground	15	System ground
3	Data 7A (MSB)	16	Data 7B
4	Data 6A	17	Data 6B
5	Data 5A	18	Data 5B
6	Data 4A	19	Data 4B
7	Data 3A	20	Data 3B
8	Data 2A	21	Data 2B
9	Data 1A	22	Data 1B
10	Data 0A	23	Data 0B
11	Spare A-A	24	Spare A-B
12	Spare B-A	25	Spare B-B
13	Cable shield	—	—

Any spare pairs connected to contacts 11,24 or 12,25 are reserved for bits of lower significance than those carried on contacts 10,23.

6. Line receiver equalization

To permit correct operation with longer interconnection links, the line receiver may incorporate equalization.

When equalization is used, it should conform to the nominal characteristics of Fig. 5. This characteristic permits operation with a range of cable lengths down to zero. The line receiver must satisfy the maximum input signal condition of § 4.4

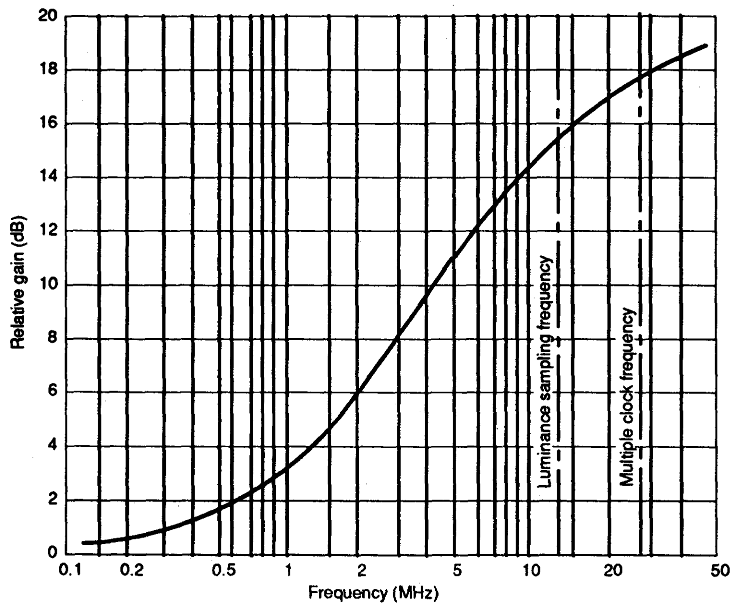


FIGURE 5 — *Line receiver equalization characteristic for small signals*

PART III

BIT-SERIAL INTERFACE

1. General description of the interface

The multiplexed data stream of 8-bit words (as described in Part I) is transmitted over a single channel in bit-serial form. Prior to transmission, additional coding takes place to provide spectral shaping, word synchronization and to facilitate clock recovery.

2. Coding

The 8-bit data words are encoded for transmission into 9-bit words as shown in Table VI.

For some 8-bit data words alternative 9-bit transmission words exist, as shown in columns 9B and $\overline{9B}$, each 9-bit word being the complement of the other. In such cases, the 9-bit word will be selected alternately from columns 9B and $\overline{9B}$ on each successive occasion that *any* such 8-bit word is conveyed. In the decoder, either word must be converted to the corresponding 8-bit data word.

Rec. 656

TABLE VI — *Encoding table*

Input	Output		Input	Output		Input	Output		Input	Output		Input	Output		Input	Output	
8B	9B	$\overline{9B}$	8B	9B	$\overline{9B}$	8B	9B	$\overline{9B}$	8B	9B	$\overline{9B}$	8B	9B	$\overline{9B}$	8B	$\overline{9B}$	$\overline{9B}$
00	0FE	101	2B	053		56	097		81	0AA		AC	12C		D7	0CC	
01	027		2C	1AC		57	168		82	055		AD	0D9		D8	139	
02	1D8		2D	057		58	099		83	1AA		AE	126		D9	0CE	
03	033		2E	1A8		59	166		84	0D5		AF	0E5		DA	133	
04	1CC		2F	059		5A	09B		85	12A		B0	11A		DB	0D8	
05	037		30	1A6		5B	164		86	095		B1	0E9		DC	131	
06	1CB		31	05B		5C	09D		87	16A		B2	116		DD	0DC	
07	039		32	05D		5D	162		88	0B5		B3	02E		DE	127	
08	1C6		33	1A4		5E	0A3		89	14A		B4	1D1		DF	0E2	
09	03B		34	065		5F	15C		8A	09A		B5	036		E0	123	
0A	1C4		35	19A		60	0A7		8B	165		B6	1C9		E1	0E4	
0B	03D		36	069		61	158		8C	0A6		B7	03A		E2	11D	
0C	1C2		37	196		62	025	1DA	8D	159		B8	1C5		E3	0E6	
0D	14D		38	026	1D9	63	0A1	15E	8E	0AC		B9	04E		E4	11B	
0E	0B4		39	08C	173	64	029	1D6	8F	153		BA	1B1		E5	0E8	
0F	14B		3A	02C	1D3	65	091	16E	90	0AE		BB	05C		E6	119	
10	1A2		3B	098	167	66	045	1BA	91	151		BC	1A3		E7	0EC	
11	0B6		3C	032	1CD	67	089	176	92	02A	1D5	BD	05E		E8	117	
12	149		3D	0BE	141	68	049	1B6	93	092	16D	BE	1A1		E9	0F2	
13	0BA		3E	034	1CB	69	085	17A	94	04A	1B5	BF	066		EA	113	
14	145		3F	0C2	13D	6A	051	1AE	95	094	16B	C0	199		EB	0F4	
15	0CA		40	046	1B9	6B	08A	175	96	0A8	157	C1	06C		EC	10D	
16	135		41	0C4	13B	6C	0A4	15B	97	0B7	148	C2	193		ED	076	
17	0D2		42	04C	1B3	6D	054	1AB	98	0F5	10A	C3	06E		EE	10B	
18	12D		43	0C8	137	6E	0A2	15D	99	0BB	144	C4	191		EF	0C7	
19	0D4		44	058	1A7	6F	052	1AD	9A	0ED	112	C5	072		F0	13C	
1A	129		45	0B1		70	056		9B	0BD	142	C6	18D		F1	047	
1B	0D6		46	14E		71	1A9		9C	0EB	114	C7	074		F2	1B8	
1C	125		47	0B3		72	05A		9D	0D7	128	C8	18B		F3	067	
1D	0DA		48	14C		73	1A5		9E	0DD	122	C9	07A		F4	19C	
1E	115		49	0B9		74	06A		9F	0DB	124	CA	189		F5	071	
1F	0EA		4A	06B		75	195		A0	146		CB	08E		F6	198	
20	0B2		4B	194		76	096		A1	0C5		CC	185		F7	073	
21	02B		4C	06D		77	169		A2	13A		CD	09C		F8	18E	
22	1D4		4D	192		78	0A9		A3	0C9		CE	171		F9	079	
23	02D		4E	075		79	156		A4	136		CF	09E		FA	18C	
24	1D2		4F	18A		7A	0AB		A5	0CB		D0	163		FB	087	
25	035		50	08B		7B	154		A6	134		D1	0B8		FC	186	
26	1CA		51	174		7C	0A5		A7	0CD		D2	161		FD	0C3	
27	04B		52	08D		7D	15A		A8	132		D3	0BC		FE	178	
28	1B4		53	172		7E	0AD		A9	0D1		D4	147		FF	062	19D
29	04D		54	093		7F	152		AA	12E		D5	0C6				
2A	1B2		55	16C		80	155		AB	0D3		D6	143				

3. Order of transmission

The least significant bit of each 9-bit word shall be transmitted first.

4. Logic convention

The signal is conveyed in NRZ form. The voltage at the output terminal of the line driver shall increase on a transition from 0 to 1 (positive logic).

5. Transmission medium

The bit-serial data stream can be conveyed using either a coaxial cable (§ 6) or fibre optic bearer (§ 7).

6. Characteristics of the electrical interface

6.1 *Line driver characteristics* (source)

6.1.1 Output impedance

The line driver has an unbalanced output with a source impedance of 75 Ω and a return loss of at least 15 dB over a frequency range of 10 to 243 MHz.

6.1.2 Signal impedance

The peak-to-peak signal amplitude lies between 400 mV and 700 mV measured across a 75 Ω resistive load directly connected to the output terminals without any transmission line.

6.1.3 DC offset

The DC offset with reference to the mid amplitude point of the signal lies between +1.0V and –1.0 V.

6.1.4 Rise and fall times

The rise and fall times, determined between the 20% and 80% amplitude points and measured across a 75 Ω resistive load connected directly to the output terminals, shall lie between 0.75 and 1.5 ns and shall not differ by more than 0.40 ns.

6.1.5 Jitter

The timing of the rising edges of the data signal shall be within ± 0.10 ns of the average timing of rising edges, as determined over a period of one line.

6.2 *Line receiver characteristics* (destination)

6.2.1 Terminating impedance

The cable is terminated by 75 Ω with a return loss of at least 15 dB over a frequency range of 10 to 243 MHz.

6.2.2 Receiver sensitivity

The line receiver must sense correctly random binary data either when connected directly to a line driver operating at the extreme voltage limits permitted by § 6.1.2, or when connected via a cable having loss of 40 dB at 243 MHz and a loss characteristic of $1/\sqrt{f}$.

Over the range 0 to 12 dB no equalization adjustment is required; beyond this range adjustment is permitted.

6.2.3 Interference rejection

When connected directly to a line driver operating at the lower limit specified in § 6.1.2, the line receiver must correctly sense the binary data in the presence of a superimposed interfering signal at the following levels:

d.c.	± 2.5 V
Below 1 kHz:	2.5 V peak-to-peak
1 kHz to 5 MHz:	100 mV peak-to-peak
Above 5 MHz:	40 mV peak-to-peak

6.3 *Cables and connectors*

6.3.1 Cable

It is recommended that the cable chosen should meet any relevant national standards on electro-magnetic radiation.

Note — It should be noted that the ninth and eighteenth harmonics of the 13.5 MHz sampling frequency (nominal value) specified in Recommendation 601 fall at the 121.5 and 243 MHz aeronautical emergency channels. Appropriate precautions must therefore be taken in the design and operation of interfaces to ensure that no interference is caused at these frequencies. Emission levels for related equipment are given in CISPR Recommendation: "Information technology equipment – limits of interference and measuring methods" (Document CISPR/B (Central Office) 16). Nevertheless, No. 964 of the Radio Regulations prohibits any harmful interference on the emergency frequencies.

6.3.2 Characteristic impedance

The cable used shall have a nominal characteristic impedance of 75 Ω.

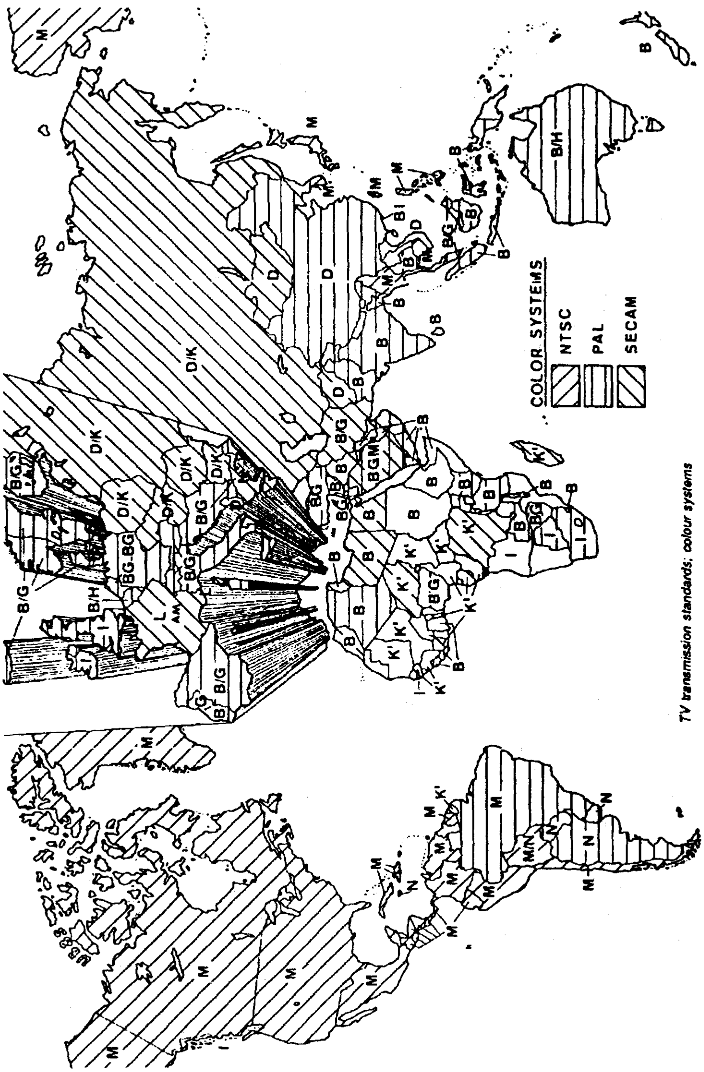
6.3.3 Connector characteristics

The connector shall have mechanical characteristics conforming to the standard BNC type (IEC Publication 169-8), and its electrical characteristics should permit it to be used at frequencies up to 500 MHz in 75 Ω circuits.

7. Characteristics

To be defined.

TV transmission standards; colour systems



TV transmission standards; colour systems

International TV systems and standards

Country	VHF	UHF	colour
A			
Afganistan	B		PAL
Albania	B		
Algeria	B	G,H	PAL
Angola	I		
Argentina	N	N	PAL
Australia	B	G	PAL
Austria	B	G	PAL
Azores	M		
B			
Bahamas	M		NTSC
Bahrain	B		PAL
Bangla-Desh	B		
Barbados	N		NTSC
Belgium	B	H	PAL
Bermuda	M		NTSC
Bolivia	N		NTSC
Brazil	M	M	PAL
Brunei	B		PAL
Bulgaria	D	K	SECAM
Burma			NTSC
C			
Cambodia	M		
Canada	M	M	NTSC
Canary Isl.	B		PAL
Centr. Afr. Rep.	B		
Chad	K1		
Chile	M	M	NTSC
China	D	K	PAL
Colombia	M	M	NTSC
Congo	D		
Costa Rica	M	M	NTSC
Cuba	M	M	NTSC
Cyprus	B	G,H	PAL
Czechoslovakia	D	K	SECAM
D			
Dahomey	K1	K1*	
Denmark	B	G	PAL
Djibouti	K1		SECAM
Dominican Rep.	M	M	NTSC
E			
Ecuador	M	M	NTSC
Egypt	B	G,H	SECAM
El Salvador	M	M	NTSC
Equatorial Guinea	B		PAL
Ethopia	B		

Country	VHF	UHF	colour
F			
Finland	B	G	PAL
France	E	L	SECAM
French Polynesia	K1		
G			
Gabon	K1		SECAM
Gambia	(K1)		
German Dem. Rep.	B	G	SECAM
German Fed. Rep.	B	G	PAL
Ghana	B		PAL
Gibraltar	B		PAL
Greece	B	G	SECAM
Greenland	M/B		NTSC/ PAL
Guadeloupe	K1		SECAM
Guatemala	M	M	NTSC
Guana (French)	K1		
H			
Haiti	M	M	NTSC
Honduras	M	M	NTSC
Hong Kong	B	I	PAL
Hungary	D	K	SECAM
I			
Iceland	B		PAL
India	B		
Indonesia	B	G	PAL
Iran	B		SECAM
Iraq	B		SECAM
Ireland	A,I	I	PAL
Israel	B	G	PAL
Italy	B	G	PAL
Ivory Coast	K1		SECAM
J			
Jamaica	M		–
Japan	M	M	NTSC
Jordan	B		PAL
K			
Kenya	B		PAL
Korea, North	D		SECAM
Korea, South	M	M	NTSC
Kuwait	B		PAL

International TV systems and standards

Country	standard for VHF	UHF	colour
L			
Lebanon	B		SECAM
Liberia	B		PAL
Libya	B		SECAM
Luxembourg	C	G,L	PAL/ SECAM
M			
Madagascar	K1		
Madeira	B		PAL
Malagasy	K1		SECAM
Malawi	B	G*	
Malaysia	B		PAL
Mali	K1	K1*	
Malta	B	H	PAL
Martinique	K1		SECAM
Maruitania	B		
Maruitius	B		SECAM
Mexico	M	M	NTSC
Monaco	E	G,L	PAL/ SECAM
Mongolia	D		
Morocco	B		SECAM
Mozambique	B		
N			
Netherlands	B	G	PAL
Neth. Antilles	M	M	NTSC
New Caledonia	K1		SECAM
New Zealand	B		PAL
Nicaragua	M	M	NTSC
Niger	K1		SECAM
Nigeria	B		PAL
Norway	B	G	PAL
O			
Oman	B	G	PAL
P			
Pakistan	B		PAL
Panama	M	M	NTSC
Paraguay	N		PAL
Peru	M	M	NTSC
Philippines	M	M	NTSC
Poland	D	K	SECAM
Portugal	B	G	PAL
Puerto Rico	M	M	NTSC
Q			
Qatar	B		PAL

Country	standard for VHF	UHF	colour
R			
Reunion	K1		SECAM
Rumania	D	D	I
S			
Sabah/Sarawak	B		PAL
St. Kitts	M	M	NTSC
Samoa	M		NTSC
Saudi Arabia	B	G	SECAM
Senegal	K1		
Sierra Leone	B		PAL
Singapore	B		PAL
South Africa	I	I	PAL
Spain	B	G	PAL
Sri Lanka	B		PAL
Sudan	B		
Surinam	M	M	NTSC
Swaziland	B	G	PAL
Sweden	B	G	PAL
Switzerland	B	G	PAL
Syria	B		SECAM
T			
Tahiti	K1		
Taiwan	M	M	NTSC
Tanzania (Zanzibar)	B	B	PAL
Thailand	B	M	PAL
Togo Rep.	K1		SECAM
Trinidad & Tobago	M	M	NTSC
Tunisia	B		SECAM
Turkey	B		(PAL)
U			
Uganda	B		PAL
United Arab Emirates	B	G	PAL
United Kingdom	A	I	PAL
Upper Volta	K1		
Uruguay	N	N	PAL
USA	M	M	NTSC
USSR	D	K	SECAM

International TV systems and standards

Country	VHF	UHF	colour
	standard for		
V			
Venezuela	M	M	NTSC
Vietnam (Khmer)	M		NTSC
Y			
Yemen (Arab Rep.)	B		PAL
Yemen (Dem. Rep.)	B		
Yugoslavia	B	H	PAL
Z			
Zaire	K1		SECAM
Zambia	B		PAL
Zimbabwe	B		

* Estimated

( ) There is no local broadcast station, but one can listen to a broadcast form a neighbouring country.

– There is no broadcast.

International TV systems and standards

BASIC CHARACTERISTICS OF VIDEO AND SYNCHRONIZING SIGNALS

Characteristics	CCIR system designation										
	A	M	N	C	B,G	H	I	D,K	K1	L	E
Number of lines per frame	405	525	625	625	625	625	625	625	625	625	819
Number of fields per second	50	60 (59.94)	50	50	50	50	50	50	50	50	50
Line frequency f_H, Hz, and tolerances	10,125	15,750 15,734 (±0.0003%)	15,625 ±0.15%	15,625 ±0.02%	15,625 ±0.02% (±0.0001%)	15,625 ±0.02% (±0.0001%)	15,625 (±0.0001%)	15,625 ±0.02% (±0.0001%)	15,625 ±0.02% (±0.0001%)	15,625 ±0.02% (±0.0001%)	20,475
Interlace ratio	2/1	2/1	2/1	2/1	2/1	2/1	2/1	2/1	2/1	2/1	2/1
Aspect ratio	4/3	4/3	4/3	4/3	4/3	4/3	4/3	4/3	4/3	4/3	4/3
Blanking level, IRE units	0	0	0	0	0	0	0	0	0	0	0
Peak-white level	100	100	100	100	100	100	100	100	100	100	100
Sync-pulse level	–43	–40	–40	–43	–43	–43	–43	–43	–43	–43	–43
Picture-black level to blanking level (setup)	0	7.5 ±2.5	7.5 ±2.5	0	0	0	0	0–7	0 color 0–7 mono	0 color 0–7 mono	0–5
Nominal video bandwidth, MHz	3	4.2	4.2	5	5	5	5.5	6	6	6	10
Assumed display gamma	2.8	2.2	2.2	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8

Notes: (1) Systems A, C, and E are not recommended by CCIR for adoption by countries setting up a new television service. (2) Values of horizontal line rate tolerances in parentheses are for color television. (3) In the systems using an assumed display gamma of 2.8, an overall system of gamma of 1.2 is assumed. All other systems assumed an overall transfer function of unity.

CCIR COLOR SYSTEMS CHARACTERISTICS (II)

Item	M/NTSC	M/PAL	B,G,H,PAL	I/PAL	B,D,G,H,K,K1,L/SECAM
Subcarrier frequency, MHz	3.579545 ± 10	3.575611.49 ± 10	4.433618.75 ± 5	4.433618.75 ± 1	f_{OR} = 4.406250 ± 2000 f_{OB} = 4.250000 ± 2000
f_{SC} multiple of f_H	$f_{SC} = \frac{455}{2} f_H$	$f_{SC} = \frac{909}{4} f_H$	$f_{SC} = \frac{1135}{4} + \frac{1}{25} f_H$		f_{OR} = 282 f_H f_{OB} = 272 f_H

Digital video evaluation module | DTV9051

7-bit digital video evaluation module featuring the SAA9051 and TDA4680 integrated circuits

THEORY OF OPERATION

The Digital Video Evaluation Board was designed to provide a compact, self-contained demonstration system for the Philips SAA9051 Digital Multistandard Color Television Decoder. The board accepts composite video (CVBS) signals or S-VHS (Y, C) signals and digitally decodes these input signals into luminance and color difference components. The digital outputs of the decoder are stored in a 6 Megabit frame memory and made available for output format conversion to analog red, green, and blue (RGB). An 87C751 microcontroller is required to send initialization information to various devices on the board.

In order to decode analog composite signals to component form, the TDA8708 8-bit A/D converter digitizes the input signal and sends the data to the SAA9051 Digital Multistandard Decoder. The digital decoder generates a 6.75 MHz clock locked to the horizontal sync of the input CVBS signal. This 6.75 MHz clock is sent to the SAA9057 clock generator for frequency multiplication to 13.5 MHz and 27 MHz. The 13.5 MHz clock from the SAA9057 is sent back to the SAA9051 and TDA8708 and used as the system clock for digitizing and output timing of the SAA9051. The FIFO memories and the SAA9060 triple 8-bit D/A converter also use the 13.5 MHz clock.

The digital data output from the SAA9051 is sent to the frame memory in a 12-bit data bus. The bus provides 8 bits form luminance and 4 bits for multiplexed chroma in a Y:U:V 4:1:1 ratio. Each field memory consists of 3 TMS4C1050 256K $\times$ 4 first-in-first-out (FIFO) memories. The field memories are always alternately read for output data but the writing, or input, to the memories can be stopped on an odd field boundary by pulling the still line to a logical LOW. A freeze frame of the input video signal is realized when a logical LOW is maintained on the still line.

After the data is read out of the frame memories, it is sent to the triple D/A converter, the SAA9060, for conversion to analog Y, R-Y, B-Y component signals. The gain of the SAA9060 is controlled via I^2C serial control of a D/A connected to bias at Pin 8. The pull-up resistors on Pins 9, 10, and 11 are required to match the analog outputs of the SAA9060 to the input levels of the TDA4680 output RGB processor.

Finally, the TDA4680 RGB processor converts the color difference component signals back to RGB. The TDA4680 has the capability to control the black level, contrast, saturation, and individual gain of each RGB output. 75 ohm buffers are added to provide low impedance outputs for RGB and sync signals. Three I^2C-controlled D/As are connected to Pins 21, 23, and 25 of the TDA4680 to allow the black level of the RGB outputs to be individually adjusted.

The SAA9051 does more than just decode composite video input signals into their color difference components. The DMSD also provides two programmable timing signals for sync and clamping in the TDA8708 A/D. It also provides blanking, horizontal sync, and vertical sync for interface to memory and output circuits. The SAA9051 maintains a close relationship between the 13.5 MHz clock and the input horizontal sync. The phase jitter of the master clock is kept in the 5 ns range. All output signals from the SAA9051 are synchronous to the 13.5 MHz clock, and have proper set-up and hold times for easy interface to various types of memory.

If S-VHS capability is required, the TDA8709 A/D can be used to digitize the chroma portion of the input signal. The luminance signal must still be applied to the TDA8708 for digitizing and sync processing. The TDA8708 contains a three channel input multiplexer, AGC circuit, and black level clamp.

Another feature of this demonstration board is the absence of any chrominance or luminance delay lines. No mechanical adjustments are required. All parameters for color decoding and level setting can be made by microprocessor control. The SAA9051 can decode seven variations of PAL and NTSC formats and maintain vertical, horizontal, and color lock even in VCR shuttle or scan mode.

The 26-pin connector provides all digital and timing information on the output side of memory.

With minor modification, this evaluation board can be upgraded to accept the SAA7151 Digital Multistandard Decoder.

DESIGN CONSIDERATIONS

A single 10 to 12-volt power supply was chosen to provide the simplest power supply connection. Most of the board uses 5 volt power. Therefore, the 5 volt power regulator dissipates about as much power as the rest of the board. the TDA4680 and TDA8444 are connected to the 8 volt power regulator. Analog +5V and digital +5V are isolated with 100µH inductors and bypassed at each active component. Special attention is paid to the data converter analog supply and clock generator circuit. The SAA9057 clock generator also has a bulk 220µF capacitor on analog supply to remove any low frequency ripple. A separate 5-volt regulator for this IC and the analog supply for the digital decoder will keep clock jitter well below 10 nS relative to input sync.

Since the sample clock frequency of this system is 13.5MHz, it is important to take care in grounding in order to keep clock noise away from analog video inputs. A common ground plane is suggested for the data converters, SAA9051, and SAA9057. Other ground planes can be used for the output section and for any logic or memory requirement, but careful design should allow for one common ground connection point for all ground planes.

Another source of noise is clock feedthrough into the data converters. A resistor is normally placed in series with the clock line to slow down the fast rise and fall times. Stray capacitance of the wiring and input pins of the data converters will aid in reducing the high frequency energy coupled into analog circuits.

On the output side, noise can be easily coupled from digital data lines feeding the SAA9060 D/A converter to the analog output pins of this device. Careful trace layout is required in order to minimize clock or data interference.

I²C COMMUNICATIONS

A Philips Semiconductors–Signetics 87C751 microprocessor is supplied to send power-up information to the SAA9051, TDA8444, and TDA4680. Normally, roughly one second after power is supplied to the board, 20 data bytes are sent to various slave devices. This message will not support multi-master I²C protocol. Therefore, any connection to the I²C bus connection jack if forbidden unless it is in the high inactive state for clock and data.

If an external computer of CPU is used for I²C control, data transmission can safely begin three seconds after board power-up. By this time the 87C751 CPU has completed sending the power-up instruction sequence, and has entered a halt-inactive state.

Implementation of automatic broadcast standard detection would require ongoing I²C communication between the SAA9051 and the on-board CPU. This can be seen as activity on the clock and data lines of the I²C connector, making external control or testing of the board impossible. In this case, the 87C751 should be removed from the board to allow external I²C control of the digital decoder and analog functions.

Philips has made available I²C control software for hardware development and debug of I²C products. This software runs under MS-DOS, and uses a parallel printer port as an I/O connector. This software has user-friendly menus for various I²C devices as well as a universal message generator menu for control of any I²C device.

OUTPUT VIDEO BUFFERS

Most analog RGB monitor connections require 75 ohm source terminated, 1 volt peak-to-peak video signals. The RGB output connectors meet this requirement, but the analog output levels can be adjusted in the TDA4680 to about 6dB from the nominal 1 volt peak-to-peak standard. Sync is not supplied on the RGB lines.

Looking at the supplied schematic, you should note the 10 ohm resistors in the collector leads of the output transistors. These resistors are required to keep high frequency video signals off of the 5V power supply lines and reduce power dissipation in the output transistors. These output buffers are not power-efficient, but do provide a simple 75 ohm output stage and DC output level at ground during blanking time.

GENERATION OF THE SAND-CASTLE SIGNAL

A very simple resistor and diode circuit is used to generate the sandcastle signal required by the TDA 4680 for proper operation. Unfortunately, the SAA9060 has a 22 clock pipeline delay from data input to analog output. The same BLN signal from the SAA9051 is used for the SAA9060 and sandcastle, so there will be a slight loss of picture information on the right side of the screen in this implementation. Because monitors are typically overscanned, this shouldn't cause a visible effect. A delay of the BLN signal would be required to eliminate this loss of picture information.

MEMORY INTERFACE AND FIELD ID GENERATION

This demonstration board contains 2 fields of memory organized as 256K × 12 bits each. Normal video signals are interlaced with even and odd fields. A D flip-flop can be clocked by vertical sync from the DMSD, and BLN can be used to determine and even or odd field by connecting it to the data input of the same flip-flop. This works well for standard signals.

The Field ID is used only as a reset for a divide-by-two flip-flop from vertical sync. In this way, if there is not a good field interlace, the field memories will still be written to on an alternate basis.

Only active picture information is stored in memory. The BLN signal is used to store 720 picture elements for each scan line. Each field memory has enough storage even for PAL video signals.

A digital data bus connector is provided on the output side of the memory for expansion to 8-bit 4:1:1 digital output format. The memories are rated for 30ns clock maximum. Therefore, the memory could be read out at rates higher than 13.5MHz if modifications were made to the board.

SYSTEM IMPROVEMENTS

There are several areas in the design of this board which can be improved if necessary.

The software for the microprocessor can be easily expanded to include automatic detection of broadcast standard by the SAA9051. Only about 10% of the 2KB ROM is currently used for board set-up.

This board is double-sided. If a ground plane were added, the system signal-to-noise ratio would be improved.

To improve stability of color and black level, an external circuit feeding RGB signals back into the TDA4680 dark current input is suggested. The external circuit required about six extra transistors and is not necessary for many applications. The TDA4680 application diagrams show this implementation.

PC BOARD LAYOUT CONSIDER-ATIONS

The Philips DeskTop Video ICs are designed for lowest radiated and conducted noise performance. The high noise performance can only be achieved if great care is taken with the PC board layout. The layout should be optimized for lowest noise on the IC's analog and digital power and ground lines.

A good decoupling with minimized interconnection length between the decoupling capacitors and the corresponding IC pins is important for low inductive ringing.

Analog and Digital Ground Planes

The DeskTop Video ICs with analog and digital circuits, such as A/D converter, color decoder, clock generator and D/A converter should have two separate ground planes. The lowest noise in the content of the digital data stream and a minimum uncertainty of clock jitter can be achieved on most of the PC boards by connecting both ground planes near the clock generator (SAA9057A, SAA7157, or SAA7197).

Analog and Digital Power Sup-plies

The impedance of the power supply lines should be as low as possible. In order to provide EMI suppression in series to the analog supply pins of the ICs, a ferrite bead or, better, a ferrite EMI suppressor should be connected.

Supply Decoupling

Decoupling capacitors can further reduce the noise on the power supply lines. For optimum performance, a 100nF multilayer ceramic capacitor should be placed as close as possible to every supply pin of the ICs and should be connected to the corresponding digital or analog ground plane. This is needed especially for the analog supply Pins 4 and 5 at the clock generator. In addition to the multilayer ceramic capacitors, a 5–10μF electrolytic capacitor should be placed near each IC.

Analog Signal Lines

The analog part of the board design should be isolated as much as possible from the digital signal and clock lines.

Optimum performance is achieved by overlaying the analog components with the analog ground plane.

The video signal lines at the A/D converter TDA8708 and TDA8709 from Pin 19 to Pin 20 should be as short as possible to minimize noise pickup.

I²C VALUES

The following values are loaded into the I²C-addressable components at power-up. This corresponds to video input #1, NTSC, NTSC matrix, 1 volt peak-to-peak output.

SAA9051	TDA8444	TDA4680
Slave Address 8AH	Slave Address 40H	Slave Address 88H
64H Reg 00	26H Reg 00	2AH Reg 00
35H	26H	13H
0AH	1EH	33H
f8H	00H	22H
CAH	00H	34H
FEH	23H	34H
29H	3FH	34H
00H	3FH	20H
77H		20H
E0H		20H
40H		3FH Reg 0AH
00H		89H Reg 0CH
		10H Reg 0DH

NOTE:
TDA4680 register 0BH is omitted. The TDA4670 responds to this subaddress only.

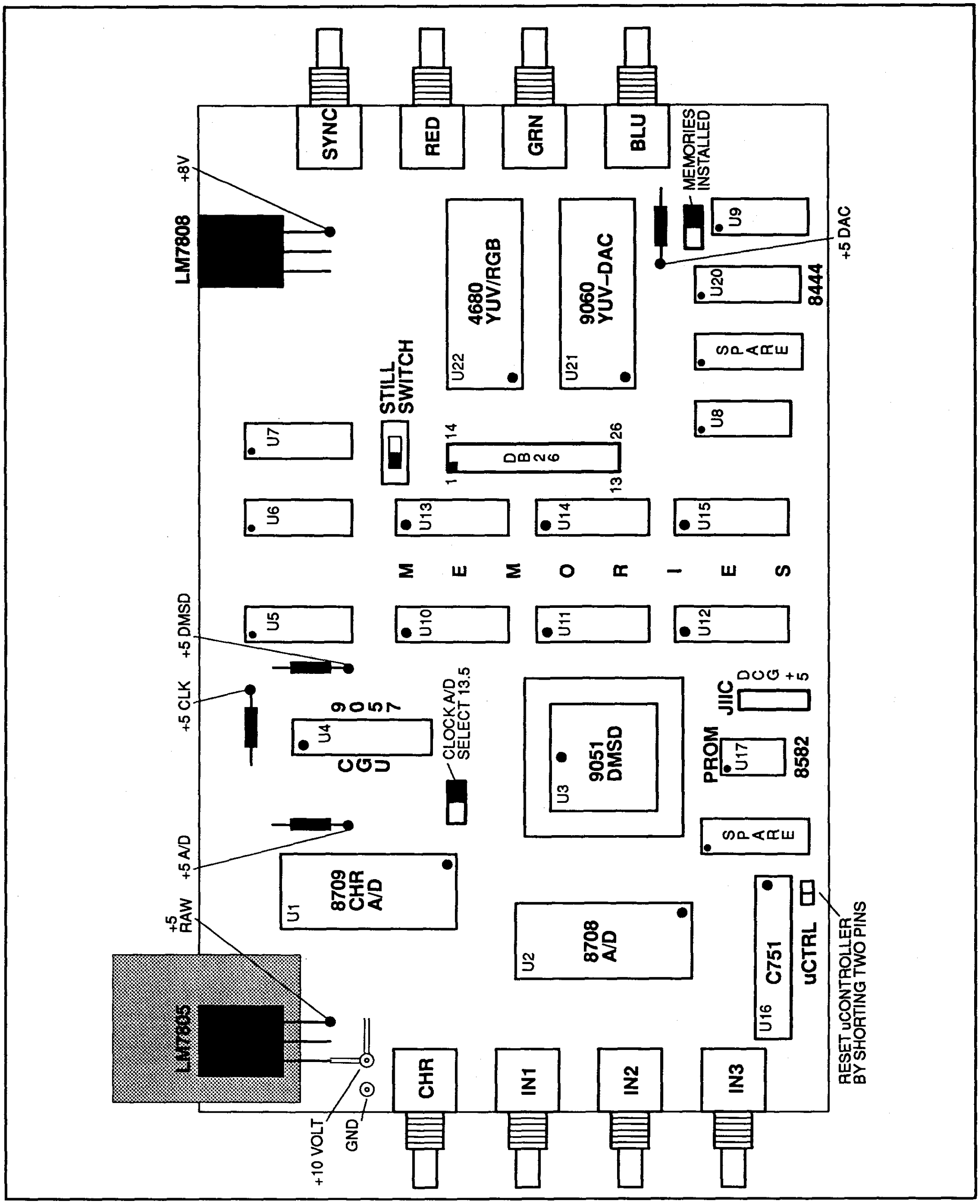
CONCLUSION

This digital multistandard decoder board provides a means of evaluating the performance of the Philips digital television system, and of quickly prototyping your application. The digital video system delivers a robust, flexible, and cost-effective solution for digitizing video images.

Digital video evaluation module

DTV9051

PHILIPS SEMICONDUCTORS–SIGNETICS DMSD2 DEMO BOARD REV B



PHILIPS DMSD2 DEMO BOARD PARTS LIST (Revised May 10, 1991)

ITEM	QUANTITY	REFERENCE	PART
1	8	J-Y/C CHROMA1, J-BLU 1, J-GREEN1, J-IN1, J-RED1, J-SYNC1, J-IN2, J-IN3	BNC
2	8	R1, R2, R3, R4, R5, R6, R7, R8	75
3	1	S1	SW SPDT
4	2	R46, R47	6.8K
5	1	C5	0.22
6	7	R11, R10, R12, R21, R48, R49, R50	10K
7	1	JP2	10 volt in
8	1	J-IIC1	4 PIN
9	1	P1	DB26
10	1	JP1	BLANK JUMP
11	5	C1, C2, C3, C4, C39	3.3/16V
12	1	VR1	LM7805
13	1	VR2	LM7808
14	35	C69, C6, C9, C14, C17, C22, C23, C24, C25, C26, C27, C29, C33, C34, C35, C40, C41, C42, C43, C44, C45, C58, C59, C60, C61, C62, C63, C64, C65, C66, C74, C75, C77, C81, C86	0.1
15	6	C70, C49, C50, C68, C71, C73	22/20V
16	1	C72	220/10V
17	14	C76, C28, C30, C31, C32, C46, C47, C52, C53, C54, C55, C78, C79, C80	22/16V
18	3	L5, L4, L7	100μH
19	1	L6	100μH
20	1	U1	TDA8709
21	1	U2	TDA8708
22	1	U3	SAA9051
23	1	C7	0.33
24	2	R13, R36	330
25	4	R14, R16, R18, R19	750
26	2	R15, R60	680K
27	1	Y1	24.576
28	2	L2, L3	22μH
29	2	C10, C12	30pF
30	2	C11, C13	30pF
31	1	R17	15
32	1	U4	SAA9057
33	2	R20, R39	470
34	2	JP3, JPDMSD ADD	HEADER 3
35	1	C8	1nF
36	1	L1	10μF
37	2	C15, C16	1/16V

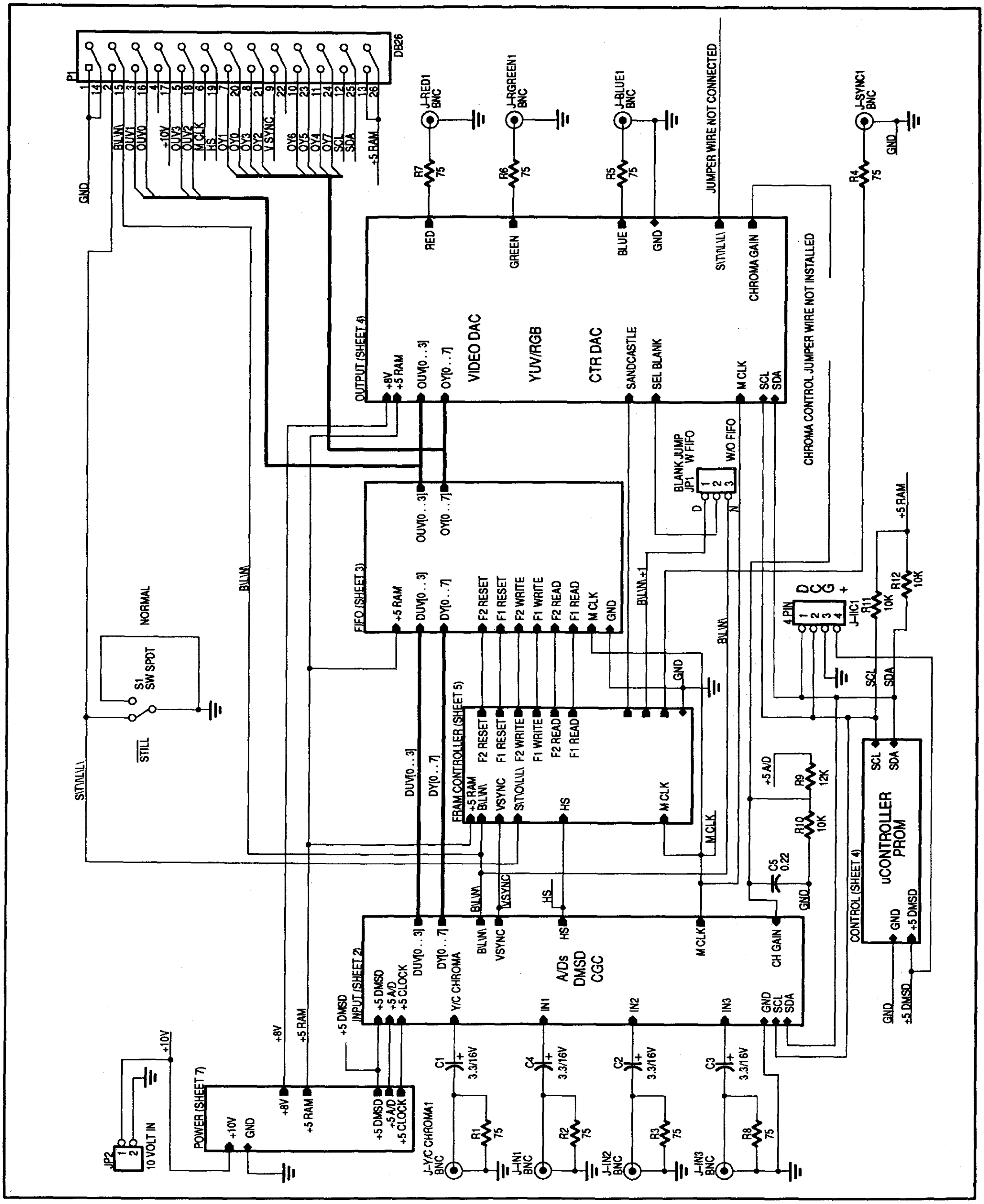
PHILIPS DMSD2 DEMO BOARD PARTS LIST (Revised May 10, 1991)

ITEM	QUANTITY	REFERENCE	PART
38	4	R26, R43, R44, R45	68
39	4	R27, R51, R52, R53	10
40	9	R28, R29, R30, R31, R32, R33, R54, R55, R56	4.7K
41	5	Q1, Q2, Q3, Q4, Q5	PN2222
42	2	C20, C21	10nF
43	5	D2, D3, D4, D5, D6	1N4148
44	3	U7, U6, U9	74HC74
45	2	U8, U5	74AHCT27
46	1	C19	33pF
47	1	R34	8.2K
48	1	R35	2.4K
49	6	U10, U11, U12, U13, U14, U15	TMS4C1050
50	1	JP5	JUMPER
51	1	R59	56K
52	1	Y20	3.5 – 12 MHz
53	1	C83	3.3nF
54	2	C85, C84	20pF
55	1	C82	15/16V
56	1	U16	S87C751–XXXX
57	1	U17	PCF8582AP
58	1	R37	560
59	1	R38	820
60	1	R40	680
61	2	R41, R42	100
62	1	C36	100pF
63	2	C37, C38	330pF
64	1	JP4	WIRE
65	1	U21	SAA9060
66	1	U22	TDA4680
67	1	U20	TDA8444
68	1	R58	82K
69	2	R57, R60	20K
70	1	R9	12K

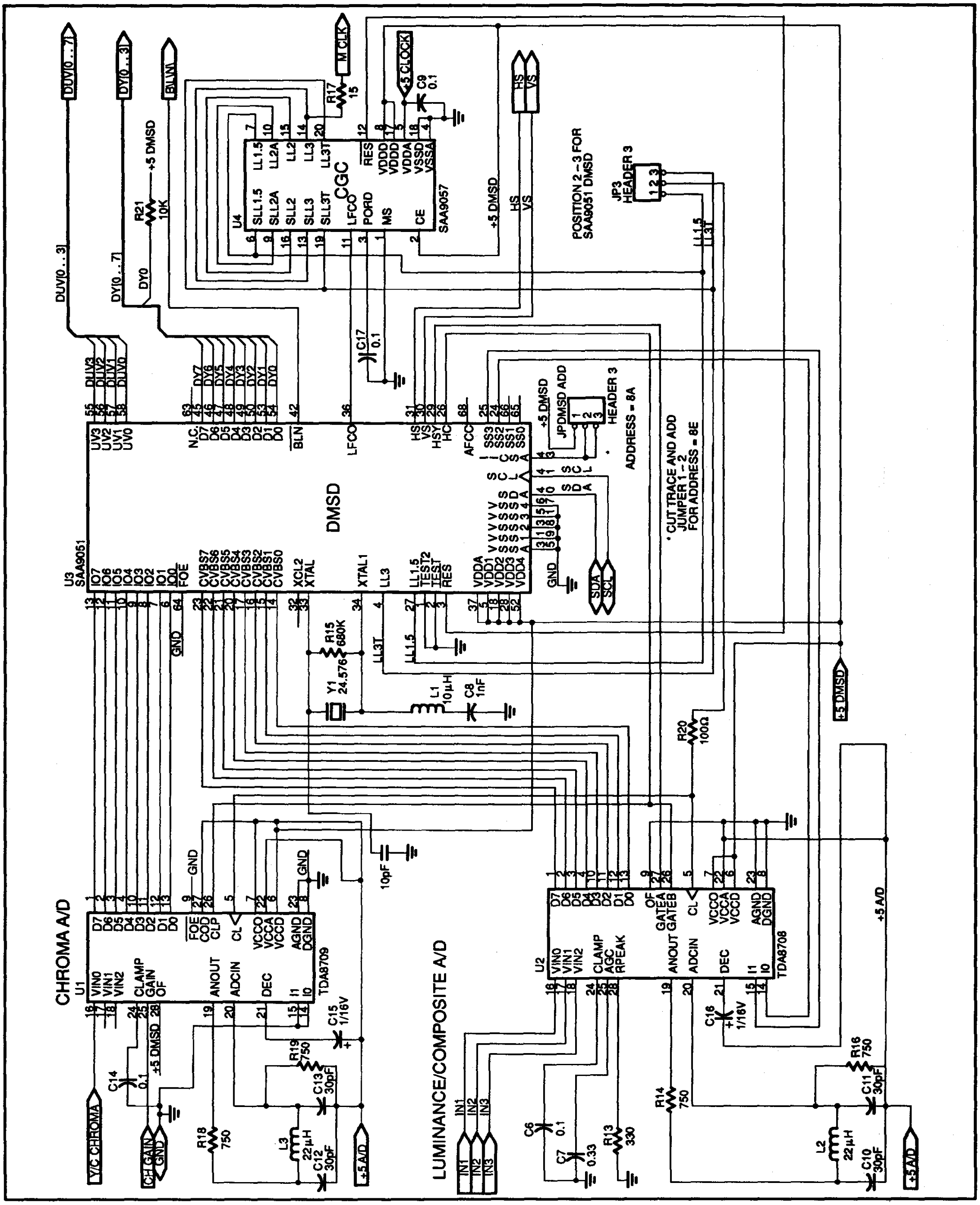
Digital video evaluation module

DTV9051

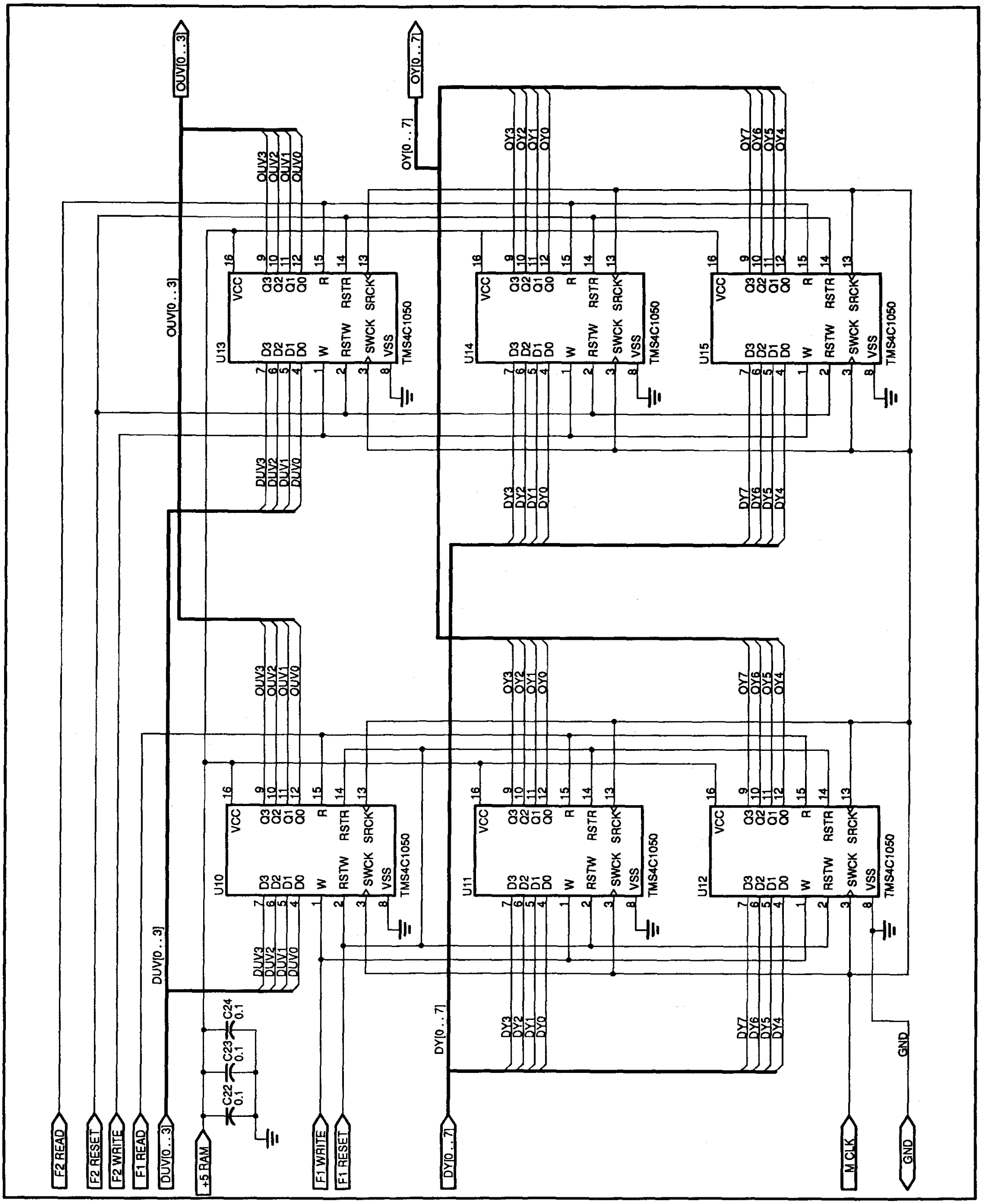
BLOCK DIAGRAM



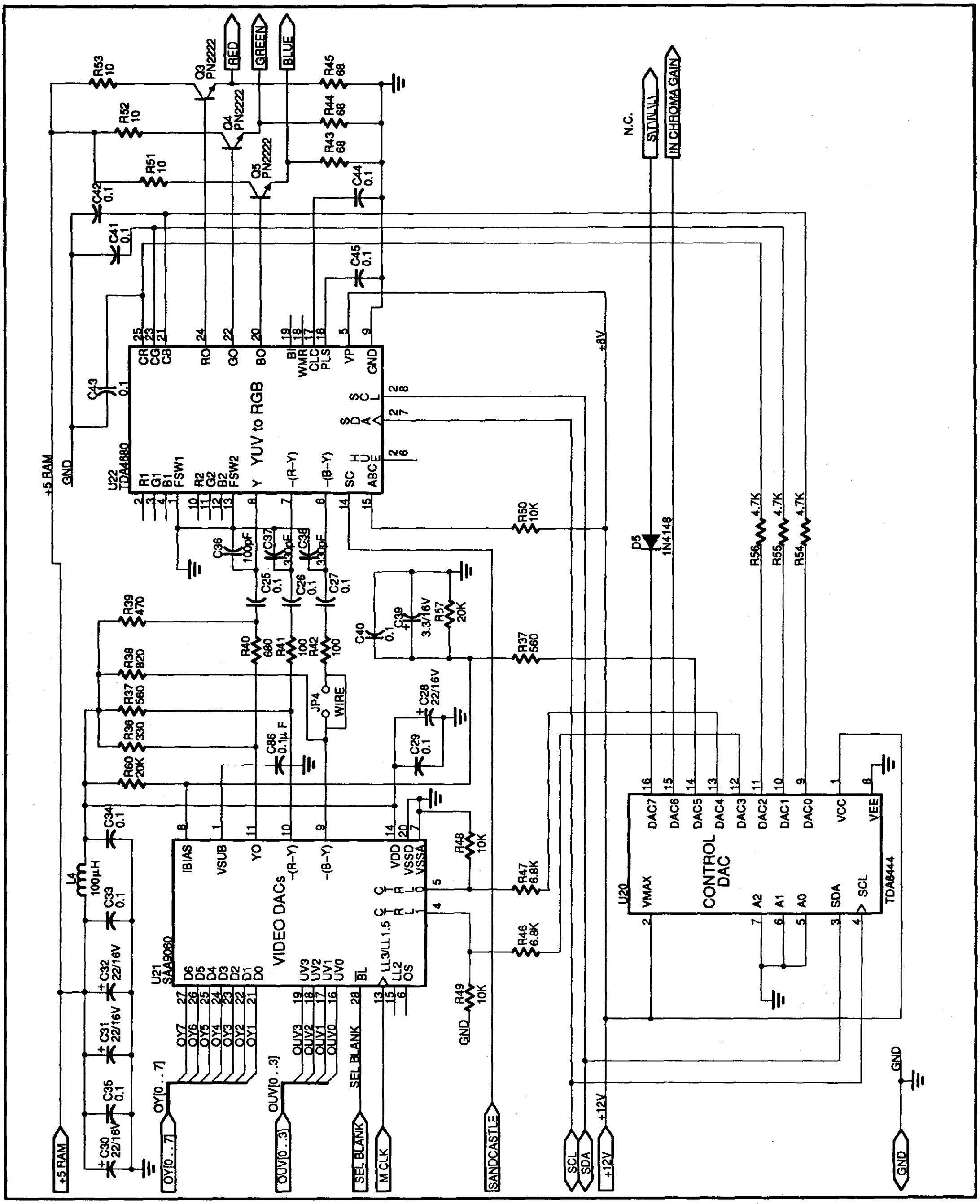
PHILIPS DMSD2 DEMO BOARD – INPUT



PHILIPS DMSD2 DEMO BOARD – FIFO

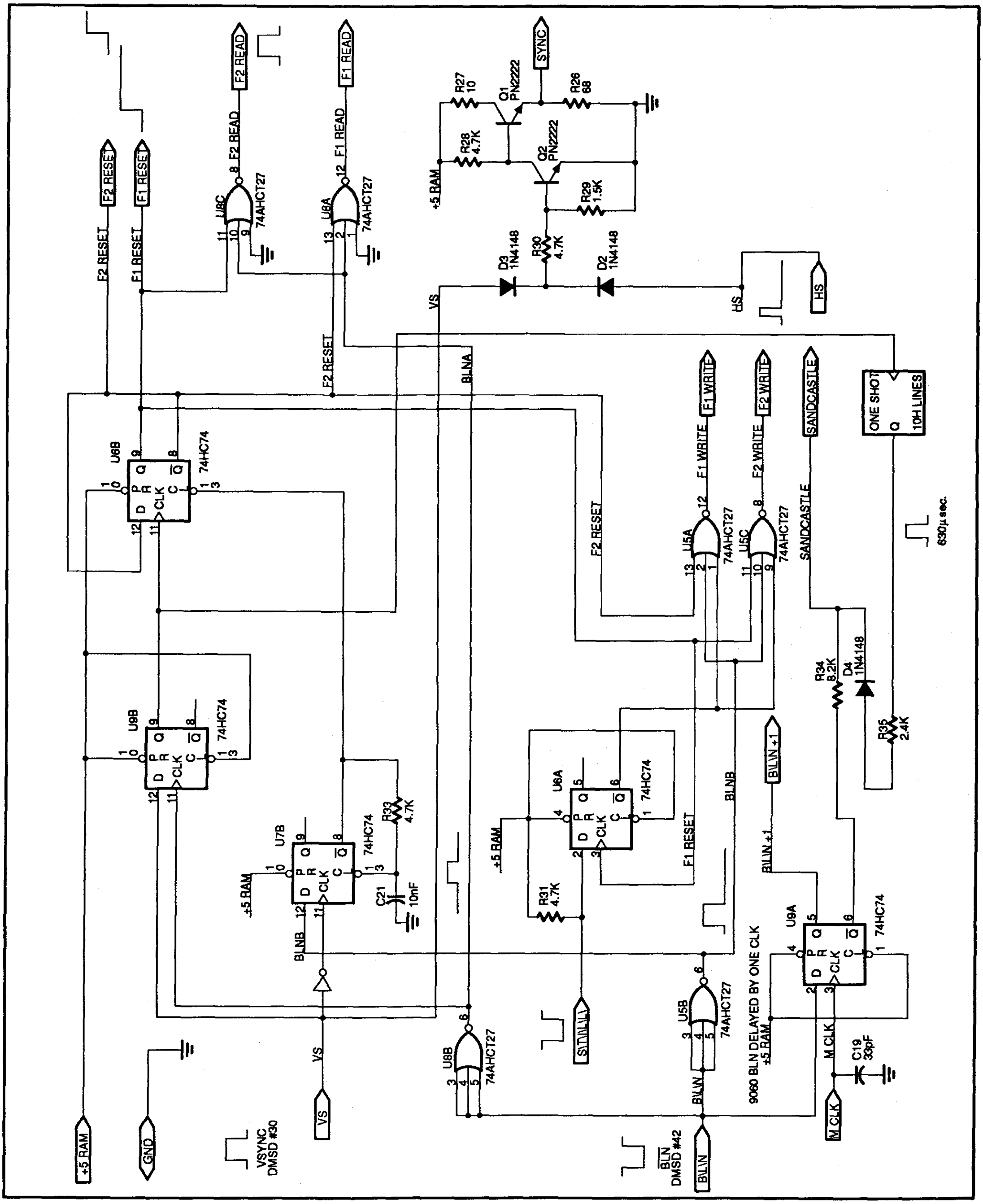


PHILIPS DMSD2 DEMO BOARD – OUTPUT

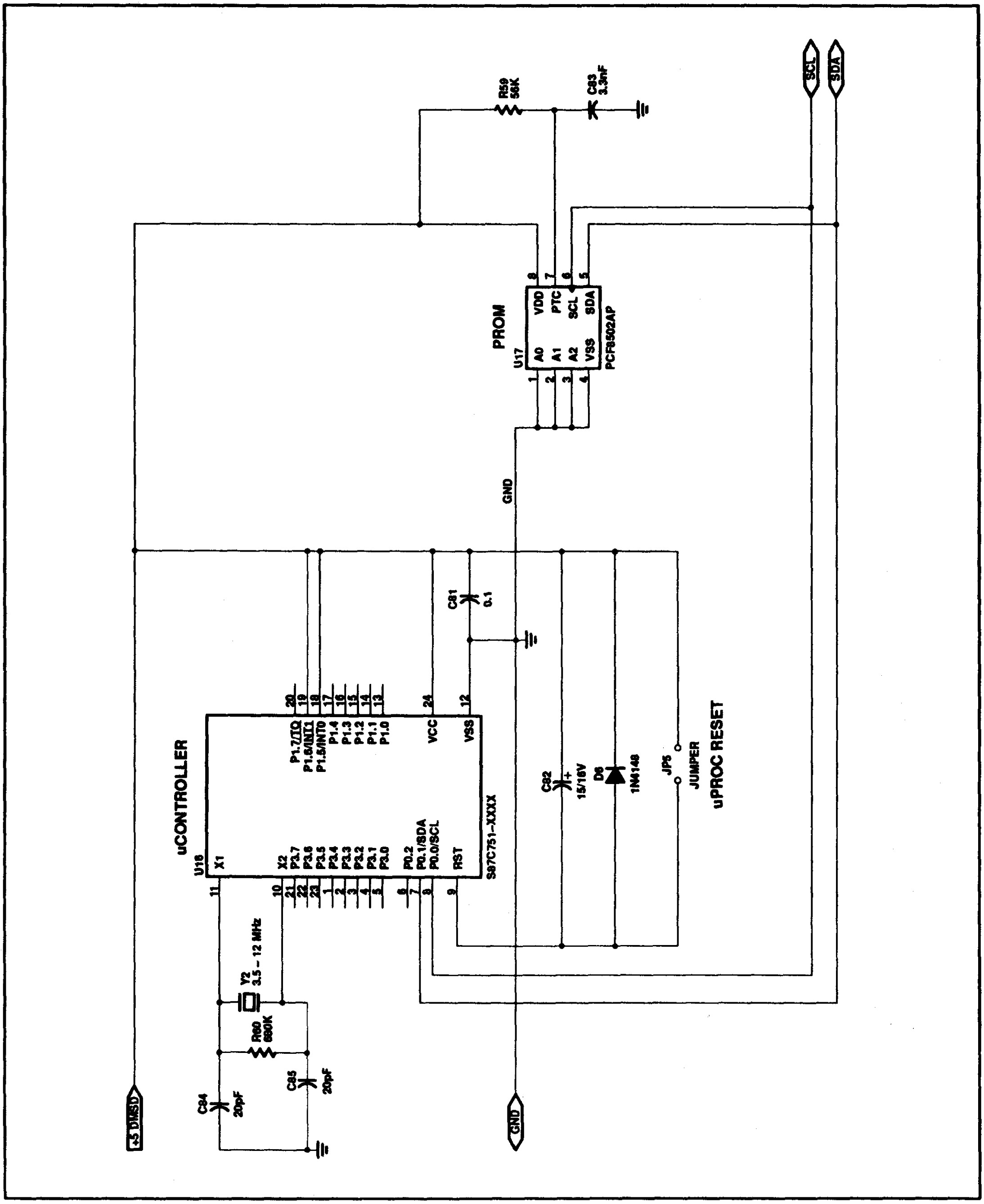


Digital video evaluation module DTV9051

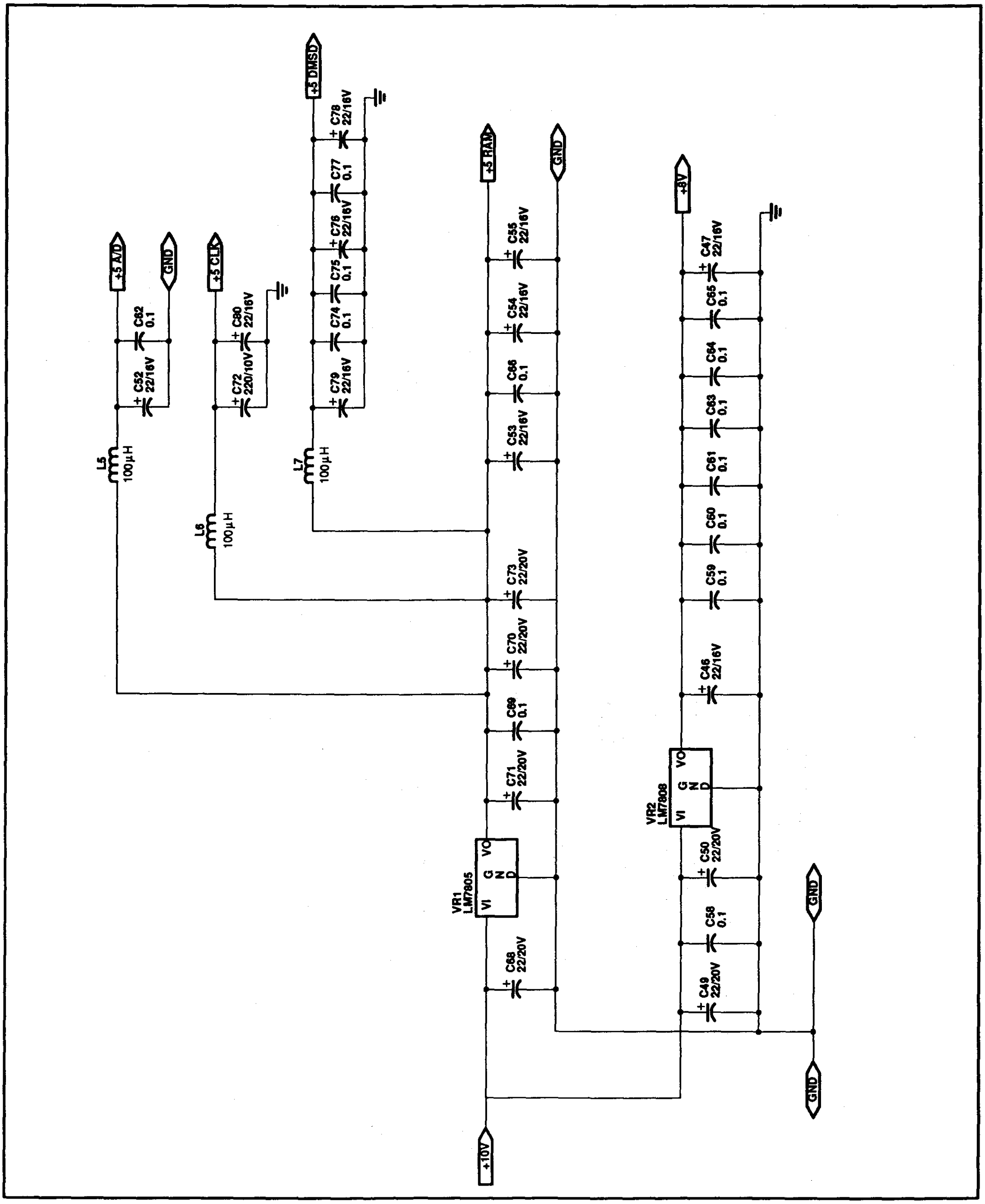
PHILIPS DMSD2 DEMO BOARD – FRAM CONTROLLER



PHILIPS DMSD2 DEMO BOARD – CONTROL



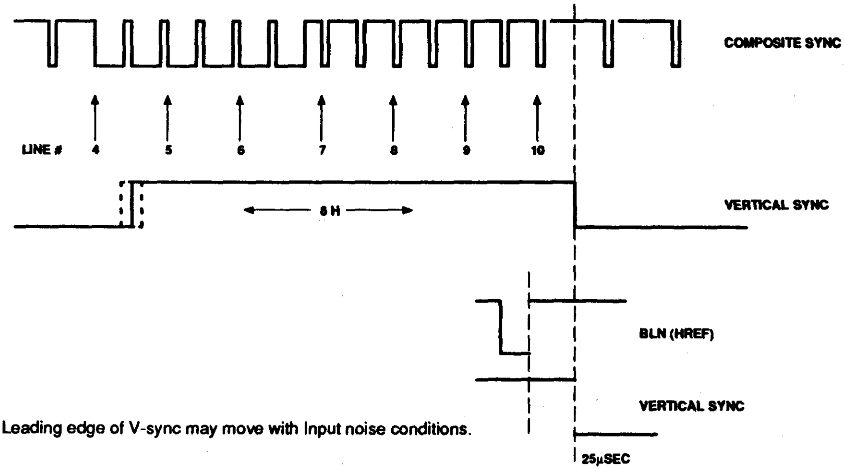
PHILIPS DMSD2 DEMO BOARD – POWER



PHILIPS SAA9051 V5.0 AND SAA7191 V1 BLANK AND SYNC TIMING

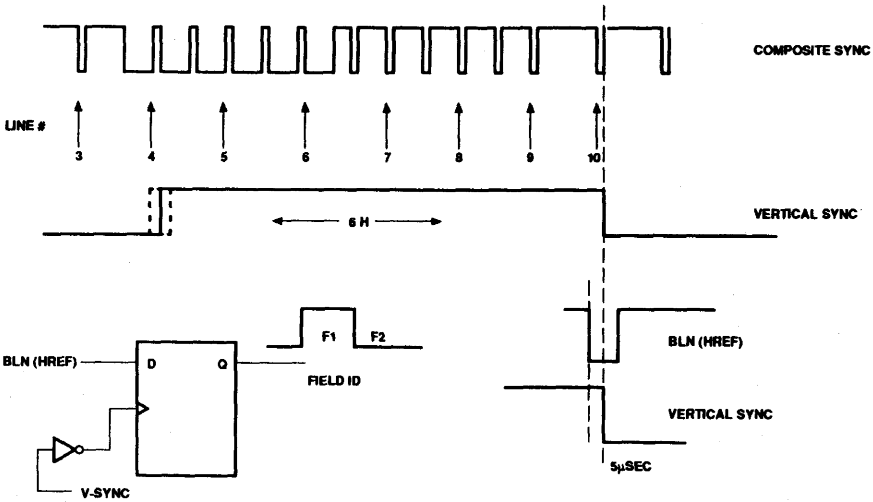
NOTE: VNL ON, VCR Mode

Field One, Odd NTSC 60Hz



NOTE: Leading edge of V-sync may move with Input noise conditions.

Field Two, Even NTSC 60Hz



DTV7199 Digital Television Demonstration System

Author: Herb Kniess

SECTION 1: OVERVIEW

The DTV7199 evaluation board provides a comprehensive means of demonstrating and evaluating the latest digital video signal processing devices from Philips Semiconductors. Color encoding and decoding is performed using a line-locked-clock system. The following ICs are featured:

TDA8708	Video A/D converter, 30MHz, 8-bit, for CVBS and Y, with analog pre-processing, clamp and gain control
TDA8709	Video A/D converter, 30MHz, 8-bit, for C of S-Video, with analog pre-processing, clamp and gain control
SAA7151B	Digital Multi Standard Decoder (DMSD), for CCIR-601 pixel raster (industrial applications)
SAA7157	Clock Generator Circuit (CGC) for SAA7191B
SAA7191	Digital Multi Standard Decoder (DMSD), for square pixel raster (graphics environment)
SAA7197	Clock Generator Circuit (CGC) for SAA7191
SAA7192A	Digital Color Space Converter (DCSC), interpolation filter, YUV to RGB matrix
SAA7169	Triple DAC, 30MHz, 9-bit in each channel
SAA7199B	Digital Encoder (DENC), GENLOCK capable, from digital YUV or RGB into analog CVBS or S-Video
S87C054	Microcontroller, 8051-based, dedicated for video control applications, with OSD, on-chip EPROM.

Analog video input is accepted in CVBS or S-Video form, in NTSC, PAL, or SECAM color standards. The video signals are digitized and sent to the digital decoder (DMSD) SAA7151B or SAA7191B for synchronization processing, line-locked-clock generation, and color decoding. The output bus of the DMSD contains digital YUV baseband information. The data is sent to a two-field frame store for buffering and time base conversion. After the frame buffer, the YUV data is converted to 24-bit RGB data in the SAA7192A color space converter. The 24-bit RGB data is fed to the SAA7169 Triple DAC for analog RGB output conversion and also to the SAA7199B digital encoder (DENC). The encoder can be programmed in various modes, such as GENLOCK so that time base correction of input signals is possible. The encoder can operate in NTSC or PAL television standards.

Various board configurations are possible by changing jumper settings and by reprogramming several of the signal processing devices. In addition, two 60-pin headers are provided to allow external connection of digital YUV data before and after the frame buffer. The MTV onboard microprocessor sends configuration data to various devices via an I^2C serial two-wire bus. A connector for the serial data is also provided to allow external computer control to the board via a DOS software package supplied with each board.

SECTION 2: INPUT VIDEO DATA CONVERSION

Input video sources can be NTSC, PAL, or SECAM world standards in Y/C or composite formats by four BNC connectors. Refer to "Input" section schematic. An S-Video or Y/C connector is provided at JSVID2 for these higher performance Y/C input signals. The Philips TDA8708 8-bit 30MHz A/D converter at location U2 is used for composite or Y signal processing. It has a three-channel multiplexer for input source selection, video clamp for DC restoration, and automatic gain control in front of the high performance 8-bit A/D converter. Input source selection is controlled via two switch signals from the SAA7191 and connected to the TDA8708 at Pins 14 and 15. The switch signals are programmed in the DMSDs via the I^2C bus.

If the higher performance Y/C input format is desired, a second data converter is required for digitizing the chrominance, or "C", half of the input signal. The TDA8709 at location U1 provides this function. Low pass filters for removing high frequency components in the analog input signals are provided between Pins 19 and 20 of both A/D converters before digitizing. Please note that the AC reference for the converters is the analog power supply. The power supplies for these devices are well decoupled since the performance of the entire system is determined at the input data converters. The digitizing clock is provided by the SAA7197 clock generator at location U3 with a rate of two times the final pixel rate for decoded signal at the output of the DMSD. The clock rate of the converters is line-loaded and can range from 24- to 30MHz depending on input television standards and the type of digital decoder used. The clock input on Pin 5 of both A/D converters is fed with a series resistor, which slows the clock slopes down in order to minimize the effect of high rise times from the clock line entering analog areas around the converter. Clamping and sync pulses coming from the decoder are fed to the A/D converters on Pins 27 and 26 to inform internal digital level detectors when to activate and make automatic adjustments of gain and black level on each scan line.

It is recommended that the input signal area and the data converters share a common ground plane for analog and digital grounds at the converters. However, it is possible to have separate ground planes and have the common point under the data converters on Pins 23 and 8. High amplitude noise between Pins 23 and 8 should be avoided. Otherwise it may cause ground loop conditions within the converters. The entire video signal is digitized in order to recover the sync and color burst information. The converters deliver 8-bit digital data in a two's complement format to the decoder input. The format selection is made by grounding Pin 9 on both converters. For other applications the A/D converters can be operated in binary format.

SECTION 3: DIGITAL COLOR DECODING

After converting analog video inputs to digital data it is the function of the Digital Multi Standard Decoder (DMSD) to provide clock information, sync, blanking and, of course, luminance and decoded color difference video data known as YUV or Y, RY, BY. Refer to the "Input" section schematic.

The output signals are all synchronized to the input video timing in frequency and phase via a clock control loop feeding from U4 DMSD on Pin 36 called Line Frequency Control Output (LFCO) to U3 SAA7197 clock generator. LFCO is internally generated via the crystal reference on Pins 33 and 34 of the DMSD and made to phase lock to incoming video sync. The frequency of LFCO is one half of the pixel clock frequency at the output of the DMSD, so the SAA7197 must multiply this synthesized frequency by 2 and 4 for the system line-locked clock. In order to close the PLL loop, the clock generators' clock outputs are fed back to the DMSD clock inputs and the A/D converters' clock inputs. The system works as a highly stable digital PLL because the DMSD calculates the clock frequency of LFCO on a line-by-line basis and in conjunction with the crystal reference maintains a constant number of clock samples for each input video scan line regardless of input signal conditions.

The DMSD also decodes the color information from video signals. The UV

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output bus contains the color information in one of several programmable industry standard formats such as CCIR 601. In CCIR 601 the output data bus is 8 bits Y of luminance and 8 bits UV time multiplexed. This is 16 bits per pixel or clock cycle. A 4:1:1 mode is also available via I^2C programming if memory cost is too high for 4:2:2 CCIR 601 mode. RAMs U8 and U9 could be removed for 4:1:1 operational mode. The DTV7199 demo board is capable for applications of the square pixel DMSD SAA7191B as well as of the CCIR-DMSD SAA7151B. Only the DMSD IC and the related reference crystal must be exchanged (see Table 2). The board layout is prepared to support both systems. Also, the MTV controller contains software to set up both ICs.

SECTION 4: MEMORY INTERFACE AND STORAGE

The 16-bit data bus from the DMSD is being clocked at rates from 12-15MHz. High speed serial RAMs were chosen to store the data without the need for memory addressing and counting chains. Refer to FIFO and MEMCON schematic. Each RAM is really a FIFO with 256k by 4 bits memory. Input and output clocks can run independently with some limiting restrictions. Four RAMs, U9, U10, U11, U12, make up a bank for field one. Four RAMs, U8, U7, U6, U5, make up the bank for field two. If memory cost is too high for 4:2:2 CCIR 601 mode, RAMs U8 and U9 could be removed for 4:1:1 operational mode. Video data from the DMSD is stored alternately in each bank. Only data during active portion of each scan line is written to the memory. Less than 75% of the RAM is used for each incoming field, even in PAL or SECAM modes.

The simple memory controller comprised of U15, U17, U19, U51, U20, U21 and U54 uses vertical sync to reset the memory pointers and horizontal blanking to stop and start reading and writing the memory. The top portion of the schematic is for writing into memory. The bottom portion is for reading from memory. Devices U15 and U54 provide timing delays to guarantee that complete fields will be stored in memory. U51B will inhibit writing to memory on frame boundaries and provide a freeze frame picture for quality analysis and special effects. Both fields will be displayed so there may be inter-field motion displayed on the monitor. The "still picture" switch activates the freeze frame with a low on U51B Pin 12. Switch S1 must be in the down position for active video. The up position is for still frame (both fields).

The DMSD generates an H_{REF} signal for enabling writing to memory. A comparable signal must be generated for reading from memory. The SAA7199B encoder does not deliver such a Horizontal Blanking, but needs to receive it. H_{REFO}, or Horizontal Blanking, is generated via counters for output video timing only by using HSYNC from DENC to trigger counters. Refer to H_{REFGEN} schematic.

The H_{REF} generator times the correct horizontal blanking interval and generates a delayed HSYNC signal for display monitor from the HSYNC from the SAA7199B encoder. U26 Pin 2 receives HSYNC from the encoder and generates a single clock reset pulse via U27 Pin 3 to reset U28 and U29 counters. The output timing diagram and clock cycles are shown. It is important only that the total number of clock cycles of H_{REFO} at U53 Pin 6 be set properly regarding display and SAA7199B timing scheme. Table 1 shows how to select the memory read blanking timing interval depending on how the board is programmed, which standard is applied and which type of decoder is installed. If there is an error between memory write format (number of pixels per line) and memory read format, there will be a horizontal error line-by-line down the screen because the line lengths are different.

HSYNCO is generated at U27 Pin 6 with a delay because of the pipeline delay through the SAA7192A color space converter. The RGB data must be in time with the RGB sync at the SAA7169 DAC outputs. Transistor Q2 provides composite sync for RGB monitors.

Data for the SAA7199B must be read from memory early to compensate the delay through the SAA7192A color space converter. The SAA7199B encoder has a programmable HSYNC for this very reason. It is not known what delay future memory or memory controllers will produce so the SAA7199B is prepared to adjust for new devices.

SECTION 5: COLOR SPACE CONVERSION AND DAC

Data from memory read operations is passed through jumper JP14 to the Digital Color Space Converter SAA7192A. Refer to SAA7192 schematic. Normally 24 jumpers are installed on the board to pass data from the memory through the connector. However, a daughter board can be added using JP3 and JP14 to multiplex YUV or RGB data at JP14. The data coming from memory must be disabled via the expansion board. Make special note of U16 Pin 5. H_{REFO} is delayed by one additional clock to compensate for the memory read delay of one clock. If this delay is not compensated for from the memory, the color space converter will not demultiplex the UV data bus correctly. U47, U48, U49 switch data on to the RGB output bus of the SAA7192A when MTV 87C054 says there is a character to display. The VCTRL signal from MTV controls which talks into the RGB data bus, either the SAA7192A or the MTV. Pin 61 of the SAA7192A tri-states its output RGB bus.

The SAA7169 DAC is wired in a standard configuration, with the low order 2 bits of all three 10-bit wide input ports grounded for 8-bit operation. RP1 and RP2 provide low order bit pull-up when the RGB data bus is switched to MTV-source in order to meet the CCIR 601 requirement of 16 for black levels. JP13 chooses two clock phases for U50. MEMRD is preferred.

SECTION 6: DIGITAL ENCODER AND GENLOCK

The SAA7191 decoder provides the memory write clocks and timing, and the SAA7199 digital encoder provides the memory read clocks and timing. These input and output clocks can be synchronous or asynchronous. The digital encoder will synchronize to any video reference input signal via U23 TDA8708 in the same manner as the SAA7191 DMSD if programmed to do so (GENLOCK mode). Refer to previous discussions on Digital Decoding. It can also run in a stable mode, by use of its crystal reference and U24 SAA7197 clock generator.

A small change in the output level of the SAA7199B DACs can be made by changing the bias on Pin 63. Linearity may be affected with large changes in bias. Key input at Pin 73 has been deactivated by pull-down resistor R45. The clock generator power supply has been well filtered at Pin 5 to guarantee minimum effects from input video timing crosstalk. Crystal selection for the SAA7199B should be made as shown in Table 2. See application note "SAA7199B Operation Modes".

SECTION 7: POWER SUPPLY GROUNDING AND LAYOUT

Clean analog power supplies are essential if the full performance of an 8-bit system is to be realized. The analog supplies on the A/D converters and the clock generator are the most sensitive. The performance of the A/D converter determines the signal-to-noise ratio of the complete system. The performance of the clock generator determines system clock

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jitter and, to some extent, the quality of the chroma demodulation.

Noise on Pins 21 and 22 of the TDA8708 A/D converter will degrade the signal-to-noise ratio of analog input signals. Please note that the low pass filter at Pins 19 and 20 has an AC reference to the analog supply on Pin 22. Therefore, noise on Pin 22 would directly be coupled to input signals being digitized.

The SAA7197 must have a clean analog supply at Pin 5 which must be directly connected to Pin 37 on the SAA7191B or SAA7151B decoders because of the close coupling of the LFCO signal between the clock generator and the decoders. Bypassing capacitors at pins of both devices is a must. Of course, all digital power inputs must be bypassed on all devices.

The DTV7199 evaluation board makes use of one other power supply isolation technique. The input and output supplies are regulated separately. This isolation guarantees minimum crosstalk between input decoding and output encoding. Small ferrite core inductors further reduce analog and digital supply crosstalk.

In many computer applications it is not possible to regulate the digital supplies because of current limits placed on higher supply voltages. In this case, only the lower current analog supplies should be regulated. Total analog supply current is under 100mA for input circuits and also under 100mA for output circuits. Because of delay differences in power supply sequencing during power up, it is suggested that 5V regulated analog supplies have parallel opposite biased diodes connected to the digital supply. This will keep both supplies in sync during power up. This is needed to perform a determined power-on reset procedure at SAA7157 and SAA7197. 1N4148 diodes will supply enough current for a short period of time and allow regulation isolation of about 600mV.

A single ground plane has been shown to be effective under input components and ICs such as the TDA8708, SAA7197 and SAA7191B. After the decoder, a digital ground plane could be used if there are a large number of digital devices and fast memory. The input ground plane could be considered analog ground. The evaluation board uses a single ground plane for the entire board. A single ground plane appears to work well for most applications.

Clock and data line routing should be kept away from analog components and analog signals. The most critical signal is LFCO between the digital decoder and the clock generator. It has an analog characteristic and may pick up unwanted digital noise. The length of the LFCO trace between these two devices must be kept to a minimum.

SECTION 8: FACTORY JUMPER CONFIGURATION

The factory jumper configuration is required for normal operation of the DTV7199 demo board when the 87C054 microcontroller has been installed. Software version 1.x will only configure the board for NTSC mode using the SAA7191 decoder with video input connected to JIN2. Any one of the push buttons can be used to switch the "Philips Digital Video" message on the screen on and off.

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Table 1: H_{REF} Length Jumper Table

12.272727	60Hz	140	SQUARE PIXELS	SAA7191
14.75	50Hz	176	SQUARE PIXELS	SAA7191
13.50	60Hz	138	CCIR 601	SAA7151B (SAA9051)
13.50	50Hz	144	CCIR 601	SAA7151B (SAA9051)

Table 2: Crystal Selection

SYSTEM	ACTIVE PIXELS	CRYSTAL	DECODER
SQUARE PIXELS	640 or 768	26.800MHz	SAA7191 decoder
CCIR 601	720	24.576MHz	SAA7151 decoder

Table 3: Factory Jumper Settings

JP3	Install all jumpers except bottom six.
JP14	Install all jumpers except bottom six.
JP2	Install jumper to left for SAA7151 (right for SAA7191).
JP20	Installed
JP5	Install jumper to the left.
JP7	Open
JP8	Open
JP6	Open. This is the microprocessor reset.
JP13	Install jumper to the right.
JP19	Open. Install jumpers only if RTC function is required.
JI^2C	This connector is for I^2C communications.
JP15	Install jumpers depending on which decoder is used. (See previous section on H_{REF} LENGTH JUMPER TABLE.)

Table 4. JP3 Functions

PINS	JP3 FUNCTIONS
1,2	DY7
3,4	DY6
5,6	DY5
7,8	DY4
9,10	DY3
11,12	DY2
13,14	DY1
15,16	DY0
17,18	DUV7
19,20	DUV6
21,22	DUV5
23,24	DUV4
25,26	DUV3
27,28	DUV2
29,30	DUV1
31,32	DUV0
33,34	LLCI
35,36	VSI
37,38	H_{REFI}
39,40	CREFI
41,42	LL3I
43,44	HSI
45,46	SDA
47,48	SCL
49,50	FEIN
51,52	RESI
53,54	
55,56	
57,58	GROUND
59,60	GROUND

Table 5. JP14 Functions

PINS	JP14 FUNCTIONS
1,2	OY7
3,4	OY6
5,6	OY5
7,8	OY4
9,10	OY3
11,12	OY2
13,14	OY1
15,16	OY0
17,18	OY7
19,20	OY6
21,22	OY5
23,24	OY4
25,26	OY3
27,28	OY2
29,30	OY1
31,32	OY0
33,34	OUV7
35,36	OUV6
37,38	OUV5
39,40	OUV4
41,42	OUV3
43,44	OUV2
45,46	OUV1
47,48	OUV0
49,50	H_{REFO}, KEY
51,52	MEMREAD, RESO
53,54	LLCO, VSYNCO
55,56	LL30, OPT2
57,58	CREFO, OPT1
59,60	GROUND

SECTION 9: DEFAULT REGISTER CONFIGURATION VALUES

For composite video input at JIN2; Decoding of NTSC into YUV 4:2:2.

NTSC – SQUARE PIXEL		
REGISTER (HEX)	SAA7191	SAA7199
00	50H	DCH
01	7FH	00H
02	53H	00H
03	43H	00H
04	19H	F0H
05	00H	2DH
06	19H	52H
07	00H	0AH
08	7FH	30H
09	7FH	00H
0A	7FH	00H
0B	7FH	00H
0C	40H	56H
0D	80H	00H
0E	79H	0CH
0F	78H	
10	00H	
11	18H	
12	00H*	
13	00H*	
14	36H	
15	0BH	
16	FEH	
17	D2H	
18	00H	

* Reserved; Program as 00H only.

NTSC – CCIR MODE		
REGISTER (HEX)	SAA7151B	SAA7199
00	66H	DCH
01	3AH	00H
02	07H	00H
03	F7H	00H
04	CBH	F0H
05	00H	2BH
06	35H	52H
07	00H	11H
08	B0H	30H
09	30H	00H
0A	7FH	00H
0B	7FH	00H
0C	24H	0FH
0D	4CH	00H
0E	30H	0DH
0F	58H	
10	60H	
11	21H	
12	C0H	

NOTE: SAA7192A is always programmed in register 0 with 2A hex.

SECTION 10: MENU CONTROLLED SOFTWARE (DVS)

The Desktop Video Software (DVS) package supports programming of the digital video ICs on the demo board DTV7199. It guides the user with a menu-controlled graphic interface, showing how to program individual functions and bits accessible by the I^2C bus. Detailed device I^2C register data can be obtained by using the "special options" function. The software runs on a PC or compatible and talks to the I^2C bus via an interface board at the parallel printer port. See application note "I^2C Parallel Printer Port Adaptor". The DVS also allows a software-only demonstration mode; neither I^2C bus interface nor device samples are required to be connected to operate this demo-mode.

This section gives a short guideline on how to get started using the Desktop Video control software for demonstration and evaluation purposes. The menu-controlled software offers a lot more features than the fundamental functions described here.

How to Use the Software-only Demonstration Mode

Required Equipment
The following equipment is required to operate the DVS software in demonstration mode:

- IBM-PC/AT compatible personal computer, with at least 384 Kbytes of system memory available
- MS-DOS or PC-DOS operating system
- preferably a color graphics adaptor and associated monitor
- floppy disk containing the DVS software and setup files

Procedure
Follow the instructions step by step to install the software and get it started:

Switch the personal computer and its monitor on. Wait for completion of self test and booting of the operation system.

Insert the floppy disk containing the Desktop Video Software into a disk drive. Change the current home drive to this drive.

You may copy the content of the DVS floppy into a dedicated directory on the hard disk. This will improve the speed for loading the program and the related utility and setup files.

Type "DVS <enter>" to start DVS. The control software will display "Philips Semiconductors" on the PC screen and perform an automatic search for installed desktop video devices and their respective I^2C addresses. Because in demonstration mode there are no such devices connected, the search will result in "not in use" noted on the screen for all devices supported by the software.

Set the devices of interest "active" by using the "+" key on the numeric keypad and the cursor up/down to move to the concerned devices.

Hit "<enter>" to finish the device activation and to proceed with the page assignment procedure. A default device-to-page assignment is offered. If you like, use the function keys to redefine the page assignment.

Hit "<enter>" to confirm the device to page assignment and to proceed.

I^2C bus check will report "not ready".

Enable demonstration mode by choosing "A" to neglect real I^2C bus operation.

Load any of the predefined settings: Press "F" to select the file selection menu, press "L" and enter a filename. "D" gives a directory of available settings.

Now you have access to all the programming parameters of the selected 'active' devices. Every device is assigned to a page number and can be selected by typing the appropriate function key. Subject to the amount of programmability for a certain IC, the page may have sub-pages called sheets, which are accessible with page up/page down.

Move the cursor up/down to select a parameter. Use "+/–" keys of the numeric keypad to change the selected parameter.

The DTV7199 Demonstration Board under Control of DVS

Required Equipment
In order to operate the Demo Board DTV7199 under DVS control the following items are required in addition to that which is mentioned for the software-only demonstration mode:

- Demo Board DTV7199
- Power supply 8V DC, 1A
- I^2C bus adapter board, to be connected to the PC's parallel printer board and associated I^2C cable
- one or two video signal sources, e.g., video test pattern generator, or a video camera, video tape recorder, etc.
- RGB monitor, capable of displaying analog RGB inputs at television frequencies of 15-16kHz horizontal and 50/60Hz vertical scan frequencies, and/or
- TV-monitor, with built-in color decoder, with 'external' CVBS or S-Video input
- cables to connect the video signal source to the board (BNC or S-Video), cables to connect the board's RGB output (BNC) to the monitor, cable to connect the encoded CVBS from the board (BNC or S-Video) to the TV monitor.

Procedure
Follow the instructions step by step to power up the system and run the software:

Connect the DTV7199 demo board with a signal source at the input BNC connector JIN2. Switch the signal source on.

Connect the RGB outputs and associated sync BNC connectors with a RGB monitor, or

Connect the encoder output CVBS-out or S-Video out with a TV monitor.

Power up the demo board with the I^2C cable *not* connected to the board. The on-board control software embedded in the MTV loads the default parameters. This requires a few seconds and then the I^2C bus is idle.

The monitor shows a picture according to the default settings.

Plug the I^2C bus adapter board into the parallel printer connector (Centronics Interface) of the personal computer. Connect the I^2C cable (gray, 4 wires) to this I^2C bus adapter board.

Switch the personal computer and its monitor on. Wait for completion of self test and booting of the operation system.

Insert the floppy disk containing the Desktop Video Software into a disk drive. Change the current home drive to this drive.

You may copy the content of the DVS floppy into a dedicated directory on the hard disk. This will improve the speed for loading the program and the related utility and setup files.

Type "DVS <enter>" to start DVS. The control software will display "Philips Semiconductors" on the PC screen and perform an automatic search for installed desktop video devices and their respective addresses. The found devices are listed with their I^2C addresses and declared as "active". If necessary, that can be changed using cursor keys and "+/–" keys.

Hit "<enter>" to confirm the device search program results as displayed and to

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proceed to the page assignment procedure. A default device-to-page assignment is offered. If you like, use the function keys to redefine the page assignment.

Hit "<enter>" to confirm the device to page assignment and to proceed.

In normal DVS operation mode the initialization is performed by selecting a predefined initialization data files.

Press "F" to select the file selection menu, press "L" and enter a filename; the file "DTV7199" is provided as default setting. Typing "D" would display a directory of available settings.

The software pre-loads all the device parameters, but the actual transmission into the I²C device registers is inhibited until the transmission is triggered by typing "T" to select the transmit option and "I" to perform the initialization.

The RGB monitor (respectively the TV monitor) should now show a picture according to the programming as loaded by the file.

Now there is access to all the programming parameters of the selected 'active' devices. Every device is assigned to a page number and can be selected by typing the appropriate function key F1, F2, etc. Subject to the amount of programmable parameters for a certain IC, the page may have sub-pages called sheets, which are accessible with page up/ page down.

Use cursor up/down to select a parameter. Use "+/–" keys of the numeric keypad to change the selected parameter. As long as transmit function is enabled, the changes of parameters are updated immediately into the device programming registers.

The results of new programming can be studied directly on the monitor screen.

Loading Look-up Tables of SAA7192A and SAA7199B

Under the programming page of the Digital Color Space Converter SAA7192A, select the "S" special option to load the Video Look-up Tables (VLUT). The sub-menu asks for a filename with the data for the contents of the VLUT. Enter "?" to see the available files or give the desired filename. All files with the extension '.VLT' are data files for VLUT.

Under the pages for the digital encoder SAA7199B one will also find a similar special option "S" sub-menu to load data into the encoders Color Look-up Tables (CLUT). The files that are provided for this purpose carry the extension '.CLT'.

The DVS floppy also contains a utility program SHOW_LUT.exe, which shows the content of VLT-files as well as CLT-files in a graphic representation. Under DOS just type "SHOW_LUT filename.CLT".

Determining I²C Register Contents

By means of DVS it is possible to determine the binary or hexadecimal values for the various programming registers for certain programming configurations. These codes can serve as reference for a specific device initialization of a dedicated system, where the programming is drawn from a ROM, PROM or other system file. The software-only demonstration mode of DVS is especially very helpful for this purpose to obtain the 'compiled' I²C register content based on the chosen parameter programming.

The SAA7192A has a single byte for I²C programming. The binary representation of the selected programming is directly displayed on that single device page.

For the digital decoders SAA7151B and SAA7191B, as well as the digital encoder SAA7199B, the "special option" is supported by pressing "S". This submenu directly displays the table of the I²C registers, displaying the content in binary as well as in hexadecimal representation. For the encoder this table is in the sub-sub-menu Read the section on Registers.

Please note that these tables do not include the I²C address and the subaddress/index data required to program the ICs. Refer to the respective data sheets for the exact data protocols for initialization of each device.

Saving of device and board program settings

It is possible to store the device settings as a data file for use in future sessions. The program saves the settings of all devices in one turn; press "F" to select the file option and "S" to select the save to file option. The user is asked for a file name. the filename must not have any file extension; this is automatically set to '.VAL' by the program. Please make sure that a unique new filename is used to store the setting, otherwise the program will update the device settings of the previously loaded data file as default file.

SECTION 11: NOTES

SOFTWARE: DVS V. 303 OR LATER FOR USE ON PC DOS SYSTEMS

UNIVERSAL I²C V. 3.2 OR LATER

MTV CPU (ON BOARD) V1.0 OR LATER

1. Do not connect the printer I²C adaptor cable to the demonstration board until the microprocessor has sent out the board configuration data after power up.
2. Only install jumpers at JP19 if RTC feature is required.

   If jumpers are installed at JP19, then U24 output clock generator, must be removed. The "B" versions of the digital decoder and digital encoder support RTC (Real Time Control). Real time control means that the Digital Encoder SAA7199B, will GENLOCK to the timing signals from the Digital Decoder and clock generator. RTC is a special GENLOCK mode of the Philips Digital Video product family.
3. JP2 selects slave address 8A or 8E for the digital decoder. The microcontroller transmits data to slave address 8A for the SAA7191 and to slave address 8E for the SAA7151B.
4. The microprocessor may have other menu and programming functions at a future date. If so, the sign-on message will contain new instructions and options as they become available.
5. IC U14 may not be installed from the factory. It can be used to store screen messages and board configuration settings in future software revisions of the onboard microprocessor at U13.
6. A display monitor such as Sony 1342Q or similar is a good choice for evaluating the Y/C, RGB, or Composite Video outputs from the evaluation board. This monitor also displays and decodes PAL if the demo board is reprogrammed.
7. The onboard microprocessor will set up the board for NTSC mode, SAA7199 GENLOCK active, SAA7191 decoder installed, video input composite at JIN2. It is recommended that a reference signal be connected to the GENLOCK input connector at JGL1 so that the digital encoder, SAA7199, will have a reference. The reference can be the same video source as the input signal. Double termination of the source signal will be compensated by the automatic gain functions in the TDA8708 A/D converters.
8. High stability GENLOCK even to VCR-type signals is possible with the digital decoder and the digital encoder as well. GENLOCK to VCRs in high speed shuttle or search mode is excellent even for the digital encoder.
9. Real Time Control (RTC) allows the SAA7199 encoder to use sync and clocks from the input section comprised of the SAA7191, SAA7197, and the TDA8708. The SAA7199B does not require the reference crystal or the SAA7197 at location U24 to operate in RTC mode.

   RTC signals from the digital decoder transport frequency, phase and other critical timing information about the system clock for other Philips' devices such as the SAA7199B encoder. RTC is a special minimum system configuration feature. It is not a requirement of most applications to make use of RTC.

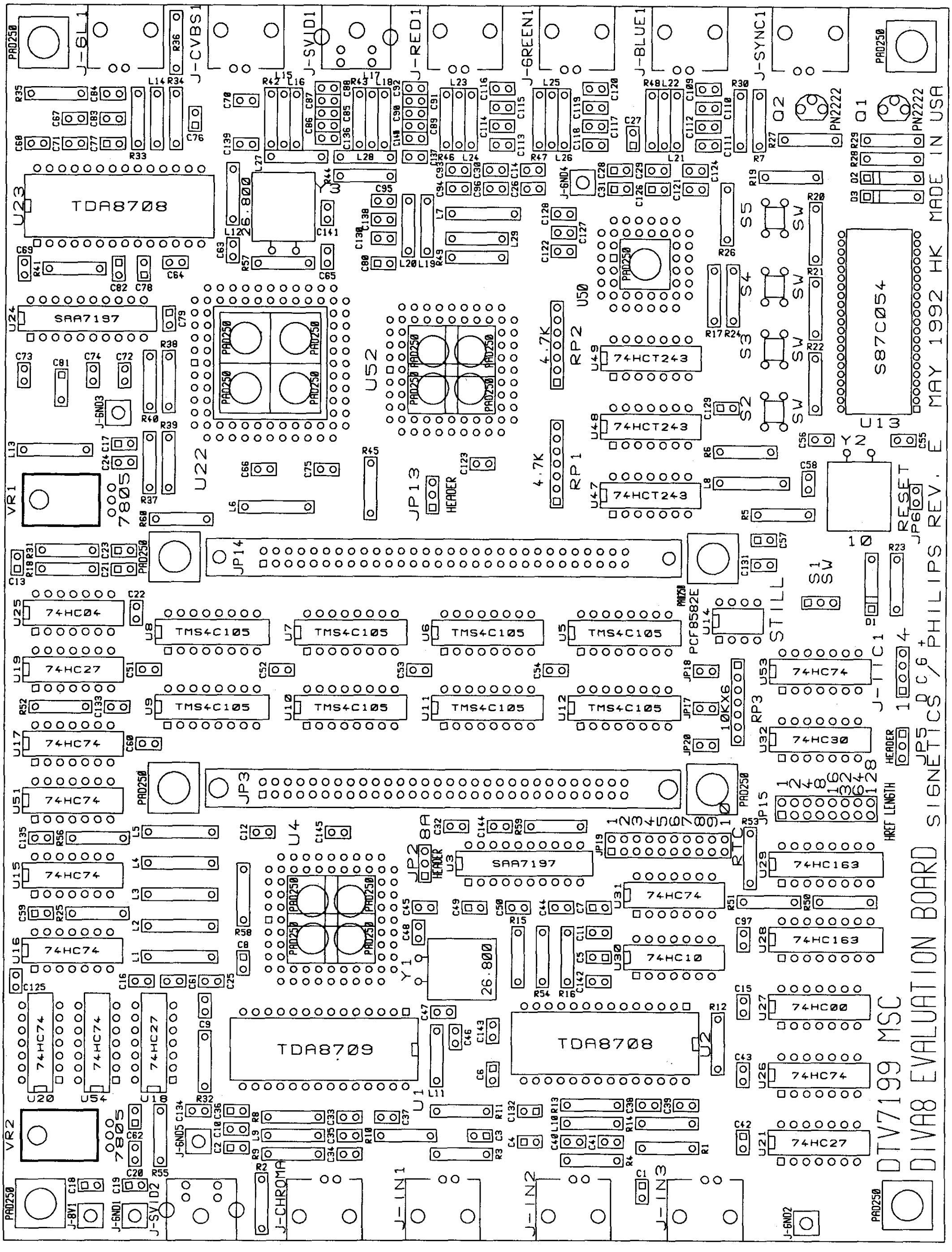
DIVA8 EVALUATION BOARD (Revised May 21, 1992)
REVISION: E
Bill of Materials May 21, 1992

ITEM	QUANTITY	REFERENCE	PART
1	7	C1, C2, C3, C4, C59, C62, C76	3.3µF
2	23	C5, C6, C7, C8, C13, C17, C18, C19, C21, C23, C27, C28, C31, C49, C57, C77, C78, C79, C80, C82, C126, C129, C132	22µF
3	52	C9, C10, C11, C12, C14, C15, C16, C20, C22, C24, C25, C26, C29, C30, C32, C33, C37, C38, C43, C44, C45, C50, C51, C52, C53, C54, C58, C60, C61, C66, C67, C69, C70, C71, C72, C73, C74, C75, C97, C121, C122, C123, C124, C125, C127, C128, C130, C131, C142, C143, C144, C145	0.1µF
4	5	C34, C40, C55, C56, C84	20pF
5	3	C35, C41, C83	30pF
6	2	C36, C42	1µF
7	2	C39, C68	.22µF
8	3	C46, C63, C133	.001µF
9	4	C47, C48, C64, C65	10pF
10	1	C81	220µF
11	12	C85, C88, C89, C92, C93, C96, C109, C112, C113, C116, C117, C120	220pF
12	6	C86, C90, C95, C111, C114, C118	390pF
13	6	C87, C91, C94, C110, C115, C119	560pF
14	2	C134, C135	.01µF
15	3	C136, C137, C138	XXXX
16	3	C139, C140, C141	680pF
17	3	D1, D2, D3	1N4148
18	1	J-8V1	8VDC
19	10	J-BLUE1, J-CHROMA1, J-CVBS1, J-GL1, J-GREEN1, J-IN1, J-RED1, J-SYNC1, J-IN2, J-IN3	BNC
20	1	J-GND1	GND
21	3	J-GND2, J-GND3, J-GND4	GND TP
22	1	J-GND5	J-GND
23	1	J-I²C1	4 PIN
24	2	J-SVID1, JSVID2	S-VIDEO
25	3	JP2, JP5, JP13	HEADER 3
26	2	JP3, JP14	HEADER 30X2
27	1	JP6	JUMPER
28	1	JP15	HEADER 8X2
29	2	JP17, JP18	HEADER 2
30	1	JP19	RTC MODE CONTROL
31	1	JP20	H_{REF0}
32	9	L1, L2, L3, L4, L5, L6, L7, L8, L13	100µH
33	3	L9, L10, L14	22µH
34	2	L11, L12	10µH
35	15	L15, L16, L17, L18, L19, L20, L21, L22, L23, L24, L25, L26, L27, L28, L29	2.7µH
36	2	Q1, Q2	PN2222
37	7	R1, R2, R3, R4, R7, R30, R36	75
38	13	R5, R6, R10, R11, R19, R20, R21, R22, R23, R32, R39, R50, R51	10K

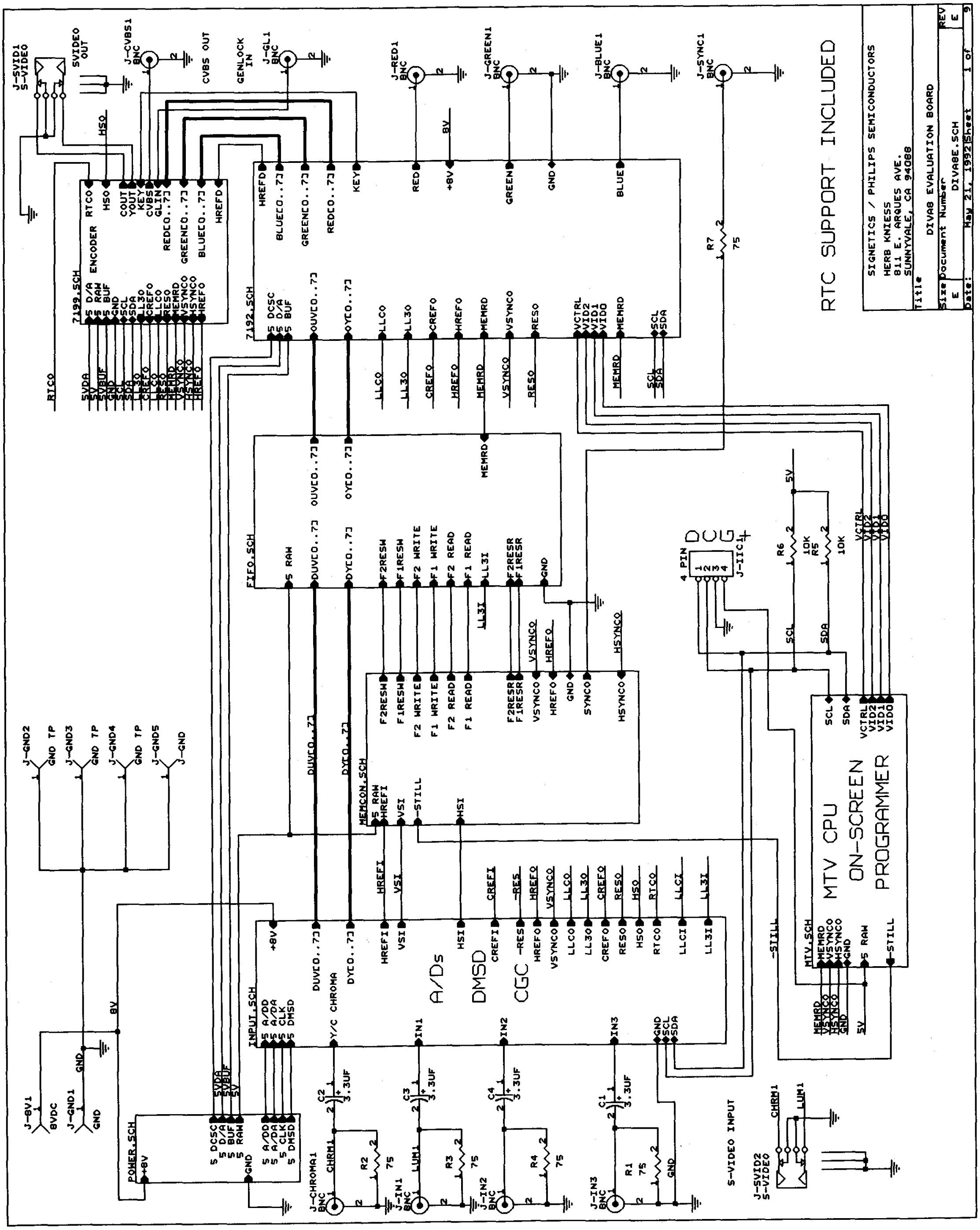
DIVA8 EVALUATION BOARD (Continued) (Revised May 21, 1992)

ITEM	QUANTITY	REFERENCE	PART
39	6	R8, R9, R13, R14, R33, R34	750
40	4	R12, R15, R35, R41	330
41	4	R16, R37, R59, R60	22
42	1	R17	47K
43	13	RP1, RP2, R18, R24, R25, R27, R28, R45, R53, R54, R55, R56, R58	4.7K
44	1	R26	10
45	2	R29, R40	1.5K
46	1	R31	33K
47	1	R38	680K
48	3	R42, R43, R44	30
49	3	R46, R47, R48	15
50	1	R49	15K
51	1	R52	6.8K
52	1	R57	100K
53	1	RP3	10KX6
54	1	S1	SW SPST
55	4	S2, S3, S4, S5	SW PUSHBUTTON
56	1	U1	TDA8709
57	2	U2, U23	TDA8708
58	2	U3, U24	SAA7197
59	1	U4	SAA7191B
60	8	U5, U6, U7, U8, U9, U10, U11, U12	TMS4C1050
61	1	U13	S87C054
62	1	U14	PCF8582E
63	9	U15, U16, U17, U20, U26, U31, U51, U53, U54	74HC74
64	3	U18, U19, U21	74HC27
65	1	U22	SAA7199B
66	1	U25	74HC04
67	1	U27	74HC00
68	2	U28, U29	74HC163
69	1	U30	74HC10
70	1	U32	74HC30
71	3	U47, U48, U49	74HCT243
72	1	U50	SAA7169
73	1	U52	SAA7192A
74	2	VR1, VR2	7805
75	2	Y1, Y3	26.800
76	1	Y2	10MHz

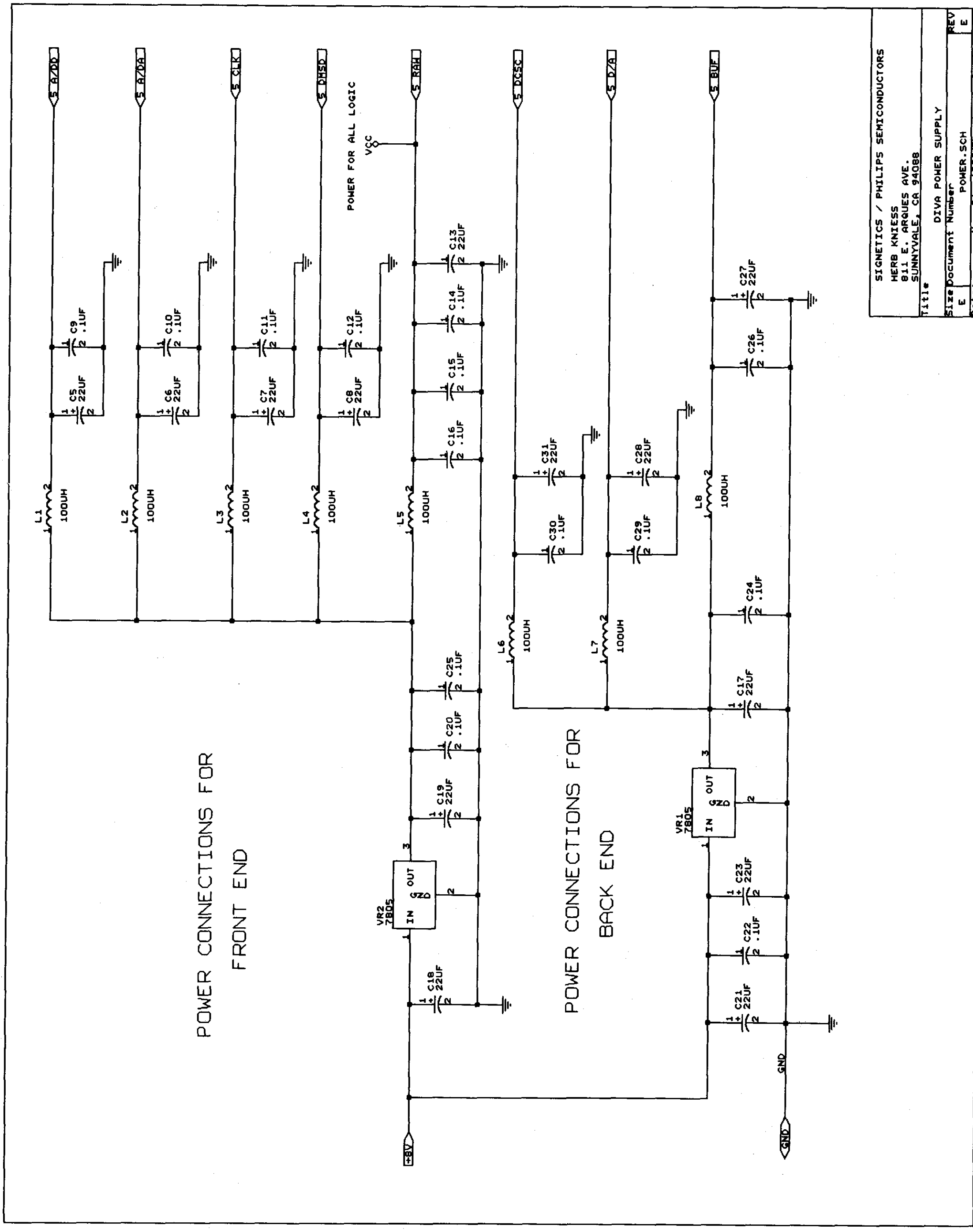
DTV7199 Digital Television Demonstration System



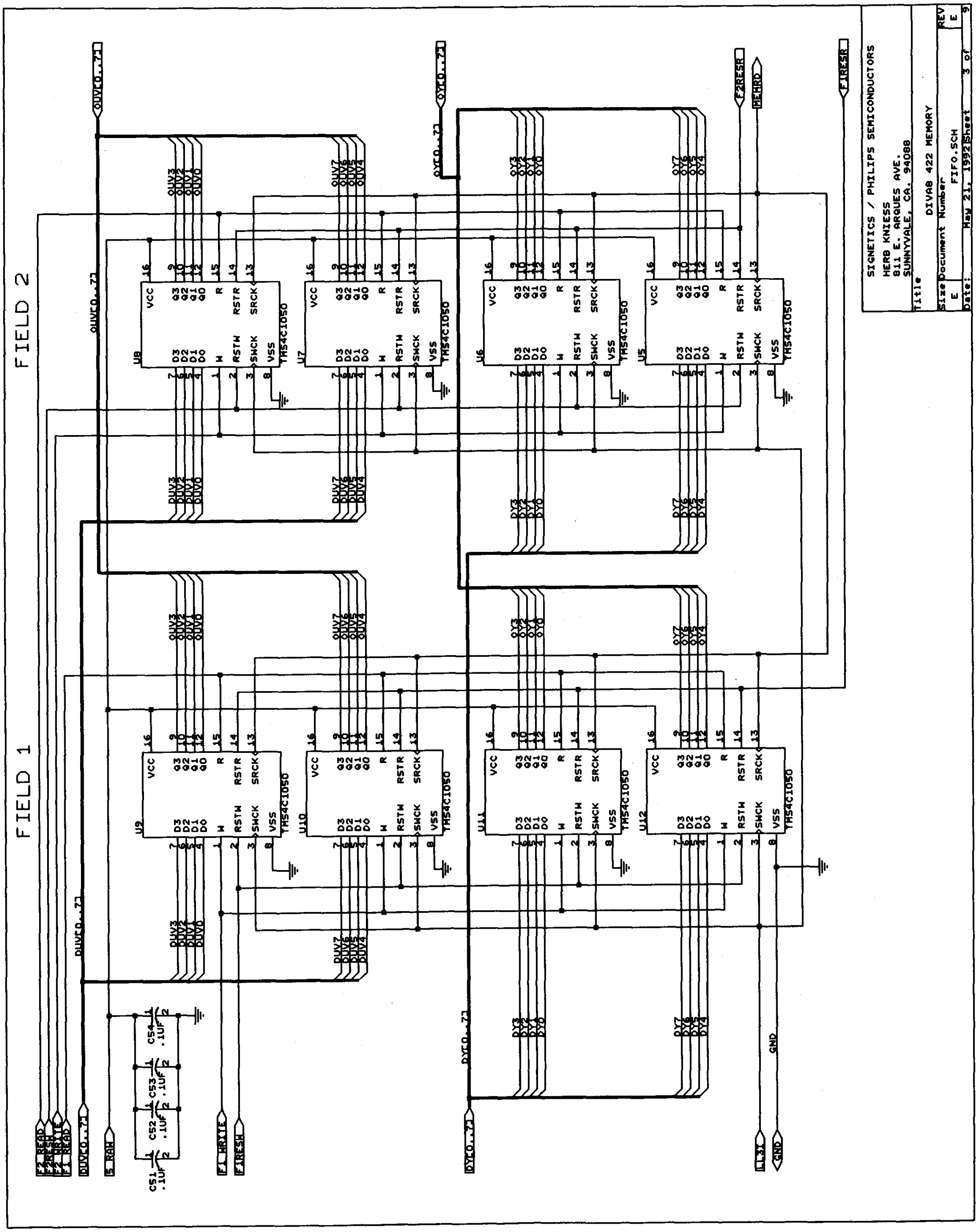
DTV7199 Digital Television Demonstration System



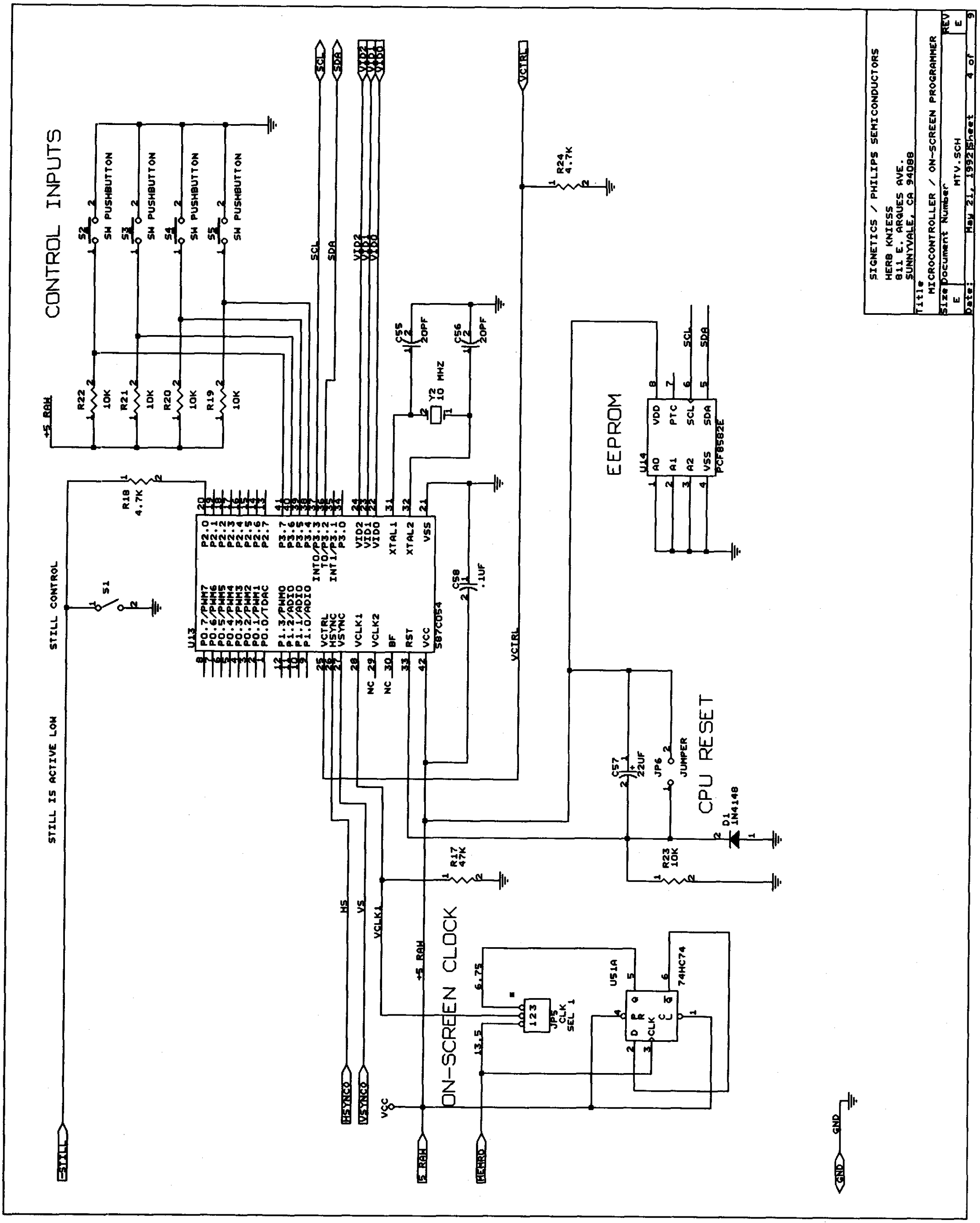
DTV7199 Digital Television Demonstration System



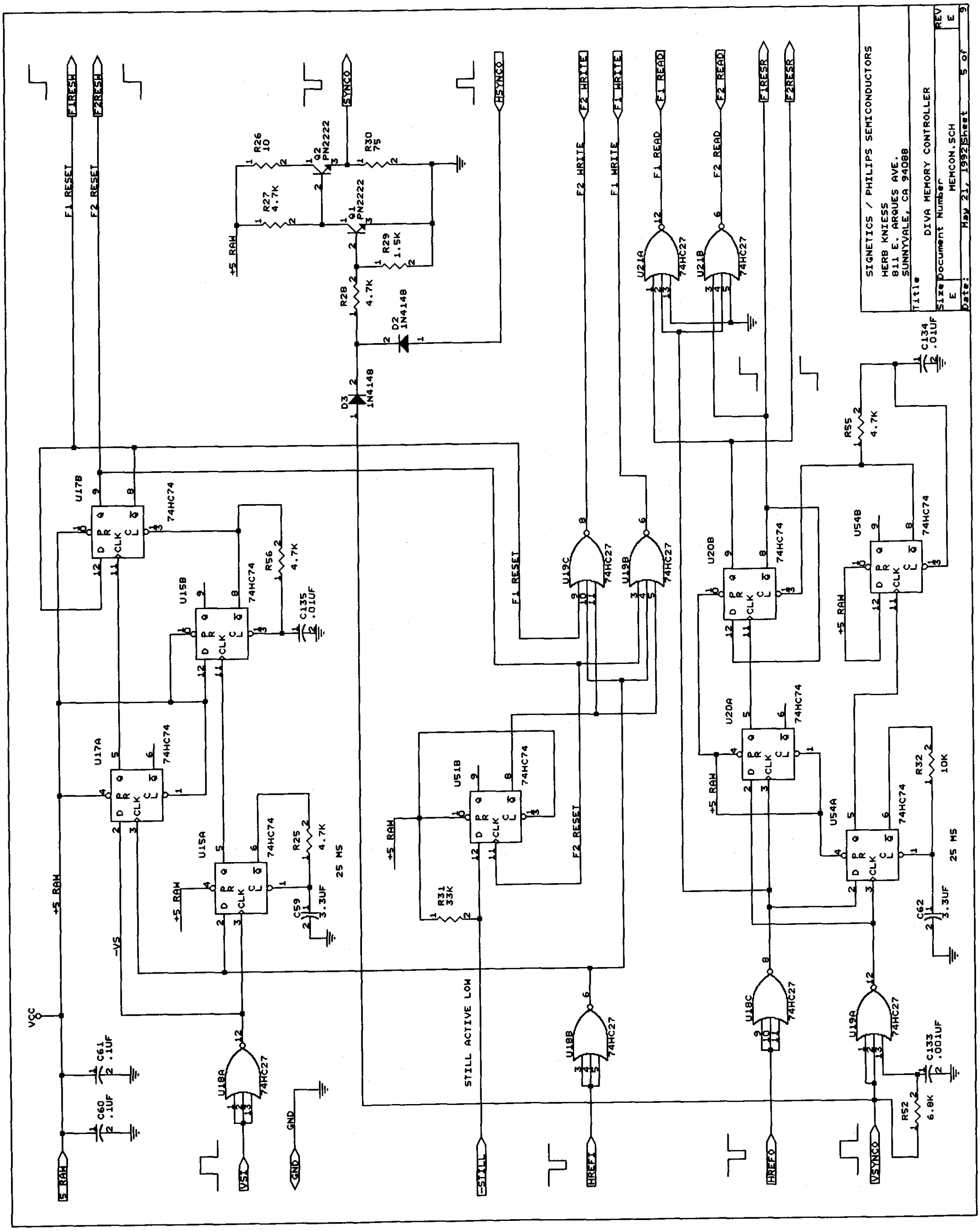
DTV7199 Digital Television Demonstration System



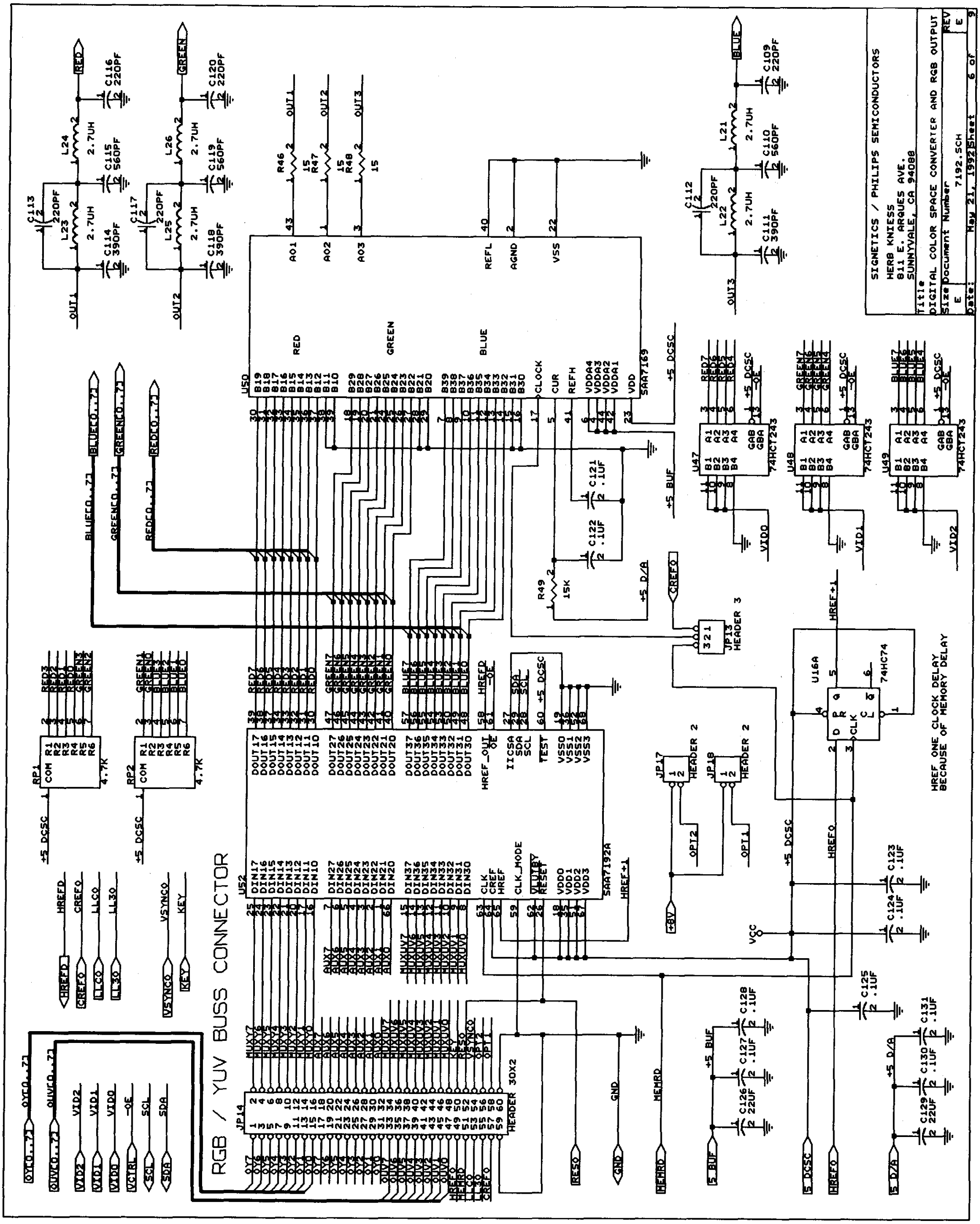
DTV7199 Digital Television Demonstration System



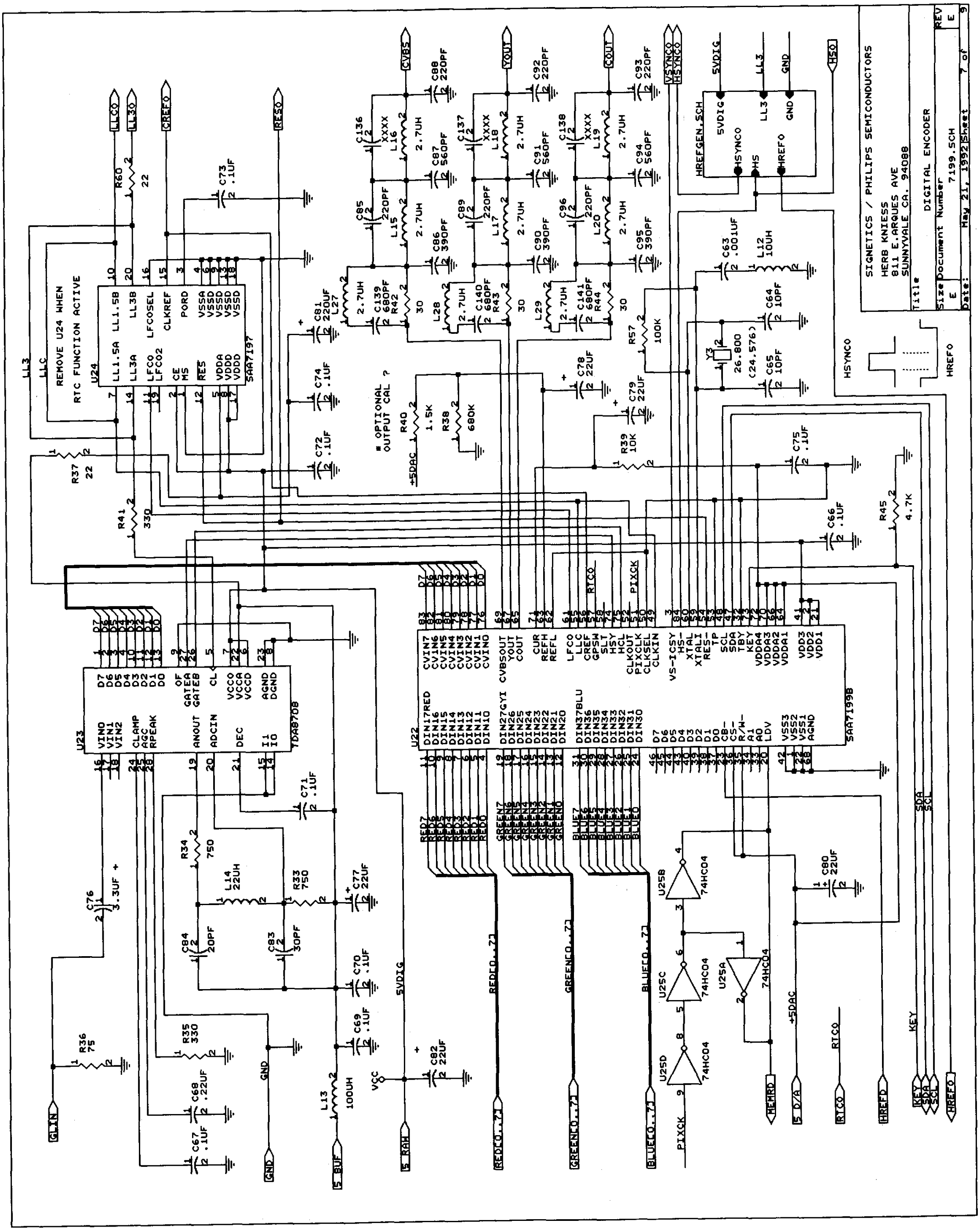
DTV7199 Digital Television Demonstration System



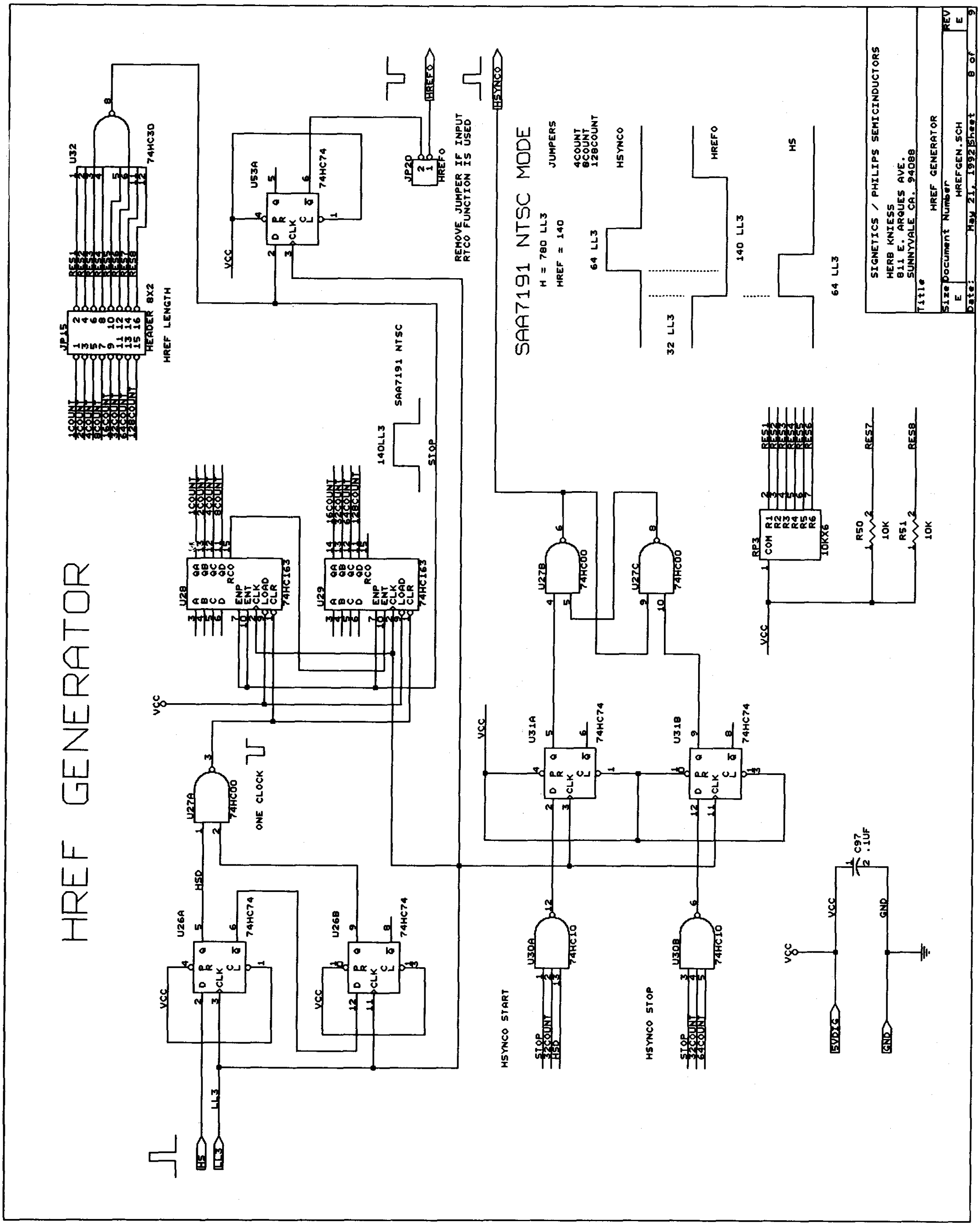
DTV7199 Digital Television Demonstration System



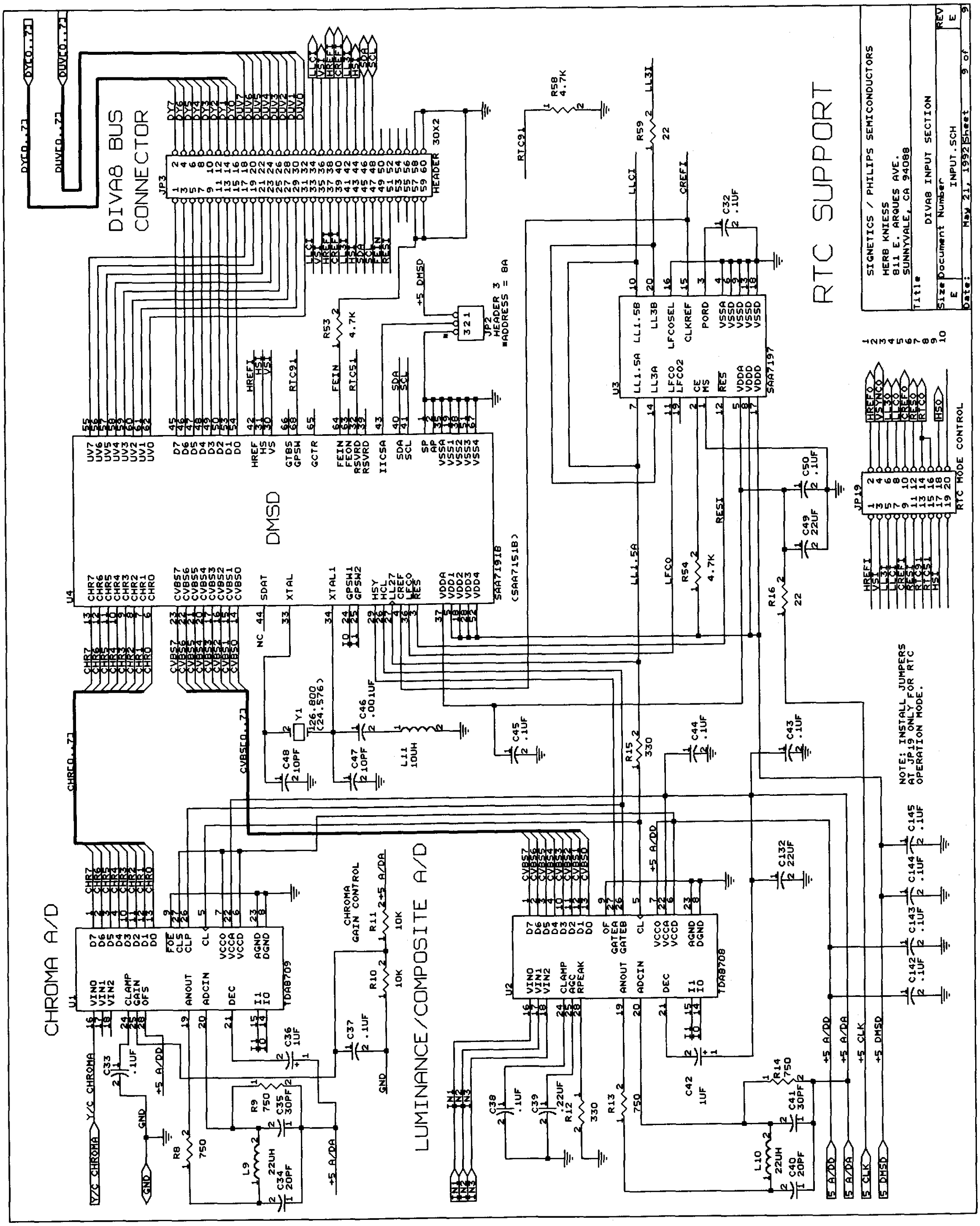
DTV7199 Digital Television Demonstration System



DTV7199 Digital Television Demonstration System



DTV7199 Digital Television Demonstration System



APPENDIX TO DTV7199 APPLICATION NOTE

Measurements on SAA7199B

The digital encoder SAA7199B is brought into slave mode and a digital pattern generator is applied to feed the data to the encoder's input. With a test pattern according to CCIR test procedure 100% luminance (white) and 75% color saturation (see application note "Digital interface for component video signals") a standard color bar test signal is generated. Figure 1 shows the measurement on Tektronix 521A vectorscope for a PAL signal under a 13.5MHz clock (CCIR 601). The color dots are clearly in the target boxes. The small deviations (spot size and angle) are in the accuracy limitations of an 8-bit representation of video baseband signals.

Figure 2 shows the transients for 100% color saturation in primary colors by means of a multiple color sawtooth test signal. This test signal, shown in Figure 3 in its time domain, provides luminance ramps and color saturation (envelope) ramps together. It supports differential phase measurement with real video specific constraints (no saturation at black). The result of such a check is shown in Figure 4. The differential phase error is less than 1.5 degrees peak-to-peak. The CCIR color bar tolerance boxes are about four times as large.

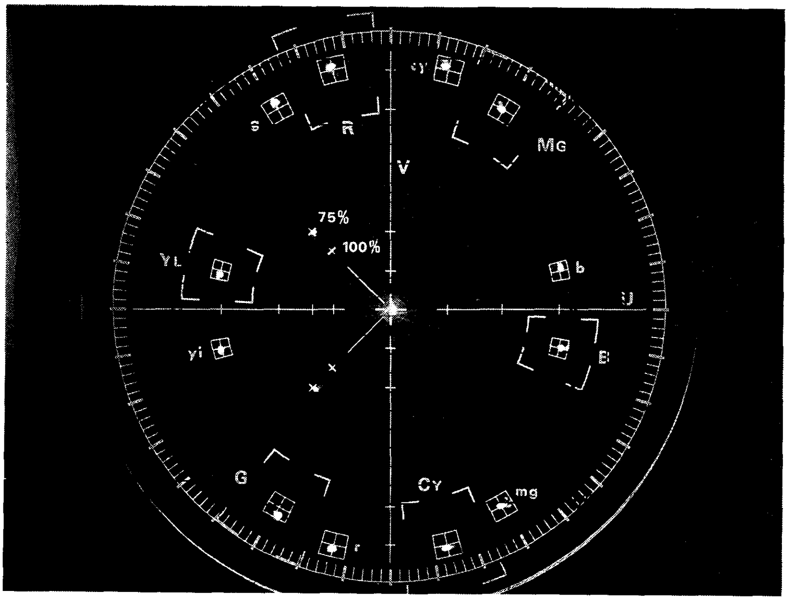


Figure 1. Color bar test signal on the vectorscope

DTV7199 Digital Television Demonstration System

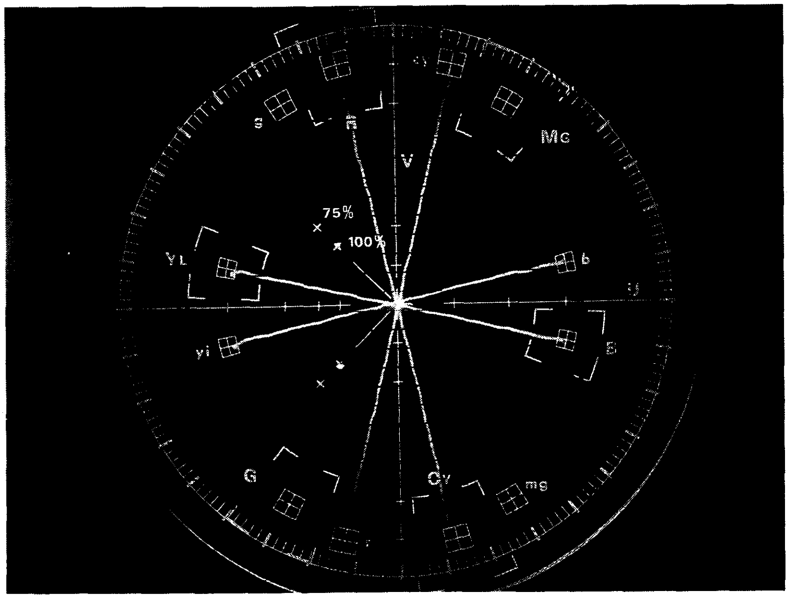


Figure 2. Color transients

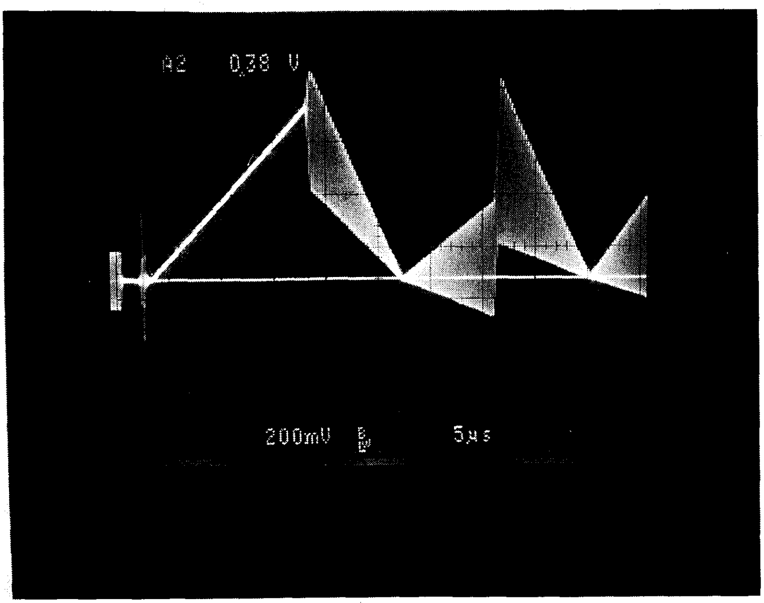


Figure 3. Color and luminance ramps combined signal

DTV7199 Digital Television Demonstration System

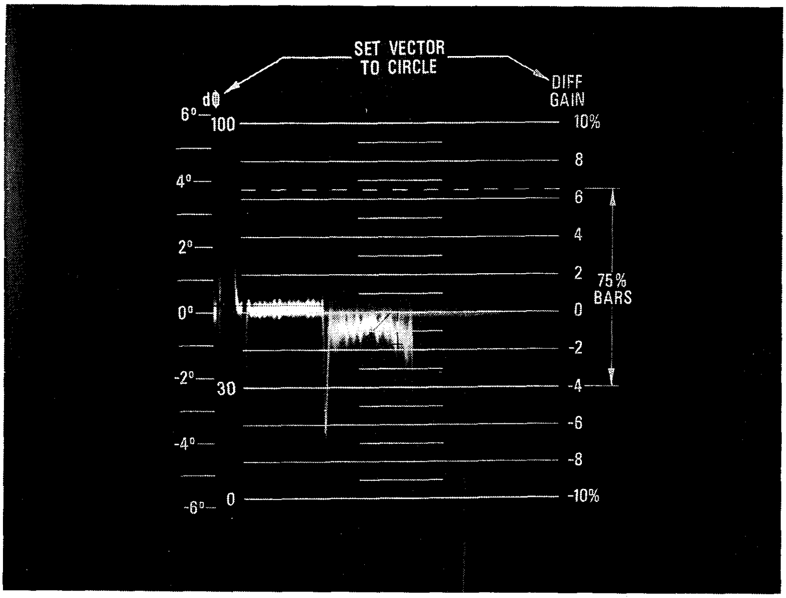


Figure 4. Differential phase measurement

DTV7199 Digital Television Demonstration System

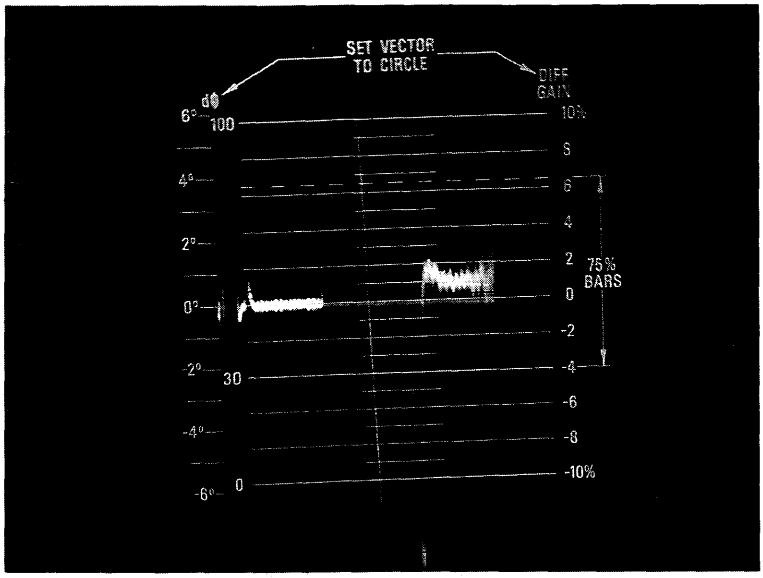


Figure 5. Differential phase measurement
Second color ramp

SAA7199B operational modes

Author: Herb Kniess

INTRODUCTION

The SAA7199B Digital Video Signal Encoder can be configured to operate in one of four different modes. Each operation mode has different system cost and interface considerations. One or more modes may be implemented for each application depending on system requirements and hardware interfaces. This note describes the different hardware configurations for the different modes and also the available timing programmabilities.

GENLOCK MODE

In many system applications it is necessary to GENLOCK the CVBS video output of the encoder to a master timing reference. It is necessary in GENLOCK MODE to adjust the horizontal sync and subcarrier phase relative to the master reference in order to compensate for external phase shift or signal delays in cable connections. The SAA7199B can GENLOCK to stable references and also to signals with time base errors such as signals from consumer VCRs. As all signals including the subcarrier will follow the reference signal, RS170A cannot be enforced automatically; if the reference is standard, the encoded CVBS will be standard. See Figure 1 for connection diagram.

GENLOCK mode can be turned off via I^2C control register in the absence of a reference sync signal and the sync-to-clock PLL will assume the nominal default frequency (see Stand Alone Mode). In GENLOCK mode it is necessary to digitize the reference signal using the TDA8708 A/D converter. The TDA8708 A/D converter is operated at normal data rates, not 2×, as in applications with the 8-bit digital decoders. The SAA7197 clock generator is used to assist in generation of the system clock. A stable crystal reference completes the GENLOCK configuration. An external stable clock could be supplied at Pin 59 instead of the crystal oscillator. It is important to note that in GENLOCK mode the SAA7199B will precisely follow the sync and subcarrier phase of the reference signal. The SAA7199B generates all sync, clock, and timing signals to strobe and trigger the data source. The SAA7199B supports that by extensive programmability.

Input data, e.g., from a frame buffer memory, must be supplied when requested so that encoded signals will be available on DAC outputs in time with the reference signal. Data inputs to the encoder must be supplied ahead of the analog output sync signal because of internal pipe line delays of 55 clocks. The horizontal sync (HSN) on Pin 84 can be programmed relative to the reference signal to compensate for memory access delays and the 55 clock pipeline delay in the encoder (see also the chapter on Timing later in this application note). The composite blanking CBN must be supplied to Pin 23 as an input to synchronize data handling. Pin 3 VS/CSY is normally programmed as vertical output to be used as a reset for memory controllers at the beginning of a field at line 6. A single clock system is shown for convenience and ease of interface (for the double clock system, please refer to the datasheet). IC 3A and 3B delay the system clock by at least 8ns at Pins 55 and 49 to follow the LDV clock requirements. LDV latches data from the signal data source.

STAND ALONE MODE

STAND ALONE MODE is a simplified version relative to GENLOCK mode but shows the same data input interface. The TDA8708 A/D converter is not used and stable sync and timing signals are always generated by the SAA7199B based on a stable clock Since the subcarrier frequency is also synthesized out of this clock frequency, the clock needs to have sufficient accuracy and stability to ensure RS1970A standard. It is an option to let the clock be generated by the SAA7199B itself in conjunction with a SAA7197 and a crystal.

The crystal reference frequency is 24.576MHz for CCIR system or 26.8MHz for square pixel system, but only one crystal for PAL or NTSC. CCIR-624 specifies - as broadcast requirement - a tolerance of 5ppm (NTSC) respectively 2ppm (PAL), but regular consumer-like equipment except static deviations of 50ppm or more. By means of FSC(0...7) in programming register index-0D frequency offset in the crystal reference can be compensated in the range of ±450ppm in steps of 2ppm. An external stable reference clock could be used at Pin 59 instead of the crystal oscillator. See Figure 2 for connection diagram. U2A and U2B is used again to delay the main encoder clocks relative to LDV about 10ns. LDV latches data from memory.

SLAVE MODE

All timing signals such as sync, clocks, and blanking are provided by external sources. The clocks must be crystal stable, without exception.

Note the clock delay through UIA and UIB of about 10ns. No other components are required because the external source provides all timing information. Pin 59 XTALI should be grounded because the reference crystal is not needed. Figure 3 shows pin connections and signal directions. The output analog sync will contain proper equalizing, serration, and burst blanking signals even if they are not contained on input sync signals.

As an option, the clock may be generated by the SAA7199A in conjunction with SAA7197 and a reference crystal (see Stand Alone Mode).

REMOTE GENLOCK (RTC MODE)

RTC MODE (Real Time Control) is an exclusive feature of Philips Digital Decoders and Digital Encoders. Pin 57 (RTCI) must be programmed and connected to a SAA7191B or SAA7151B digital decoder RTCO pin. In RTC mode the digital decoder front end provides all timing information including the clock to the SAA7199B. The clock frequency may vary, especially since a digital decoder could be locking to a VCR source. However, with the connection of RTCO from a decoder, the encoded subcarrier in the SAA7199B will be stabilized even with VCR sources as inputs. RTC and the DMSDs LLC-clock can be applied to the SAA7199B under stand alone, as well as slave mode. The connection block diagram is shown in Figure 4. Note the clock delay through U3A and U3B of about 10ns.

RTC MODE allows a complete decoding and encoding system to be configured with only four processing devices. The following ICs are required as the minimum configuration:

1. TDA8708 A/D Converter
2. SAA7151B or SAA7191B Digital Decoder
3. SAA7157 or SAA7197 Clock Generator
4. SAA7199B Digital Encoder

The RTC line contains valuable data about the system clock phase and frequency and related subcarrier information generated within the decoder during the color demodulation process. The data is updated every line and coded in a serialized protocol; protocol start is self-synchronizing, i.e., sender and receiver can have different line-sync phase.

When a SAA7199B is connected directly to the decoder clock system, it is possible to encode stable subcarrier even with variable but line-loaded system clocks from the decoding front end. The output sync and subcarrier from the encoder will have the same timing (standard or non-standard) as the input demodulated signals (standard or non-standard) in front of the decoder. The digitized CVBS in front of the DMSD can be applied to the CVBS input Pins (76-83) of the

SAA7199B operational modes

SAA7199B to be used with the CVBS key function. The timing programming range of HS as DMSD output and HSN as DENCs input allows direct sync-coupling. The subcarrier phase is adjustable via programming as needed by the application purpose. The DP inputs of the SAA7199B may carry manipulated or other video overlay data. With a memory buffer included in the system between DMSD and DENC, the sync timing can be different in phase than the accumulated data processing delay of about 150 clocks, but will remain constant because the clocks are the same.

DATA, BLANKING, AND SYNC TIMING

Processing Delay and Programmable Timing

Depending on the different operation modes of the digital encoder SAA7199B, the timing – from the digital input side to the analog output respectively to the analog CVBS reference – can be programmed in different ways.

Figure 5 is a reprint of Figure 10 from the SAA7199B data sheet; it shows the timing of input data and sync to output representing that sync and data. There is a constant 55 pixel clock pipeline delay from input data to analog output signals. The horizontal sync-signal HSN at Pin 84 can be an input or an output depending on the selected operational mode of the encoder. The relative timing of HSN to the analog output sync is programmable for input as well as for output modes.

Composite blanking CBN at Pin 23 must have a rising edge at the beginning of active data to ensure proper operation of the UV format demultiplexer and also to remove the blanking condition. Video blanking is forced during vertical and horizontal blanking regardless of the state of CBN signal of Pin 23.

Output Timing to GENLOCK Reference Input

The SAA7199B has an internal timing machine which generates all timing and gating signals to generate the proper sync pulse position (phase), sync pulse duration, sync slopes, default blanking, burst gate position and length as well as burst envelope (shaping) for all possible clock frequencies and video standards to be selected. The result of that can be seen in the CVBS output signal- or Y-C outputs at Pins 69, 67 and 65.

In GENLOCK mode the DENC refers its internal timing machine to the digital CVBS signal (applied to the Pins 76 to 83). The DENC investigates that external CVBS, detects the slope of the horizontal synchronization pulse, and locks phase and frequency of the clock via SAA7197 and sampling ADC TDA8708 to this reference t_{REF1} (Line-Locked-Clock system). Beyond that it is possible to program a constant time offset between sync-pulse of the reference t_{REF1} and sync-pulse of the CVBS output, respectively the Y-C outputs (compare Figure 5), but maintaining the Line-Locked-Clock feature. By programming the GDC-bits in register index-05 to zero the CVBS output is 17 pixel clock cycles later than the reference CVBS; programming GDC to 17 decimal (11 hexadecimal) brings reference and CVBS output into identical phase. Increasing the GDC value up to 63 decimal (3F hexadecimal) brings the internal timing scheme and the output CVBS in advance of the reference input by up to 46 pixel clock cycles earlier.

Independent of this GENLOCK-delay programming via GDC, it is also possible to adjust the subcarrier phase of the output relative to the subcarrier phase at the reference input. The programming byte CHPS(0..7) in register index-0C covers the whole cycle of 360 degrees in 256 steps, which means 1.4 degree each step.

The adjustment of GENLOCK-delay and subcarrier phase offset is relevant in an application where the generated DENC output is further processed and mixed with other video signals for editing purposes. Also for modulating multiple video sources onto one cable or for broadcasting by air a well-defined phase relationship of these signals is necessary in order to keep channel cross-talk under control.

CBN and t_{REF2}

The processing (pipeline) delay t_{ENC} from digital data input to analog output is constant under all modes, input formats, clocks and other programming conditions and is 55 pixel clocks (compare Figure 5). Data fed into the digital input ports DPn (n=1,2,3) are visible 55 pixel clock cycles later in the analog video output signal. Figure 5 shows the composite blanking input CBN in nominal standard form; CBN may claim a wider blanking period if less data than the nominal active pixels per line are available. The same processing delay t_{ENC} = 55 pixel clocks ahead of the leading slope of the CVBS output signal is the reference point for the leading edge of the (imaginary) sync pulse at the data input. In Figure 5 this point is signed with t_{REF2}. The different standard requirements for NTSC and PAL and the various possible clock frequencies result in different number of clock pulses for the nominal blanking period, and for the time from the start of sync to the end of line blanking. Table 1 lists the relevant numbers. The number for nominal line blanking period is implemented via the internal timing machine as default; it cannot be shortened, but blanking can be extended by CBN at Pin 23. The rising slope of CBN also synchronizes the UV format demultiplex sequence.

Table 1. Standards and Number of Clocks

STANDARD SYSTEM	PIXEL CLOCK (MHZ)	CLOCKS PER LINE	ACTIVE PIXELS	LINE BLANKING (PIX-CL)	SYNC START TO ACTIVE LINE	LINE PERIOD (μS)	BLANKING PERIOD (μS)
NTSC-SQP	12.273	780	640	140	125	63.56	11.41
PAL-SQP	14.750	944	768	176	163	64	11.93
NTSC-CCIR	13.500	858	720	138	122	63.56	10.22
PAL-CCIR	13.500	864	720	144	134	64	10.67

SAA7199B operational modes

HSN, VSN as output (GENLOCK, stand-alone)
In stand-alone mode as well as in GENLOCK mode the SAA7199B outputs an HSN signal at Pin 84 and a VSN/CSYN signal at Pin 3, in order to provide the signal source (graphic- or pattern-generator, memory controller) with a timing trigger signal. In order to compensate for unspecified delays in that peripheral controller, the actual position (phase) of HSN output is programmable over a range of 64 pixel clock cycles by means of the PSO-bits in register index-07. Programming PSO to "00" generates an HSN with a leading edge that is 58 pixel clock periods earlier than the nominal position t_{REF2}; "3F hex" = "63 dec" as PSO makes an HSN that is 5 pixel clock cycles after t_{REF2}. The leading edge of VSN-output, of the combined composite sync CSYN-output follows this programming of the PSO-bits to always coincide with HSN in the same clock period.

The pulse width of HSN output is always 64 clock cycles. The polarities of HSN, VSN or CSYN are independently programmable via the bits SYSEL0 and SYSEL1 in register index-04. These two bits also control whether the signal at Pin 3 acts as VS block vertical sync or as composite sync. The HSN signal form as shown in Figure 5 is called "active LOW" and requires a programming of 01 bin in SYSEL.

HSN, VSN as input (slave mode)
In slave mode, the SAA7199B requires that all sync and clock signals come from an external source. The clock frequency is supposed to be accurate and stable enough to enable the DENC to generate a proper subcarrier frequency. The clock frequency is also supposed to be line-locked, so that there is always the nominal number of clock cycles between two horizontal sync pulses.

HSN (Pin 84) and VSN/CSYN (Pin 3) act as inputs. The nominal phase relative to CBN and input data is shown in Figure 5 as t_{REF2}. Table 1 gives the times from (imaginary) sync pulse start to start of active line (end of nominal line blanking) at the DENC's input for the various standards and clock frequencies. The leading edge of the incoming sync pulse HSN triggers the internal timing machine. A minimum pulse width of one pixel clock period is required.

In order to compensate for unspecified delays in the controller for the signal source, the actual position of HSN input relative to reference point t_{REF2} is programmable over a range of 64 pixel clock cycles by means of the GDC bits in register index-05. This is not the register defining the timing offset of HSN as output, but the one to be used in GENLOCK mode to program reference to output "GENLOCK delay". Programming GDC to "00" enables the DENC to accept an HSN-input with a leading edge that is 17 pixel clock periods earlier than the nominal position t_{REF2}. If HSN-input leading edge is in phase with t_{REF2} GDC needs to be programmed with "17 dec" (11 hexadecimal); "3F hex" = "63 dec" supports an HSN-input with a leading edge that is 46 pixel clock cycles lafter t_{REF2}. The leading edge of VSN-output, of the combined composite sync CSYN-output follows programming of the GDC bits to coincide always with HSN in the very same clock period.

MULTI-PURPOSE KEY AND INPUT FORMATS

The digital encoder SAA7199B has three digital data input ports, each 8-bits wide, and named DP1, DP2 and DP3. There are seven basic input formats accepted; see Tables 10 to 16 in the data sheet. Beyond the basic format definition, the data stream can be transformed via look-up tables. The look-up tables can be used for any kind of linear or non-linear amplitude processing, as in a gain in YUV or gamma correction in RGB. CCIR-601 specifies the number range for luminance signal from 16 (black) to 235 (100% white) and for the color difference signals U and V (75% saturation) from 44 to 212. In the Philips DTV system, some slightly different numbers are chosen (DMSD-2 levels) in order to get better usage of the available 8-bit number range and to minimize truncation noise and visibility of signal limiting (clipping) artifacts. Luminance goes from 12 (black) to 230 (100% white) and provides more room for superwhite overshoots. The color difference signals are coded in two's complement and use about 20% more number range, which enhances color resolution. Refer also to the SAA7151B data sheet, Figures 5 and 6.

The SAA7199B has a CVBS KEY function, controlled by Pin 73 to insert (pixel by pixel) the reference CVBS signal in realtime into the encoded CVBS output signal. In addition, realtime input format switching is supported by means of the MPK function (Multi-Purpose Keying). Table 2, MPK-Pin and Input Formats, gives a comprehensive overview of the realtime switching possibilities by MPK at Pin 32. Two different input formats are defined simultaneously via software programming and can be mixed on a pixel-by-pixel basis at the DP input pins. For example it can be switched from any YUV format to RGB 24-bit or indexed color, or between RGB with and without look-up table.

SAA7199B operational modes

Table 2. MPK-Pin and Input Formats

MPK PIN #32	PROGRAM-BYTE INDEX 00HEX D7 VTBY	D6 FMT2	D5 FMT1	D3 FMT0	D2 CCIR	INDEX 09HEX D5 MPKC1	D4 MPKC0	SELECTED: FORMAT #	LUTs	LEVELS ACC. TO
LOW	(*)	0	0	0	(*)	X	X	#0	(*)	(*)
LOW	(*)	0	0	1	(*)	X	X	#1	(*)	(*)
LOW	(*)	0	1	0	(*)	X	X	#2	(*)	(*)
LOW	(*)	0	1	1	(*)	X	X	#3	(*)	(*)
LOW	(*)	1	0	0	(*)	X	X	#4	(*)	(*)
LOW	(*)	1	0	1	1	X	X	#5	(*)	CCIR
LOW	X	1	1	0	X	X	X	NOT USED		
LOW	0	1	1	1	1	X	X	#7	8 → 24	CCIR
HIGH	X	0	0	0	(*)	0	0	#0	BYPASS	(*)
HIGH	X	0	0	1	(*)	0	0	#1	BYPASS	(*)
HIGH	X	0	1	0	(*)	0	0	#2	BYPASS	(*)
HIGH	X	0	1	1	(*)	0	0	#3	BYPASS	(*)
HIGH	X	1	0	0	(*)	0	0	#4	BYPASS	(*)
HIGH	X	1	0	1	1	0	0	#5	BYPASS	CCIR
HIGH	X	1	1	0	X	0	0	NOT USED		
HIGH	X	1	1	1	1	0	0	#7	8 → 24	CCIR
HIGH	X	X	X	X	X	0	1	#5	ACTIVE	CCIR
HIGH	X	X	X	X	X	1	0	DON'T USE		
HIGH	X	X	X	X	X	1	1	#7	8 → 24	CCIR

NOTES:

X = don't care
(*) → see table about VTBY and CCIR programming bits

HIGH = TTL level high, i.e., > 2.0V
LOW = TTL level low, i.e., < 0.8V

LUTs: BYPASS = Look-up tables not in signal path
ACTIVE = the three RAM-tables are used independently as three 8-bit → 24-bit Look-up tables in the three channels RGB or YUV

8 → 24 = the RAM-block is used as one 8-bit → 24-bit look-up table to transform indexed or palettized 8-bit color into 24-bit color

SAA7199B operational modes

Table 3. VTBY and CCIR Bits

MPK PIN #32	PROGRAM-BYTE				SELECTED:	
	INDEX 00HEX		INDEX 09HEX			
	D7 VTBY	D2 CCIR	D5 MPKC1	D4 MPKC0	LUTs	LEVELS ACC. TO
LOW	0		X	X	IN DATA-PATH	
LOW	1		X	X	IN BYPASS	
LOW		0	X	X		DMSD-2
LOW		1	X	X		CCIR 601
HIGH	X		0	0	IN DATA-PATH	
HIGH	X	0	0	0		DMSD-2
HIGH	X	1	0	0		CCIR 601
HIGH	X	X	0	1	IN DATA-PATH	CCIR 601
HIGH	X	X	1	0	DON'T USE	DON'T USE
HIGH	X	X	1	1	8 → 24 BITS	CCIR 601

NOTES:

X = don't care

HIGH = TTL level high, i.e., > 2.0V

LOW = TTL level low, i.e., < 0.8V

SAA7199B operational modes

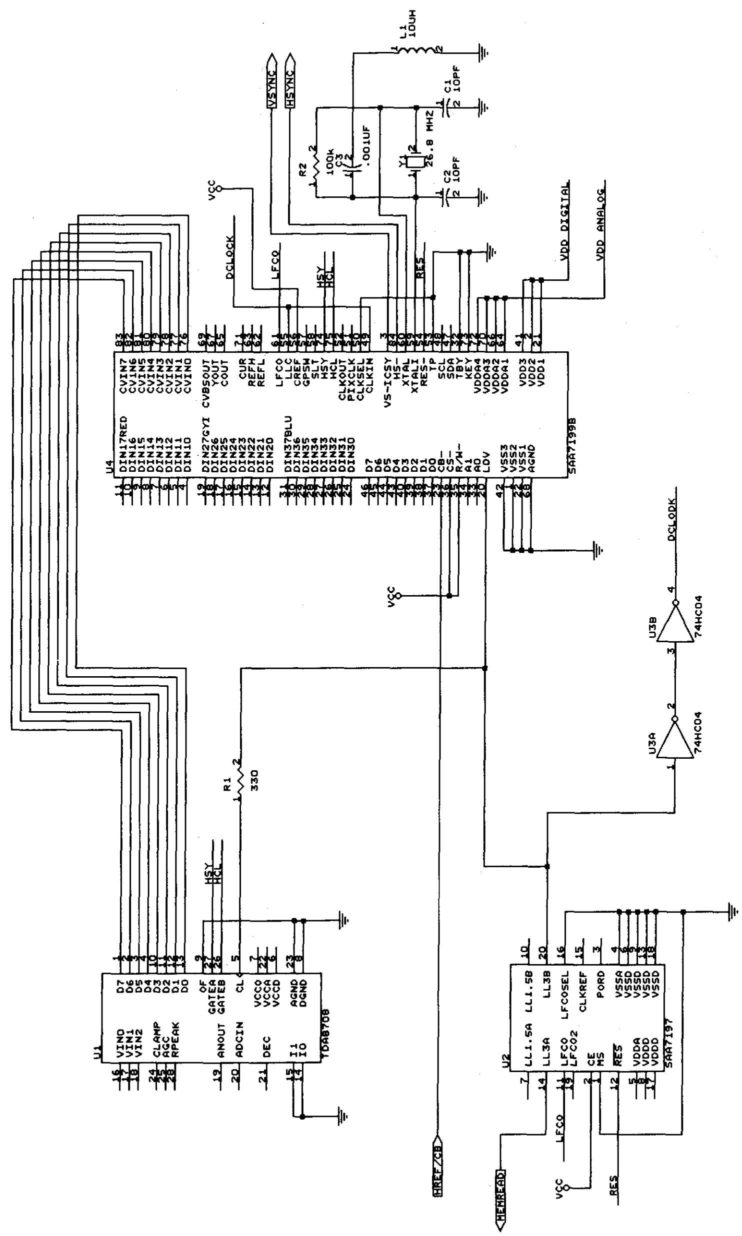


Figure 1. SAA7199B clock wiring GENLOCK mode

SAA7199B operational modes

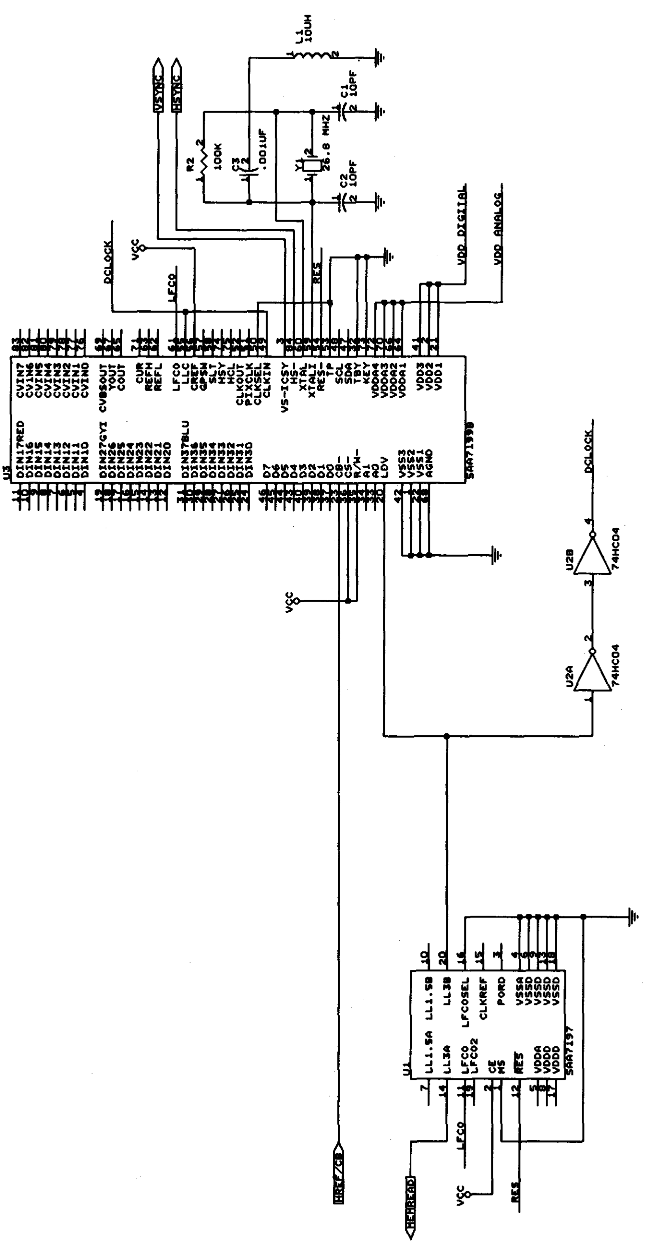


Figure 2. SAA7199B clock wiring Stand Alone mode

SAA7199B operational modes

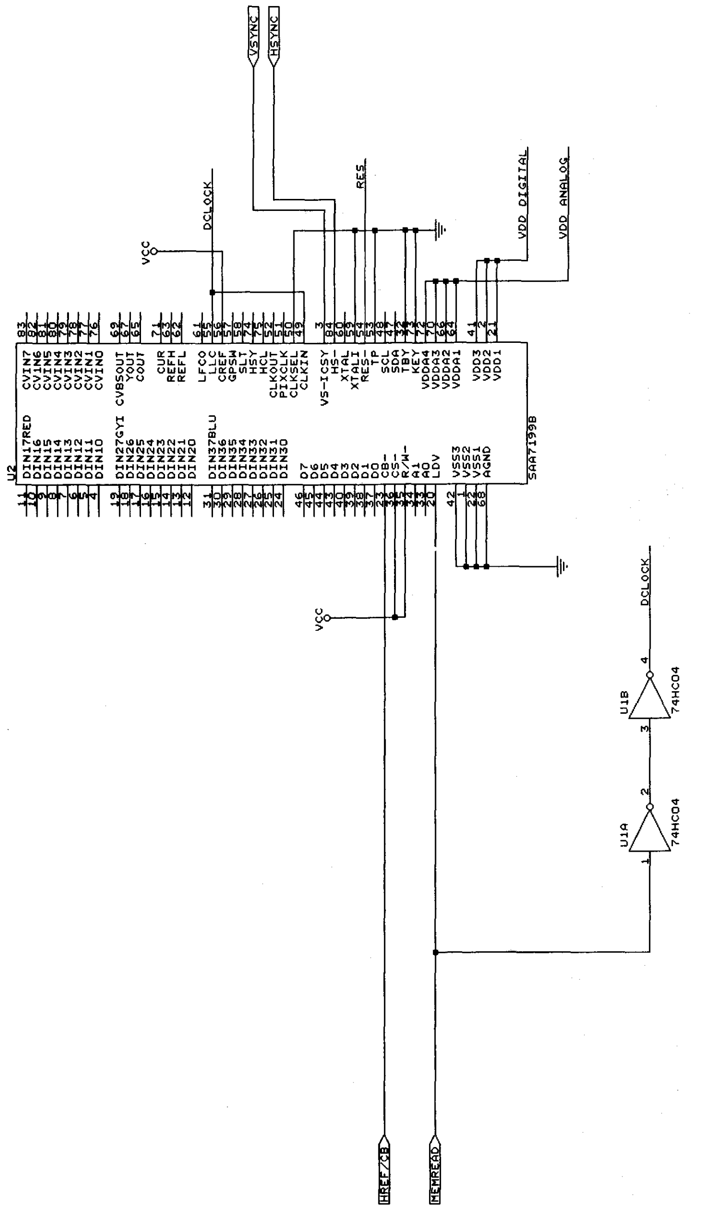


Figure 3. SAA7199B clock wiring Slave mode

SAA7199B operational modes

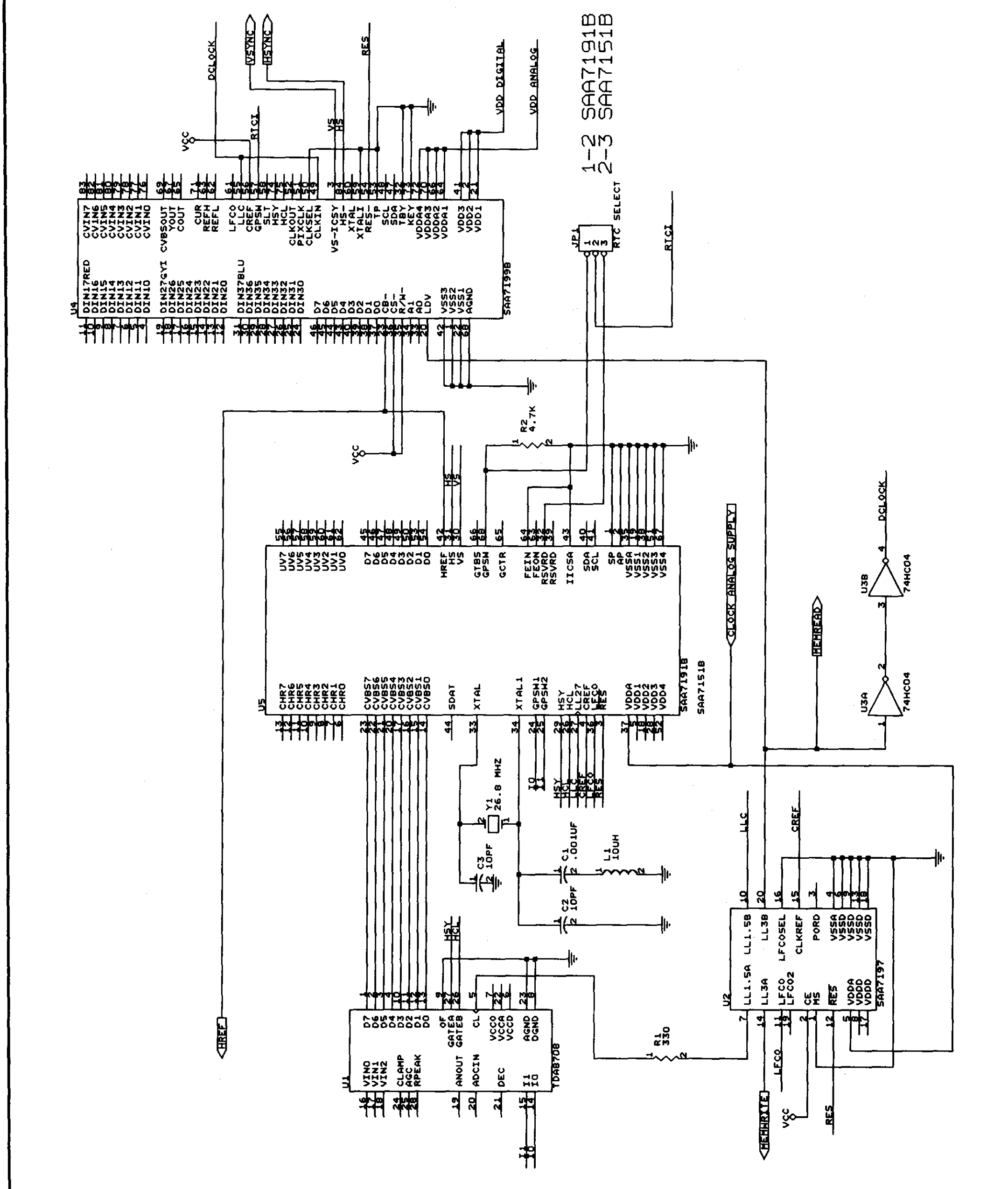
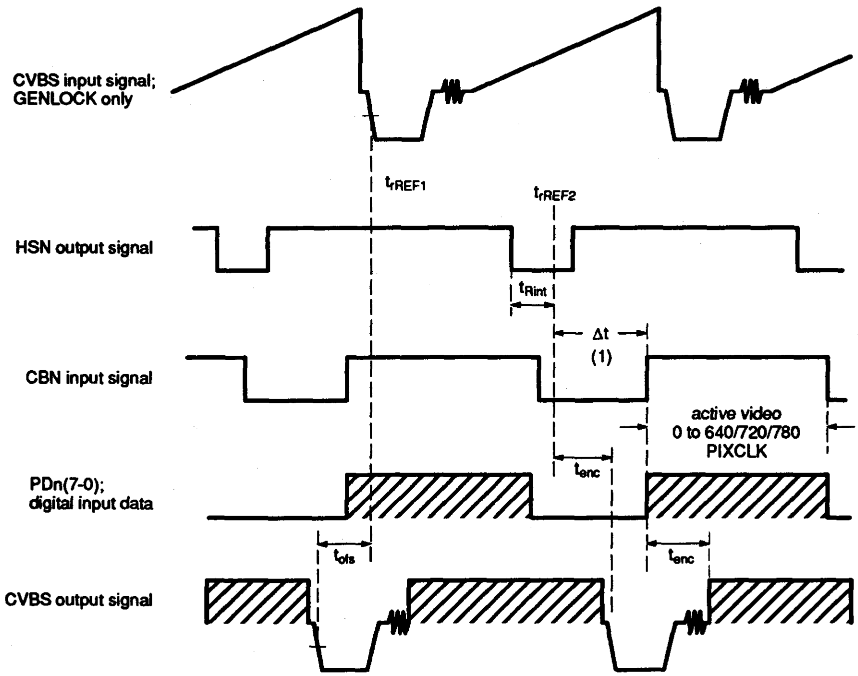


Figure 4. SAA7199B clock wiring Remote GENLOCK (RTC) with SAA7191B decoder



(1) $\Delta t = 125 \times$ PIXCLK at 12.27 MHz
$\Delta t = 163 \times$ PIXCLK at 14.75 MHz
$\Delta t = 134 \times$ PIXCLK at 13.50 MHz / 50 Hz mode
$\Delta t = 122 \times$ PIXCLK at 13.50 MHz / 60 Hz mode

Figure 5. Processing delay and programmable timing

DTV7186

Author: Herb Kniess

OVERVIEW

The DTV7186 application note is designed to show proper connection and operation of the SAA7186 resizer and SAA7191 color decoder. The SAA7199 digital encoder is also shown as the video output device for monitoring the performance of the system. Philips Semiconductors makes available the DTV7186 MSC demo board for customer evaluation and measurement purposes. Please refer to the DTV7186 revision D schematic on the pages that follow for particular information about the design of this board.

There are five main functional parts needed to demonstrate the operation of the SAA7186 resizer. The input section digitizes, processes, and resizes the incoming analog video signal. The logic on page 4 of the schematic adds special control data values into the serial memory write data path. A 1 megabyte serial memory stores the resized image and control information. During read operation, the logic on page 3 of the schematic decodes the control information and generates a display window. Finally, the digital video data is modulated and converted back to an analog composite video signal by the SAA7199 digital encoder. An 87C751 microprocessor is provided to program all Philips video devices on the board via IIC serial communication.

INPUT SECTION

Please refer to Section 2 and Section 3 of DTV7199 application note for a description of the input A/D conversion and digital color decoder. The SAA7186 resizer connects directly to the digital YUV outputs of the SAA7191B or the SAA7151B decoders. Other signals such as Vsync, Href, and clocks are shown connected on page 8 of the schematic. An expansion port at J9 is provided that will mate with the DTV7199 demo board and provides a direct connection to the SAA7191B digital decoder data bus if necessary. Headers JP4-JP7 provide access to all pins of the SAA7186 for measurement purposes. U43 provides clock buffering if external signals are applied at J9. Standalone operation requires U43 to be removed and jumpers installed at JP14 of page 1 of the schematic. Clock generator U40 must be removed if external clocks are being used.

SAA7186 RESIZER AND MEMORY ENCODING

The function of the SAA7186 is to filter and reduce the number of pixels per line and lines per field coming from the digital decoder SAA7191B. The SAA7186 contains 2 full bandwidth YUV line stores for vertical filtering, horizontal filters, a chroma keyer, color space converter, and resizer logic. It is operated in "TEST" or "TRANSPARENT" mode, such that all pixels and lines are passed through the output fifo. A pixel qualifier at pin 100 called PXQ is the only signal needed to decide which data to write into memory. Note that VCLK on pin 51 is the system pixel clock inverted to insure proper operation of the fifo interface during "TRANSPARENT" mode. The output fifo must not be operated in phase with incoming pixel data from the decoder! The color space converter is bypassed to make use of only 16 bits for YUV memory storage.

The logic on page 4 shows that the luminance channel (Y[0 . . 7]) from the decoder is not passed directly to memory, but can be altered to contain special control codes. Chroma Key (ALP) encodes a 00H, End Of scan Line (EOL) encodes on 01H, and End Of Frame (EOF) encodes on 02H. The UV bus (UV[0 . . 7]) is only passed through a buffer to match the delay of the Y channel for timing purposes and buffering to memory. U29A generates an extra memory write cycle after every line to add an EOL marker in memory. If the Chroma Key function is active from the SAA7186 resizer, then 00h is stored in memory on a pixel by pixel basis. Vsync encodes 02h at any time to insure that an EOF marker is placed in memory. Memory is not written if PSTILL at U31 pin 8 is high. The image is frozen in memory is this case. The SAA7186 will not send data values out on the luminance bus less than 10H, therefore, the selected control codes are unique for this design.

READ WINDOW GENERATOR

The schematic shows on page 3 that luminance data from memory (OY[0 . . 7]) is checked for special control codes that were added on the input side only after a proper vertical line delay from U24 and U23 and horizontal delay from U21 and U19. These devices set the upper left corner of the displayed resized image. Comparitors U14, U16, and U17 check the luminance data for control codes. Their outputs are reregistered via D flip flops and control the status of HOKN at U18 pin 8 and VOKN at U22 pin 6. These signals are low only when the resized image is being displayed. U22B pin 9 is low on any pixel within the resized image that matches the chroma key color programmed in the SAA7186. Chroma Key can be disabled by setting limits out of range, such as lower limits at the maximum values.

It should be mentioned that U18A and JP2 establish the correct UV phase relationship of the resized picture. Resolution for picture start is limited to every other pixel with JP2 setting the correct phase. It should also be mentioned that the luminance data bus (OY[0 . . 7]) is encoded to 10H whenever memory is not driving the bus in order to force black data values for the SAA7199 encoder. The memory only stores data for the resized picture in a serial fashion. The output picture will be black except for the resized image if it is being displayed.

The simple method of adding control information to the data that is written to memory makes a very simple output window generator possible. Only the upper left corner must be programmed for display. The SAA7186 can be programmed for any size picture from full size to 1 pixel without restriction, and the correct size will automatically be displayed in a window.

DIGITAL ENCODER AND OUTPUT

If the DTV7186 demo board is installed on top of a DTV7199 demo board, then the background picture can come from the decoder input on the DTV7199 board. Page 6 of the schematic shows the connection bus at JP3. Multiplexers U25, U26, U27, and U28 are controlled via PIPSELN and PIPSEL which select data from JP3 of the resized picture. The data bus on the left hand side of JP3 is also encoded with pull-up and pull-down resistors so that black data will be sent to the SAA7199 encoder if external data is not available.

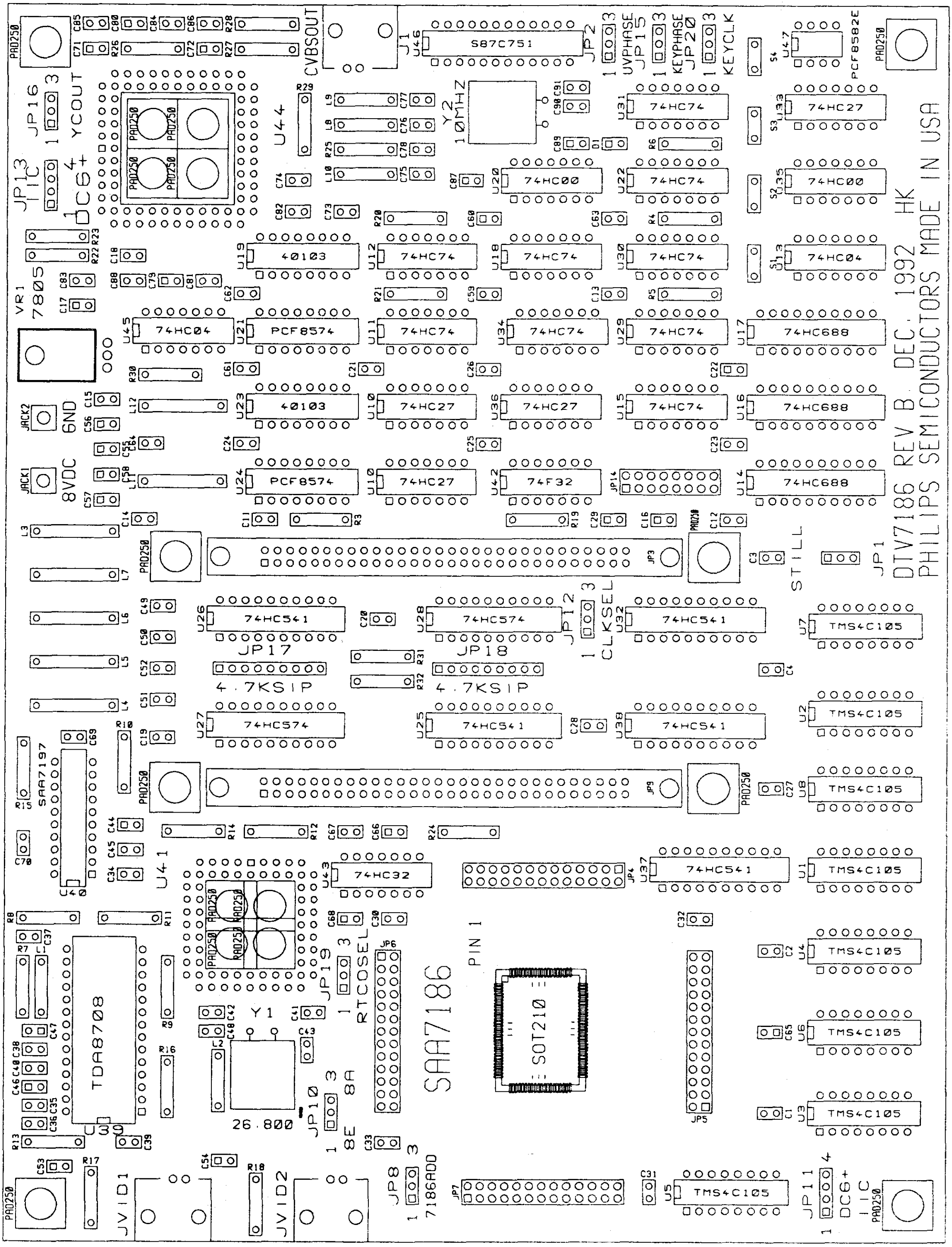
Finally, Hsync, Href, clock, and YUV data is sent to the SAA7199 encoder for modulation and D/A conversion back into composite video again. The SAA7199 encoder must be operated and programmed for "RTC" operation. This means that the clocks and sync from the SAA7191B digital decoder and a special signal called RTCO are supplied to the encoder to maintain sync and color lock to the input video signal. A modification to this design might be to add the SAA7197 clock generator and TDA8708 A/D converter to the SAA7199 for genlock. In this case, "RTC" mode is not necessary.

DTV7186

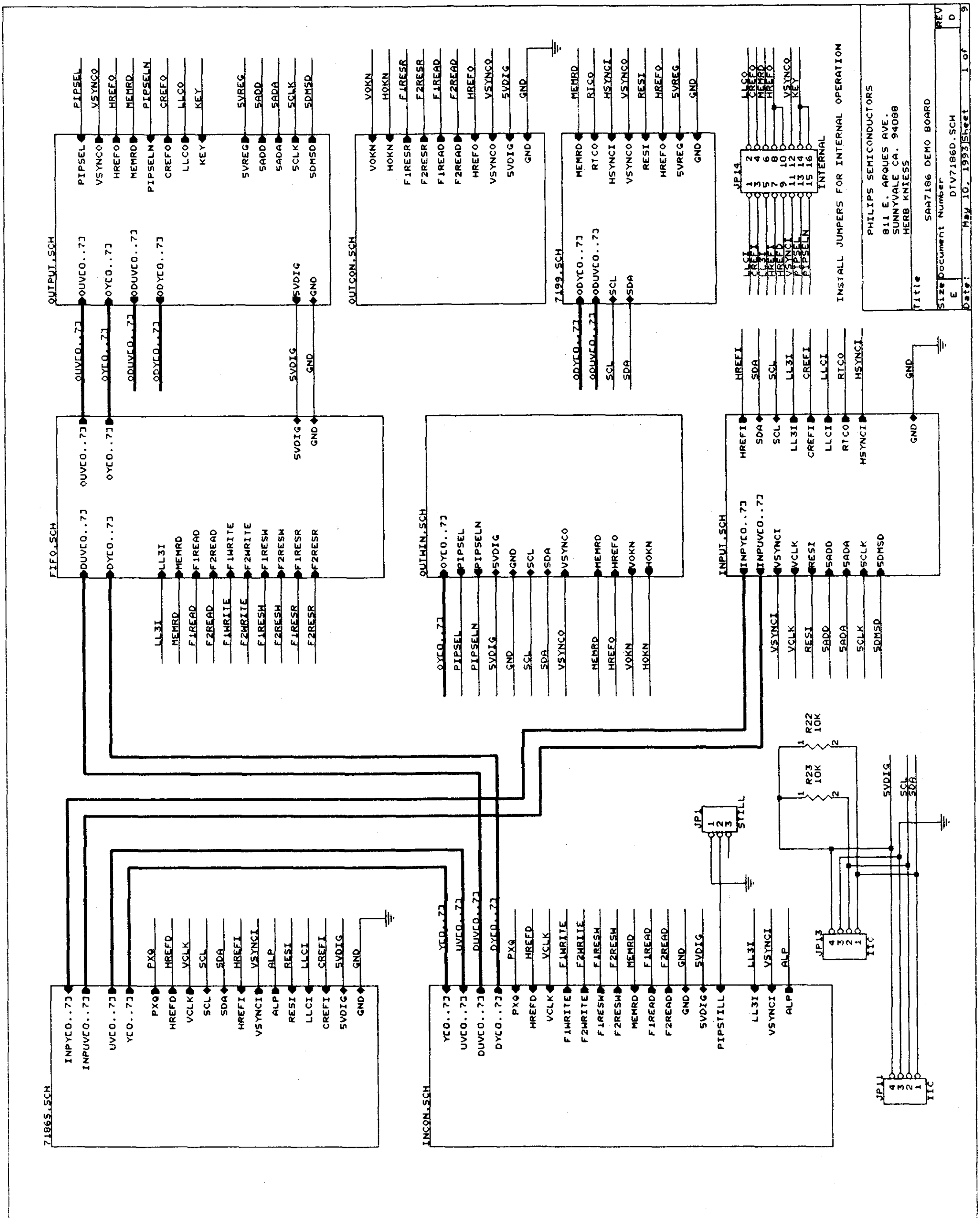
SAMPLE PROGRAMMING FOR SAA7186, SAA7191B, SAA7199B

SAA7186		SAA7191B	SAA7199B	index=02
92H	SUB ADD 00H	5DH	A6H	sub add=00
D0H		7EH	00H	
80H		53H	00H	
12H		43H	00H	
28H		19H	C4H	
50H		00H	20H	
F0H		39H	52H	
10H		00H	26H	
60H	SUB ADD 08H	7FH	10H	
00H		7FH	05H	
00H		7FH	00H	
00H		7FH	00H	
50H		00H	00H	
A8H		88H	01H	
6CH		78H	0CH	
B4H		7CH		
0EH	SUB ADD 10H	00H		
		1EH		
		00H		
		00H		
		36H		
		09H		
		FCH		
		D1H		
	SUB ADD 18H	ECH		

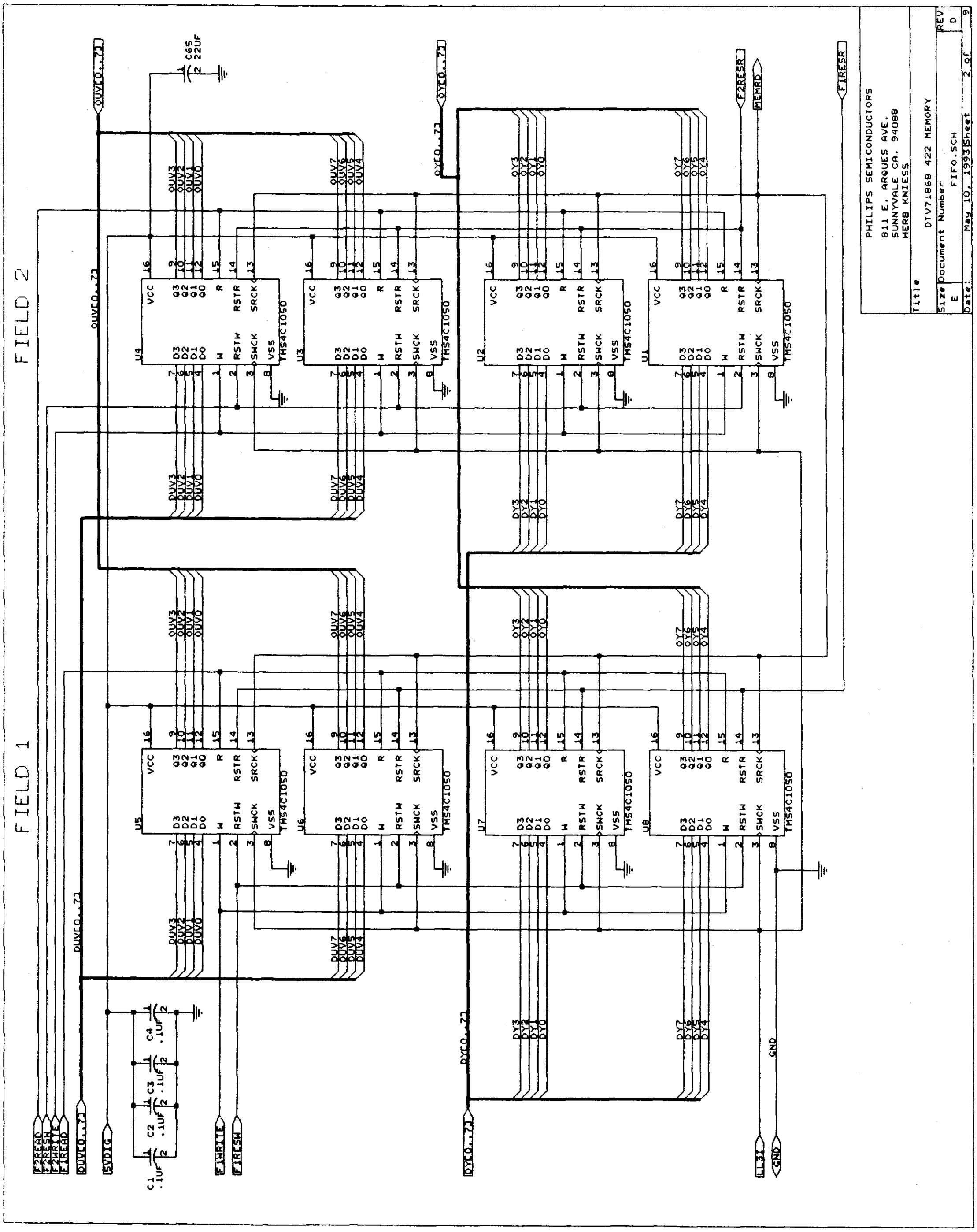
DTV7186


CVBSOUT
YCOUT
JP16
JP13
IIC
DC6+
S87C751
JP2
UVPHASE
JP15
KEYPHASE
JP20
KEYCLK
PCF8582E
Y2
10MHZ
74HC74
74HC27
74HC00
74HC04
40103
PCF8574
74HC688
74F32
VR1
7805
6ND
8VDC
JACK1
JACK2
JP3
JP9
STILL
JP1
JP12
CLKSEL
74HC541
74HC574
JP17
JP18
4.7KSIP
TMS4C105
SAA7197
U41
74HC32
TDA8708
U39
JP4
JP5
JP6
JP7
JP8
7186ADD
PIN 1
SOT210
SAA7186
JP19
RTCOSEL
JP10
8A
8E
Y1
26.800
JVID1
JVID2
JP11
DTV7186 REV B DEC. 1992 HK
PHILIPS SEMICONDUCTORS MADE IN USA

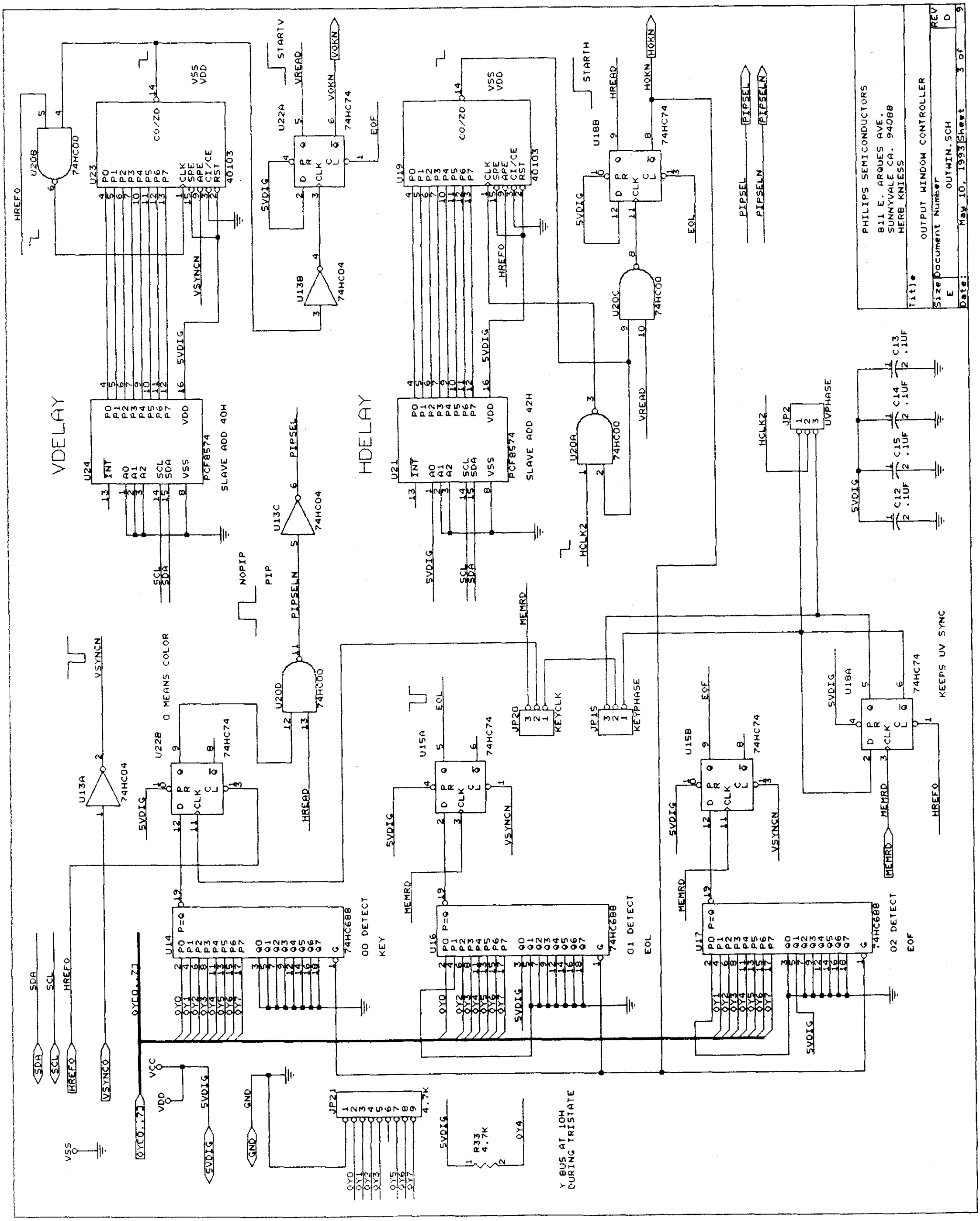
DTV7186


PHILIPS SEMICONDUCTORS
811 E. ARQUES AVE.
SUNNYVALE CA. 94088
HERB KNIESS
SAA7186 DEMO BOARD
DTV7186D.SCH
May 10, 1993
REV D
INSTALL JUMPERS FOR INTERNAL OPERATION
OUTPUT.SCH
OUTCON.SCH
7199.SCH
FIFO.SCH
OUTWIN.SCH
INPUT.SCH
7186S.SCH
INCON.SCH

DTV7186


FIELD 2
FIELD 1
U1
U2
U3
U4
U5
U6
U7
U8
TMS4C1050
VCC
Q3 Q2 Q1 Q0
R
RSTR
SRCK
D3 D2 D1 D0
W
RSTW
SWCK
VSS
OUVC0..7]
OYC0..7]
DUVC0..7]
DYC0..7]
F2RESR
MEMRD
F1RESR
F2READ
F2RESW
F2WRITE
F1READ
5VDIG
F1WRITE
F1RESW
LL3I
GND
C65 22UF
C1 .1UF
C2 .1UF
C3 .1UF
C4 .1UF
PHILIPS SEMICONDUCTORS
811 E. ARQUES AVE.
SUNNYVALE CA. 94088
HERB KNIESS
Title
DTV7186B 422 MEMORY
Size E
Document Number FIFO.SCH
REV D
Date: May 10, 1993
Sheet 2 of 9

DTV7186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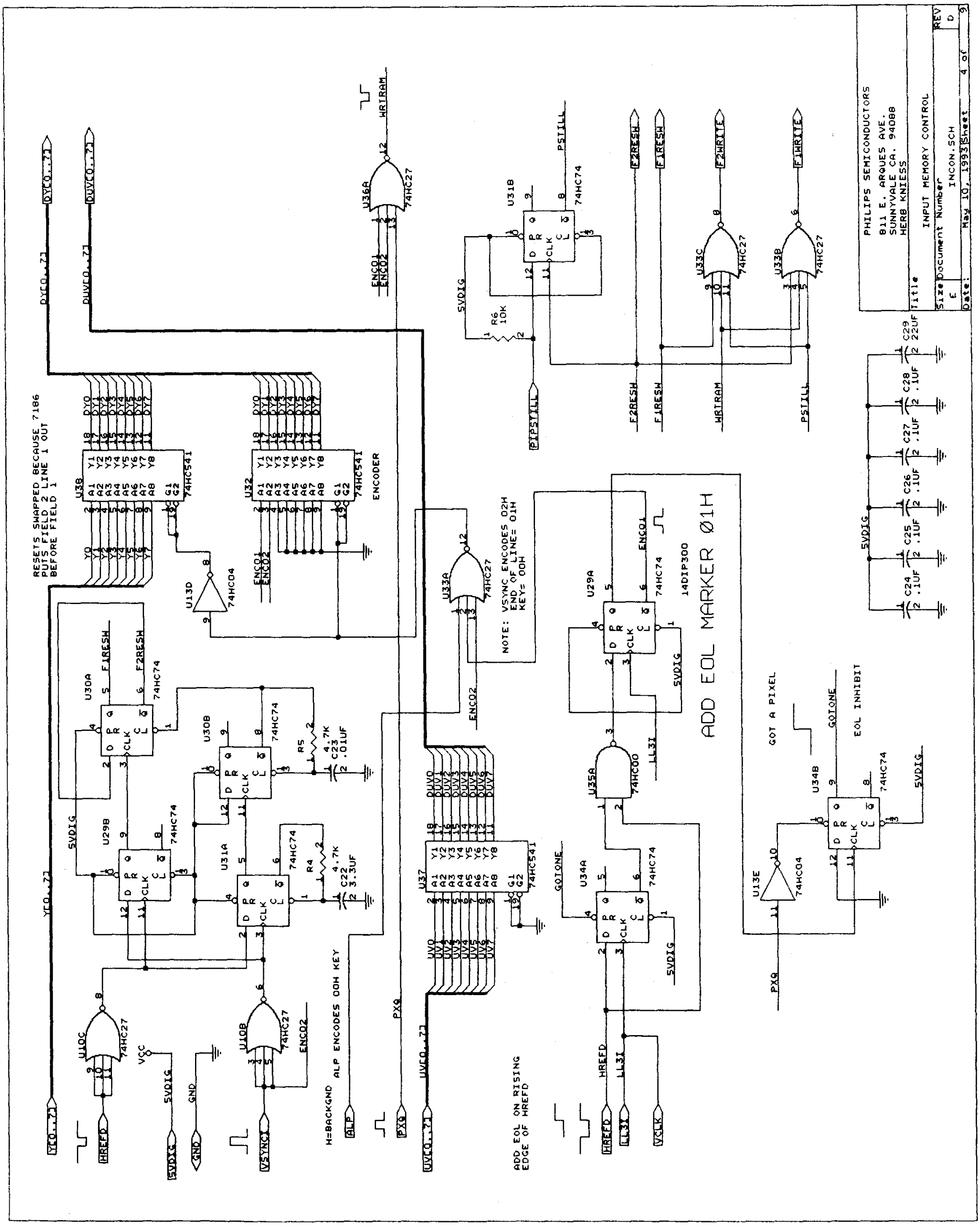
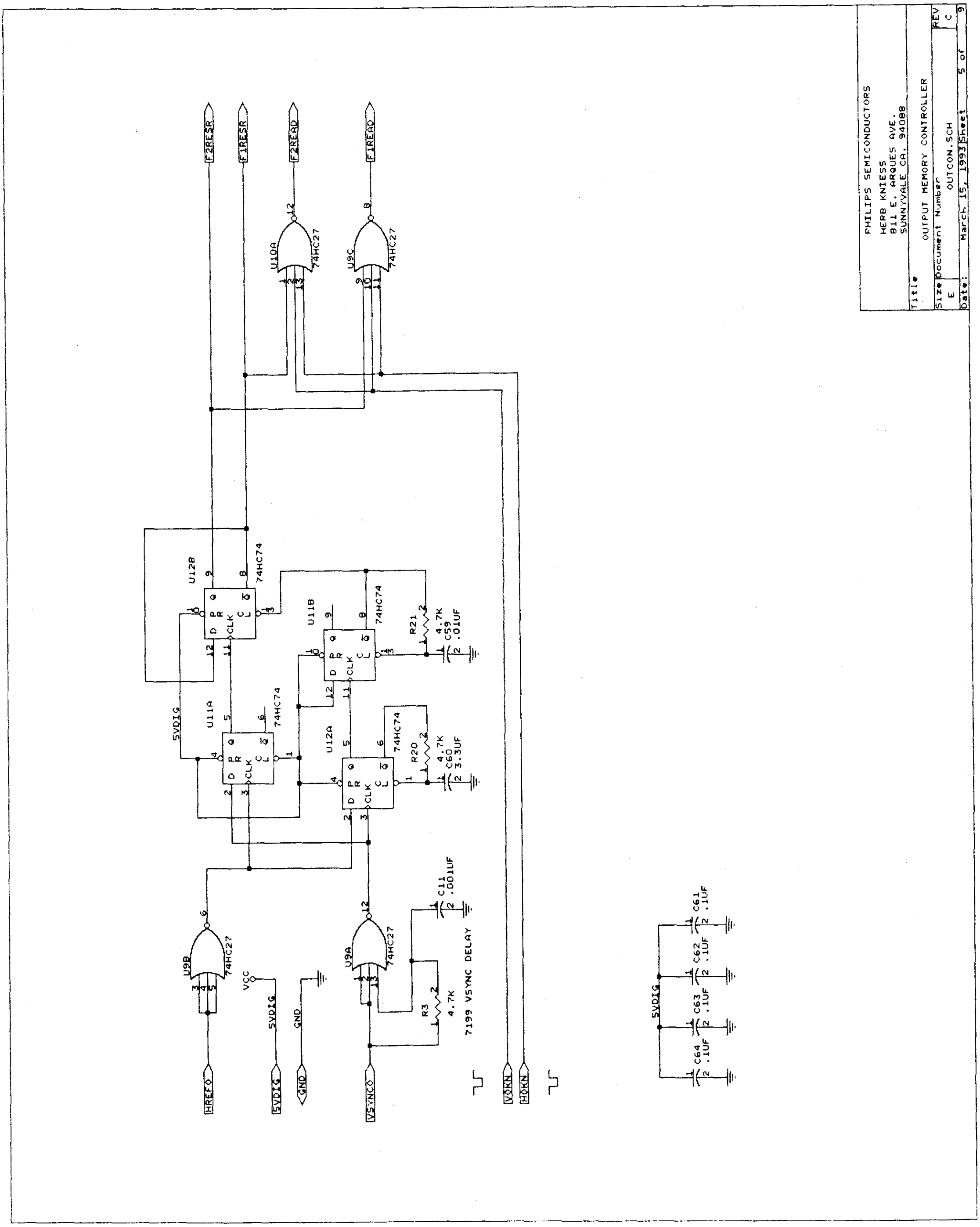
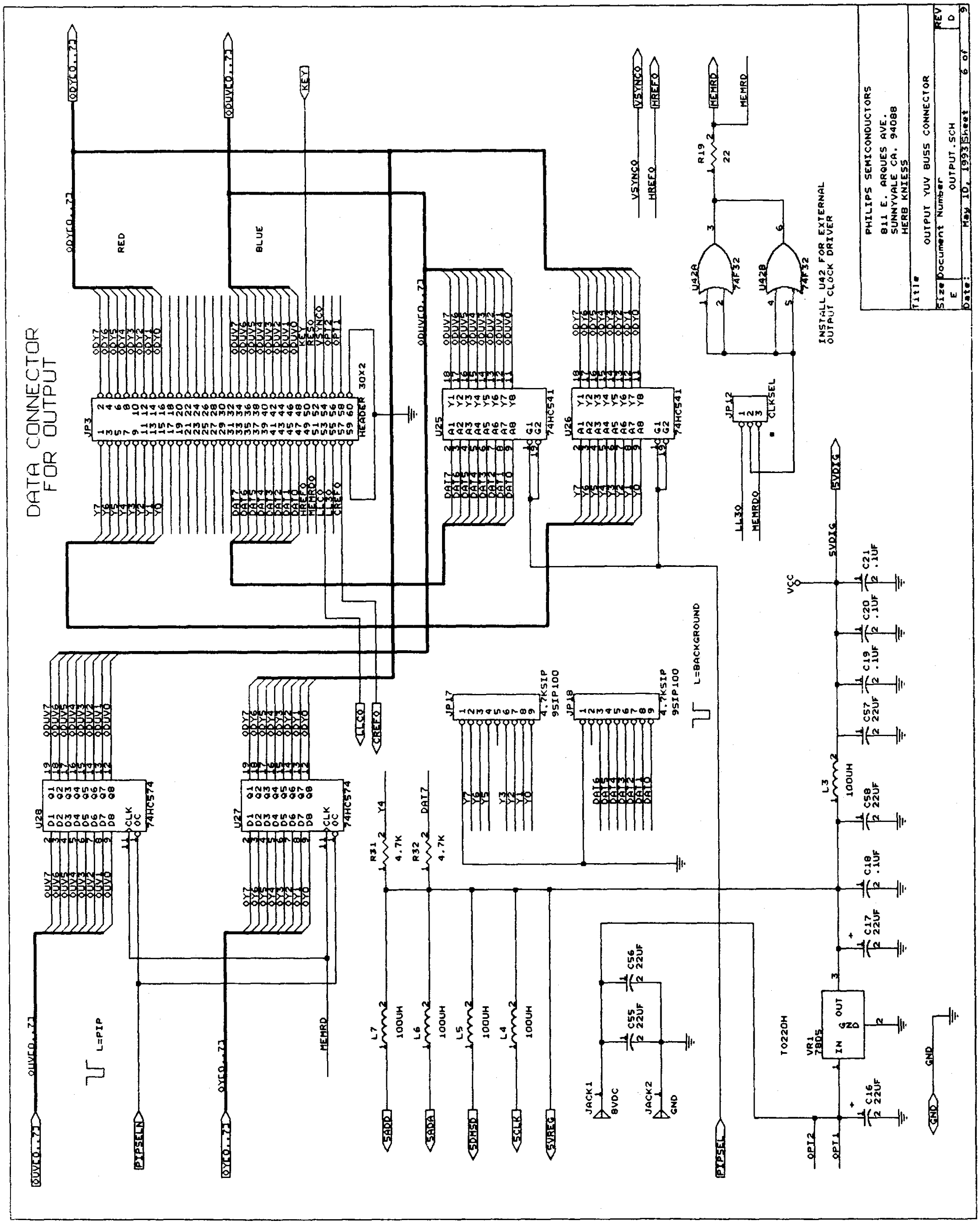
811 E. ARQUES AVE.
SUNNYVALE CA. 94088
HERB KNIESS
Title
OUTPUT WINDOW CONTROLLER
Size E
Document Number
OUTWIN.SCH
REV D
Date: May 10, 1993
Sheet 3 of 9
VDELAY
HDELAY
SLAVE ADD 40H
SLAVE ADD 42H
00 DETECT
KEY
01 DETECT
EOL
02 DETECT
EOF
0 MEANS COLOR
KEEPS UV SYNC
Y BUS AT 10H
DURING TRISTATE
NOPIP
PIP

DTV7186

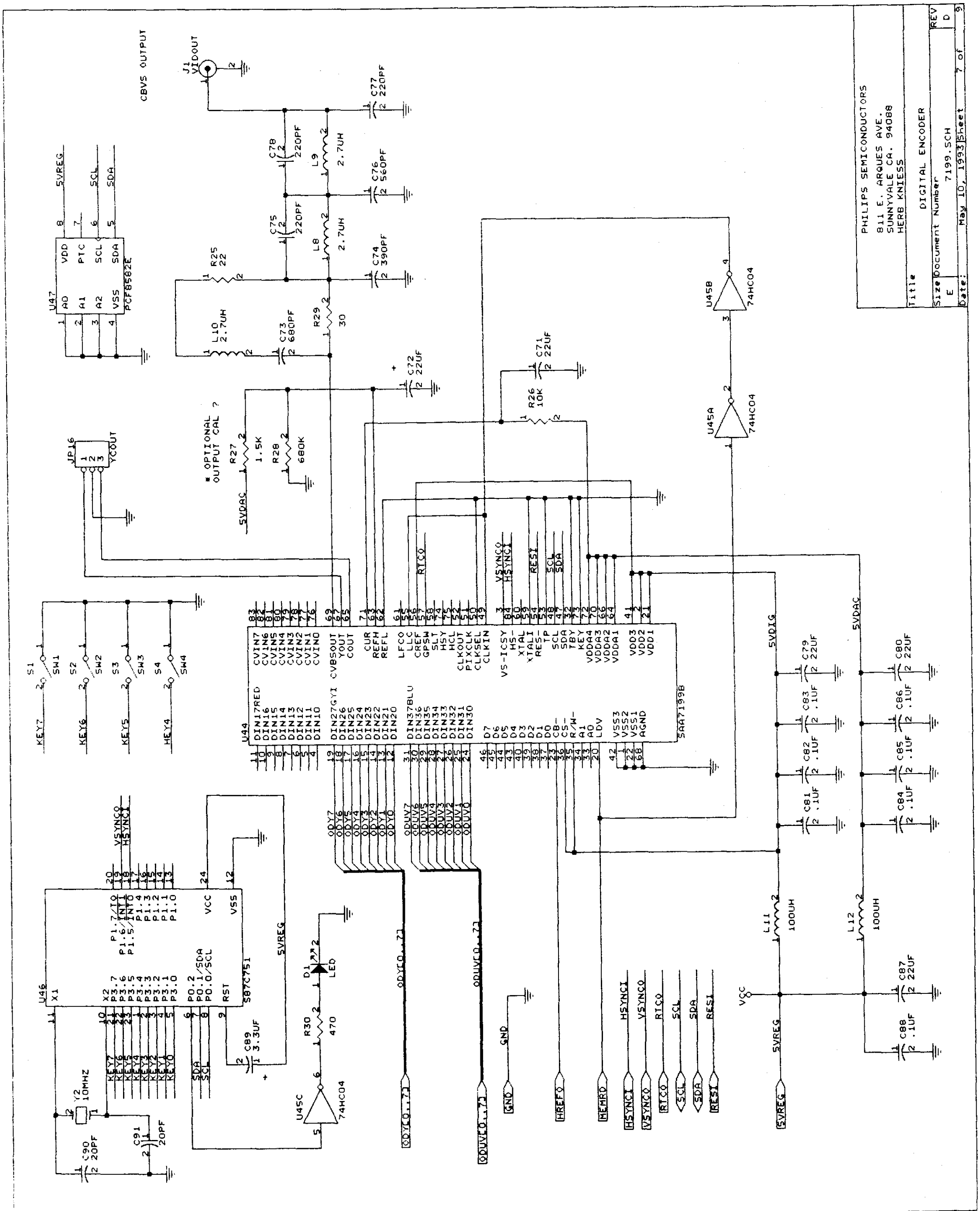

PHILIPS SEMICONDUCTORS
811 E. ARQUES AVE.
SUNNYVALE CA. 94088
HERB KNIESS
INPUT MEMORY CONTROL
INCON.SCH
ADD EOL MARKER 01H
NOTE: VSYNC ENCODES 02H END OF LINE= 01H KEY= 00H
ALP ENCODES 00H KEY
ADD EOL ON RISING EDGE OF HREFD
RESETS SWAPPED BECAUSE 7186 PUTS FIELD 2 LINE 1 OUT BEFORE FIELD 1


PHILIPS SEMICONDUCTORS
HERB KNIESS
811 E. ARQUES AVE.
SUNNYVALE CA. 94088
Title
OUTPUT MEMORY CONTROLLER
Size E
Document Number
OUTCON.SCH
REV C
Date: March 15, 1993 Sheet 5 of 9
F2RESR
F1RESR
F2READ
F1READ
U10A 74HC27
U9C 74HC27
U12B 74HC74
U11B 74HC74
U11A 74HC74
U12A 74HC74
R21 4.7K
C59 .01UF
R20 4.7K
C60 3.3UF
C11 .001UF
U9B 74HC27
U9A 74HC27
R3 4.7K
7199 VSYNC DELAY
VCC
5VDIG
GND
HREFO
VSYNCO
VOKN
HOKN
C61 .1UF
C62 .1UF
C63 .1UF
C64 .1UF

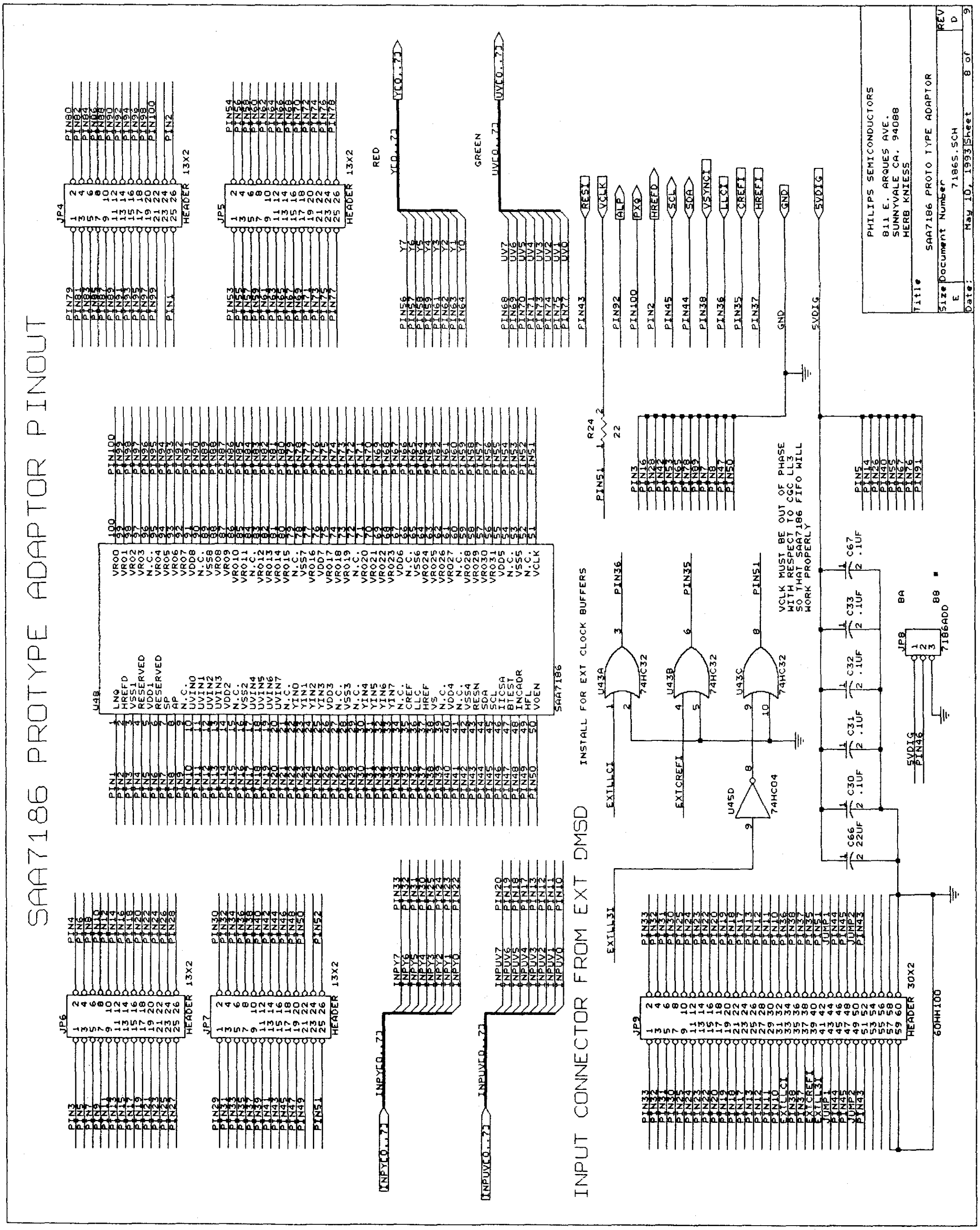
DTV7186


DATA CONNECTOR FOR OUTPUT
PHILIPS SEMICONDUCTORS
811 E. ARQUES AVE.
SUNNYVALE CA. 94088
HERB KNIESS
OUTPUT YUV BUSS CONNECTOR
OUTPUT.SCH
May 10, 1993
INSTALL U42 FOR EXTERNAL OUTPUT CLOCK DRIVER
L=BACKGROUND
L=PIP

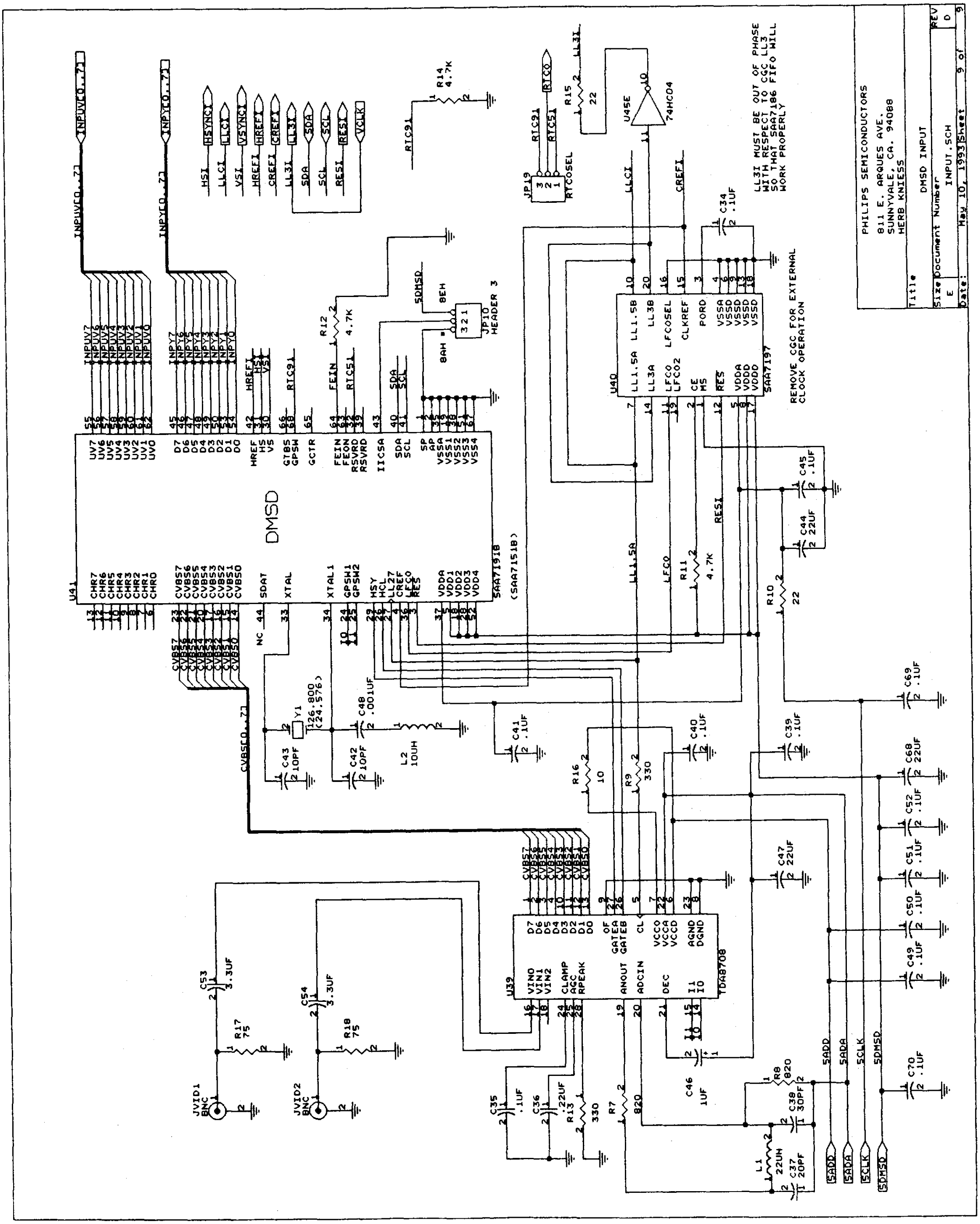
DTV7186


CBVS OUTPUT
PHILIPS SEMICONDUCTORS
811 E. ARQUES AVE.
SUNNYVALE CA. 94088
HERB KNIESS
Title
DIGITAL ENCODER
Size E
Document Number 7199.SCH
REV D
Date: May 10, 1993
Sheet 7 of 9

DTV7186


SAA7186 PROTYPE ADAPTOR PINOUT
INPUT CONNECTOR FROM EXT DMSD
INSTALL FOR EXT CLOCK BUFFERS
VCLK MUST BE OUT OF PHASE WITH RESPECT TO CGC LL3 SO THAT SAA7186 FIFO WILL WORK PROPERLY
PHILIPS SEMICONDUCTORS
811 E. ARQUES AVE.
SUNNYVALE CA. 94088
HERB KNIESS
Title
SAA7186 PROTO TYPE ADAPTOR
Size E
Document Number 7186S.SCH
REV D
Date: May 10, 1993
Sheet 8 of 9

DTV7186


PHILIPS SEMICONDUCTORS
811 E. ARQUES AVE.
SUNNYVALE, CA. 94088
HERB KNIESS
Title
DMSD INPUT
Size Document Number
E INPUT.SCH
REV
D
Date: May 10, 1993 Sheet 9 of 9
LL3I MUST BE OUT OF PHASE WITH RESPECT TO CGC LL3 SO THAT SAA7186 FIFO WILL WORK PROPERLY
REMOVE CGC FOR EXTERNAL CLOCK OPERATION
DMSD
SAA7191B
(SAA7151B)
SAA7197
TDA8708
74HC04

DPC7194 Evaluation Board

Author: Herb Kniess

OVERVIEW

The DPC7194 evaluation board is designed to demonstrate and evaluate the performance of the Philips SAA7194 digital multistandard decoder and resizer integrated circuit. It has been designed in a PC XT form factor so that it could be installed in a personal computer if necessary. The board will run standalone with external power supply and decode analog composite video into analog RGB and digital YUV or RGB. Data connectors are provided for any interface to the SAA7194 that an engineer might need in order to evaluate timing parameters or the overall performance of the device.

A Philips SAA7169 triple 10-bit DAC has been included so that an analog color monitor capable of displaying 15kHz horizontal video timing via a VGA 15-pin connector or conventional RCA phono jack can be connected as a display monitor. All Philips Digital Video processing devices use IIC serial communication for configuration. Therefore, the board also contains an 87C751 microcontroller to configure the board for standalone operation.

POWER SUPPLY

Pages 1 and 2 of the schematic show that +12V and +5V power can be provided from the PC bus if so desired. JP1 should be installed in position 2-3 for PC operation, and in position 1-2 for external power 8-12VDC. Total board current should be under 500mA.

CLOCK SELECTION

Page 3 shows the input section of the board. Special attention has been given to allow several modes of operation of the output fifo of the SAA7194. JP6-JP8, and JP14 can be configured for different clock timings and operational output modes of the SAA7194 fifo. For RGB output mode using the SAA7169 DAC, JP14 should be in position 1-2, and JP6, JP7, and JP8 should be left open. U9A provides clock inversion to keep the output fifo operational in transparent mode so that the DAC receives constant data. On page 4, JP15 should be installed to force Black video during blanking time for analog RGB output. U9B gates the output fifo to tristate during blanking time if JP15 is installed.

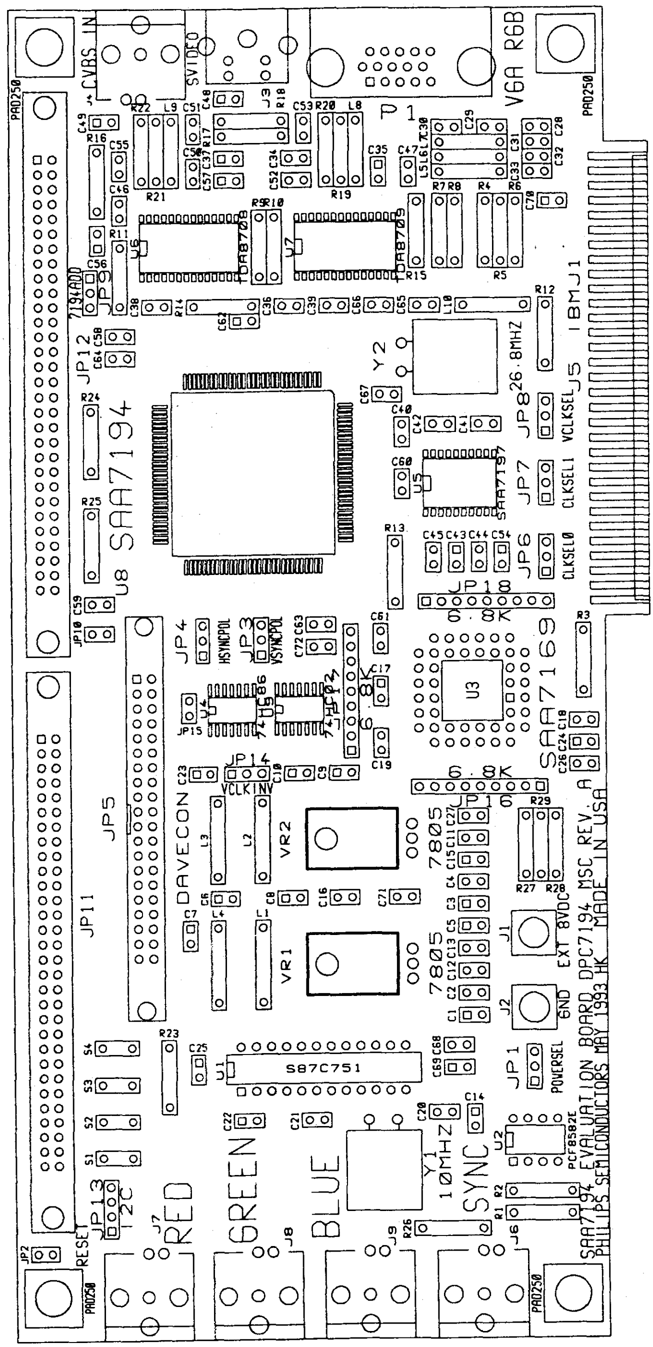
RGB OUTPUT

The SAA7169 DAC receives VCLK from the input section and 24-bit RGB data from the output fifo port of the SAA7194. On page 5, you can see that JP16, JP17, and JP18 provide hex values of 10H if the fifo is in tristate mode during blanking time. Normally, blanking time is kept at black levels to provide a reference for color monitors. Picture information is any value greater than 10H on the RGB data bus feeding the SAA7196 DAC. The low pass filters on pins 1, 3, and 43 of the DAC provide a 5MHz lowpass at 75Ω for the analog outputs. RGB and sync is sent to VGA connector P1 and to individual RCA connectors shown on page 6. Vertical and horizontal sync polarity can be selected on JP3 and JP4 for the VGA connector. Composite sync is negative going on for RCA outputs.

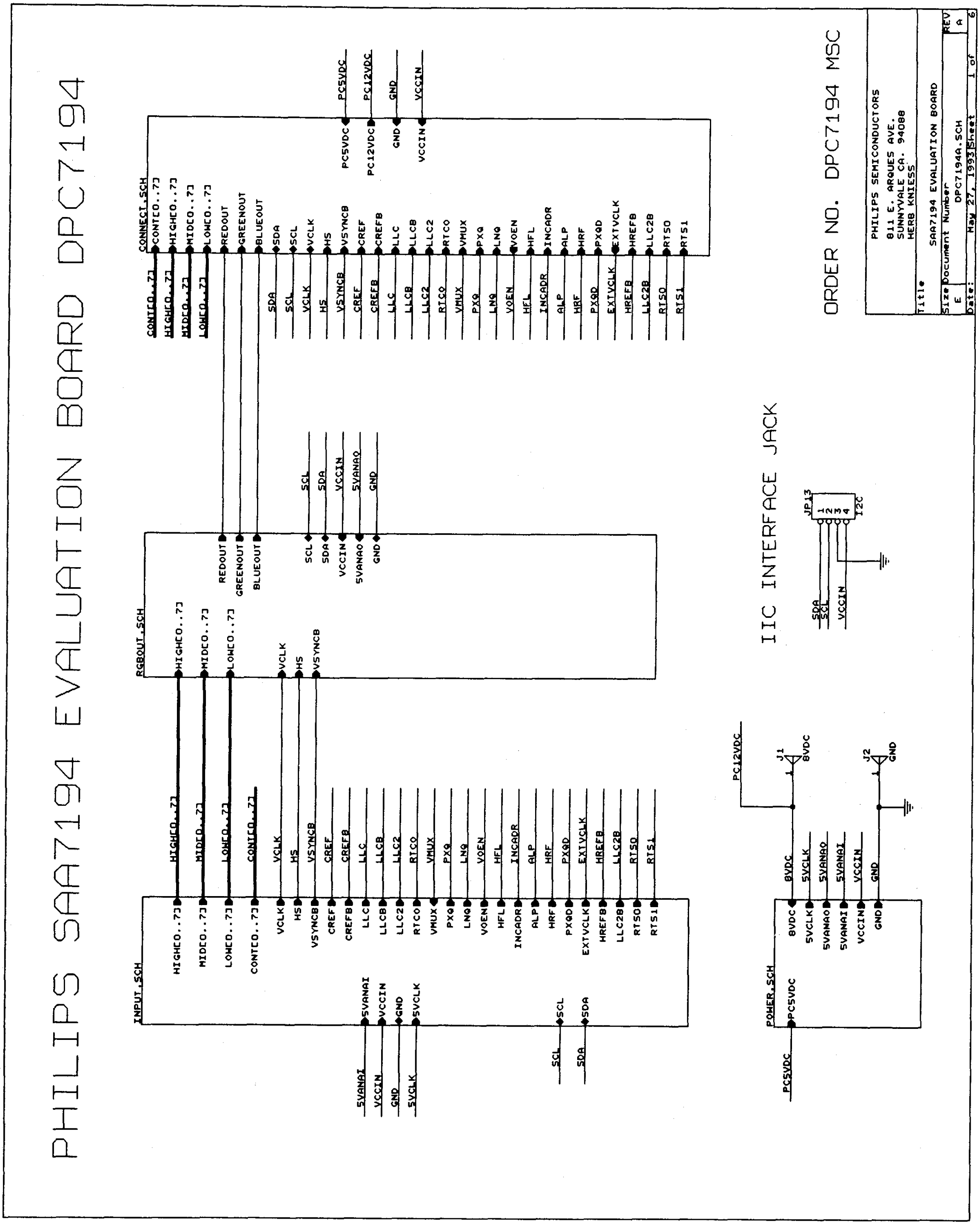
DIGITAL OUTPUTS

JP11 and JP12 provide access to all interface pins of the SAA7194 output fifo. Care must be taken to insure that only one source of clock drive is supplied at a time. Do not supply clocks to the digital output connectors unless JP6, JP7, JP8 and JP14 are properly configured on page 3.

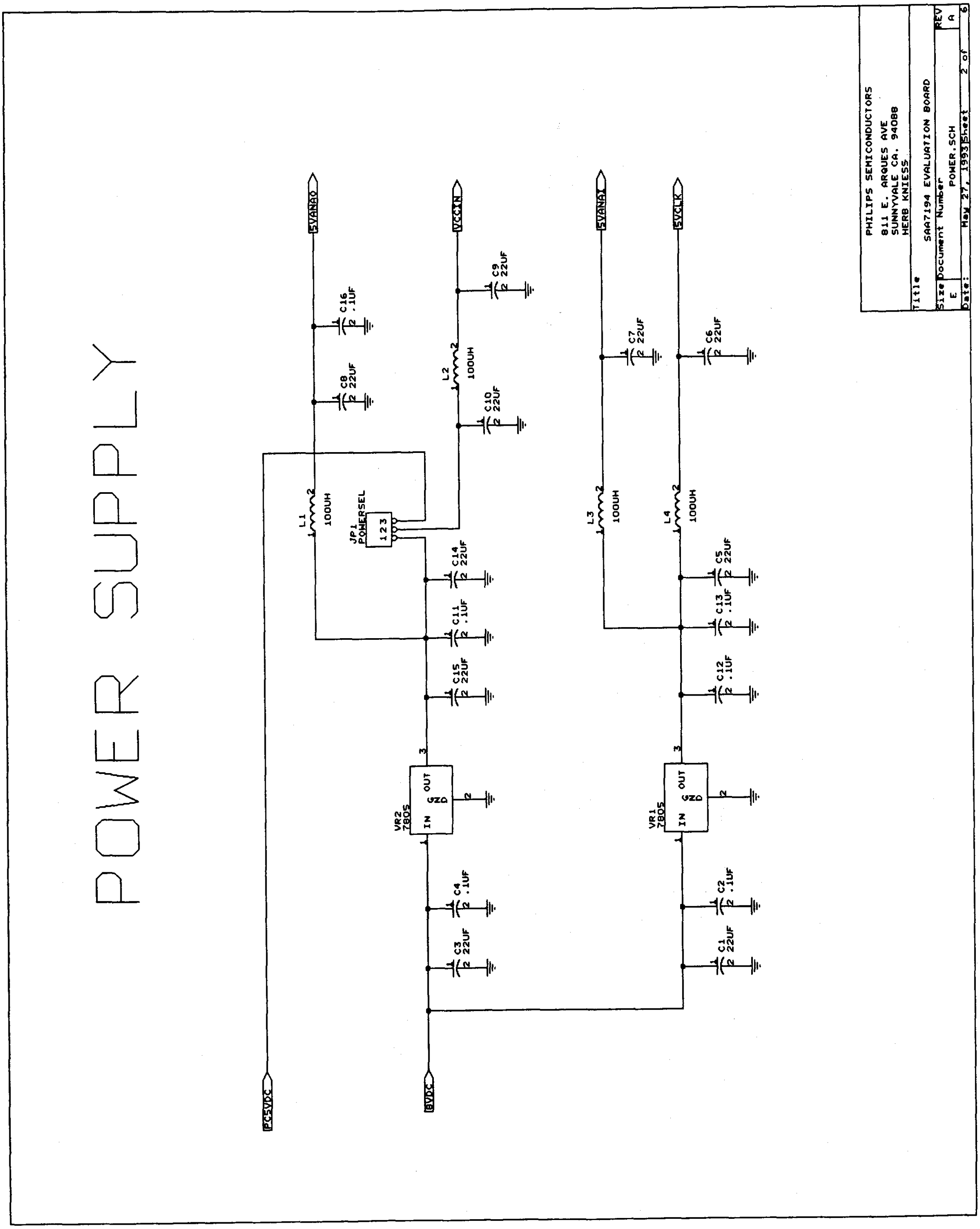
DPC7194 Evaluation Board



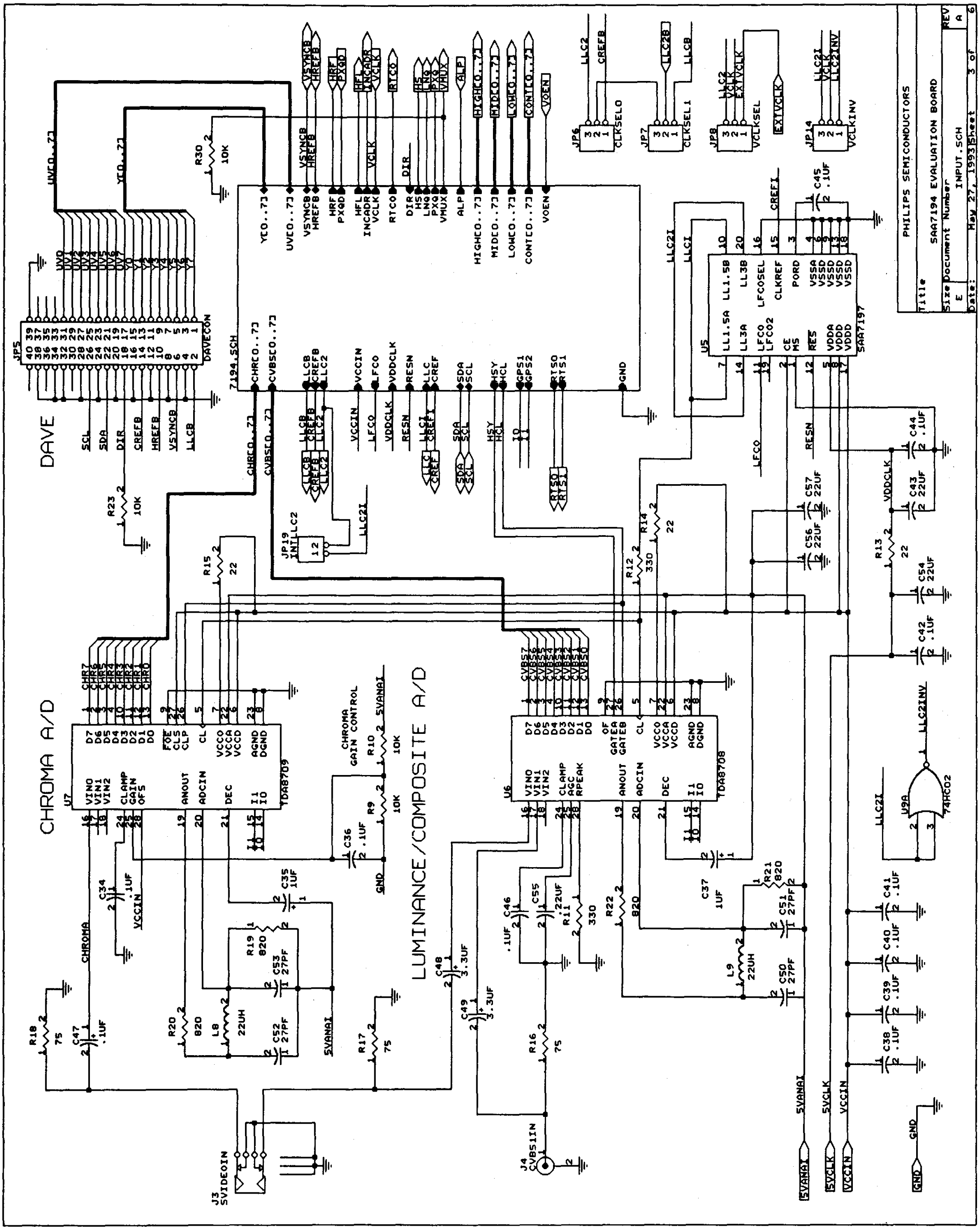
DPC7194 Evaluation Board



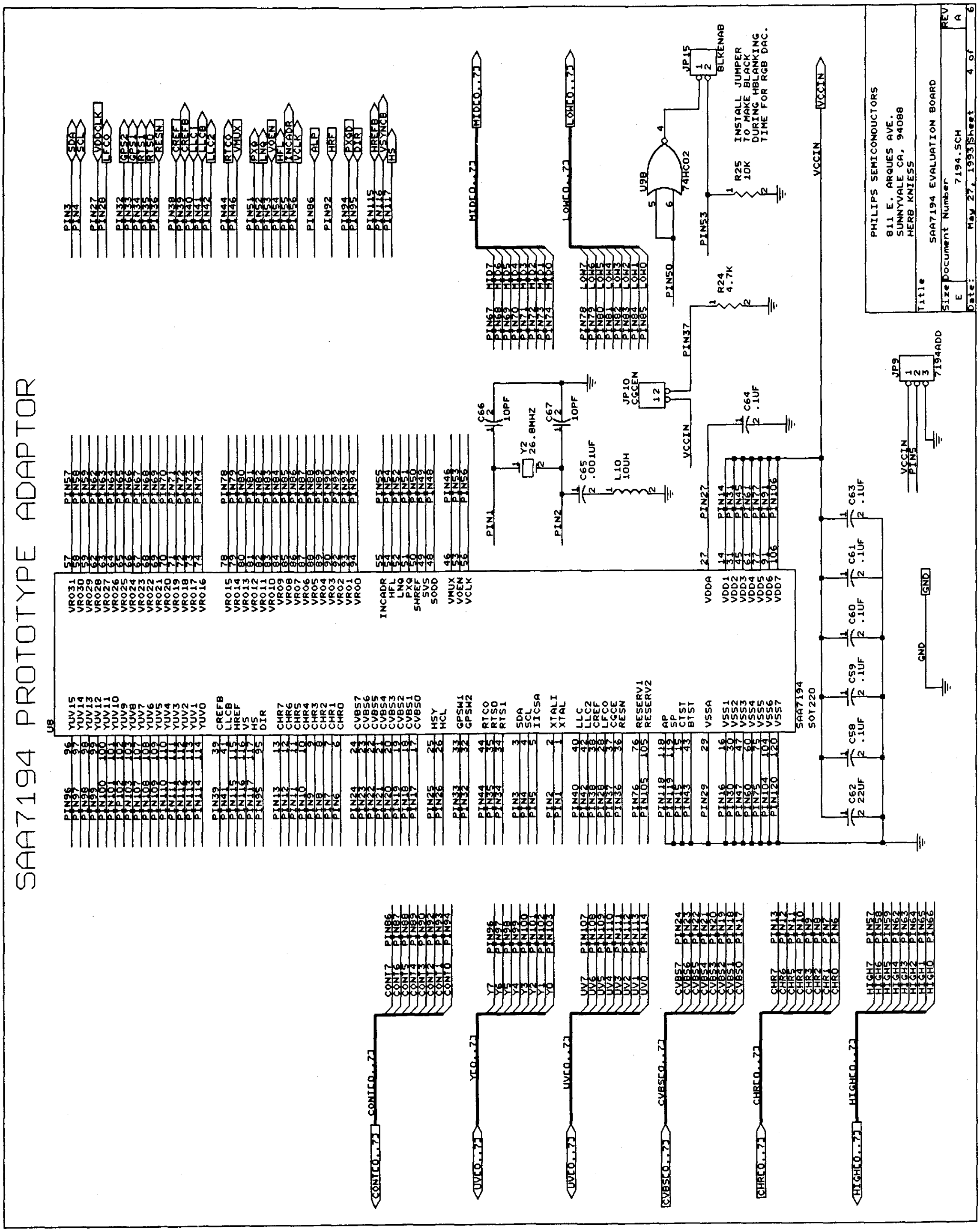
DPC7194 Evaluation Board



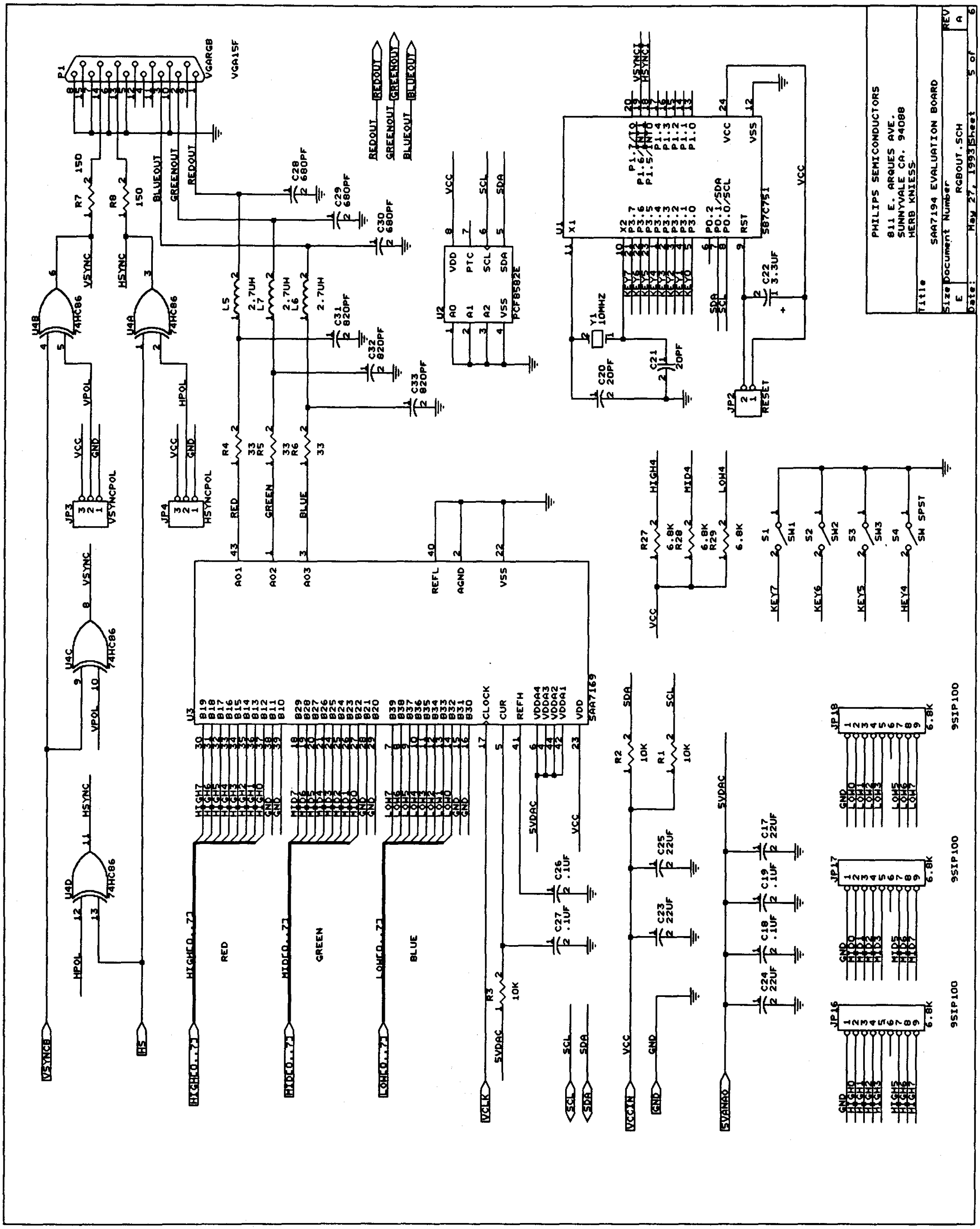
DPC7194 Evaluation Board



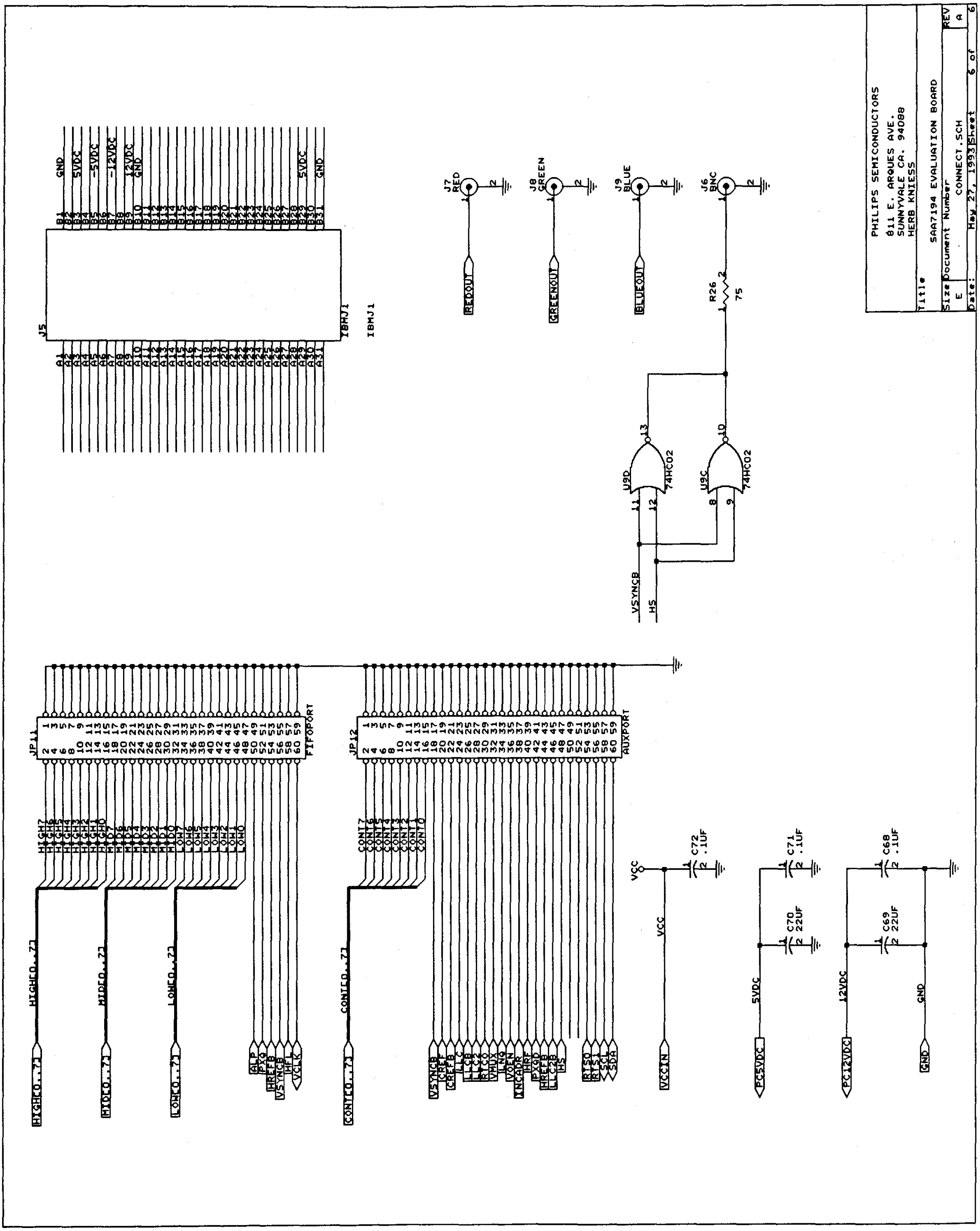
DPC7194 Evaluation Board



DPC7194 Evaluation Board



DPC7194 Evaluation Board



Desktop video demo board DTV7194

Author: Leo Warmuth

OVERVIEW

The DTV7194 demo board shows the system concept of Philips desktop video ICs. The main video processing functions incorporated in the demo board, are:

1. Video capture with multistandard decoding
2. Standardized digital video signal interface
3. Digital scaling
4. Frame buffer and related control
5. Video encoding
6. DACs and RGB conversion.

The DTV7194 demo board features the following Philips desktop video ICs:

TDA8708	8-bit ADC for CVBS and Y
TDA8709	8-bit ADC for CVBS and C
SAA7194	Digital true multistandard decoder—NTSC, PAL, and SECAM; horizontal and vertical scaling with filtering in both horizontal and vertical domains; control function for brightness, contrast, and saturation; expansion port I/O
SAA7197	Clock generator
SAA7199B	Digital NTSC/PAL encoder
SAA7169	Three channel ADC (RGB)
SAA7165	DAC for YUV 4:2:2 with peaking; color and transient improvement
TDA4686	High-speed YUV-RGB matrix with switch and control functions

The demo board also uses the following Philips ICs with general purpose functions:

PCF8574	I²C serial-to-parallel interface
PL22V10	Programmable Logic Device (PLD)
PLC42VA10	PLD
PML2552	PLD
87C054	Microcontroller (MTV), I²C controller, character overlay generator
PCF8582E	EEPROM with serial I²C interface
82B715	I²C booster

This document focuses on the functionality and interfaces of the new highly integrated video capture IC SAA7194, also called DESC:

- Digital multistandard decoder (NTSC, PAL, SECAM)
- Expansion port with standardized digital video interface, CCIR oriented, YUV
- SCaling with programmable filter in horizontal and vertical direction for anti-aliasing and asynchronous FIFO buffer for easy memory interface.

In addition, a memory controller is described, realized by means of PLDs, which demonstrates both scaler output interface modes: synchronous (transparent) and asynchronous (FIFO) operation. The problem of conversion from interlaced to non-interlaced video signal and vice-versa is addressed, too.

The appendix shows all the schematics and listings of the PLD programming, i.e., logic equations and state machine definitions.

FRONT END

The front end, with the analog-to-digital converters TDA8708 and TDA8709, includes automatic clamp and gain control. This circuitry is identical to the front end processing used for SAA7191 and SAA7151. For a more detailed description, please refer to the application note "DTV7199 Digital Television Demonstration System," p. 2-72. The application, including the programming model for the decoder part of the SAA7194, is very similar to that of the SAA7191.

THE PORTS OF THE SAA7194

Adaptor

The layout of the DTV7194 demo board provides a ring of through-hole measurement points around the 120-lead quad flat pack (QFP) package. This layout enables the signals at each pin to be probed.

Expansion Port

The expansion port of the SAA7194 is a bi-directional digital video signal interface with YUV and 4:2:2 sampling scheme. The signal format, i.e., the meaning of the code values, is based upon CCIR recommendation 601. The expansion port carries three types of signals:

- 16-bit wide YUV data
- synchronization signals, HREF and VS
- LLC and CREF clock signals.

These signals can be selected independently as input or output by means of the I²C bus. The direction pin DIR can switch the data stream on a pixel-by-pixel basis.

The expansion port taps the signal path between the decoder part and scaler part of the SAA7194. The expansion port interface, as output, looks exactly like the output of the SAA7191, and is compatible. As input, the expansion port feeds the scaler part of the SAA7194. As input, it can share its timing with the decoder part, or it can provide its own timing signals, including clock, even if it is asynchronous to the line locked clock of the decoder part. In the latter case, the decoder part, together with the analog front end (ADCs) and CGC, determines its clock and stays locked to the incoming analog CVBS or Y/C signal.

The signals of the expansion port are brought onto a separate connector called DAVE. The two I²C signals are also provided. The connector is prepared for a ribbon cable connection, input or output, and support interface to other video signal processing devices, e.g., for compression or decompression, video conference.

Scaler output port

The scaler output of the SAA7194 has—depending on the chosen data format—up to 32 data lines in the VRO port. The SAA7194 provides various RGB, YUV, and gray-scale data formats at the VRO scaler output port. The circuitry of the DTV7194 demo board supports the two formats:

- RGB 24 bits in 4:4:4 sampling scheme
- YUV 16 bits in 4:2:2 sampling scheme, one pixel at a time.

The color key 'alpha-bit' is available and used in both formats. The demo board does not utilize the 2-pixels-per-longword formats, which are provided by the SAA7194 for wider memory organizations, which would enable very-high-speed read pixel rates at the display side.

The scaling output port of SAA7194 has two interface modes:

- the asynchronous FIFO mode
- the synchronous transparent mode.

The DTV7194 demo board works in both interface modes.

In the asynchronous FIFO buffer mode the SAA7194 operates with a FIFO 16 words deep and up to 32 bits wide, and provides the signals:

- HFL, the 'half-full-flag', indicates that the device has at least 8 valid words in the output FIFO
- INCADR, the 'increment-address' signal, indicates—together with HFL—that the memory controller should increment line and/or field pointer

and requires the signals:

- VCLK, a gated clock burst, as answer to a request by HFL to empty the FIFO
- VOEN, output enable signal, whose use is optional.

The operation of the FIFO mode requires that the memory controller provide a gated VCLK after an HFL request to empty, or partly empty, the FIFO. It is recommended to apply a burst of 8 VCLK pulses. The SAA7194 has already "preloaded" the output with the "next-to-deliver" signal before it requests a burst of VCLK. Then, the first VCLK rising edge clocks out the next following sample. VCLK is the clock which directly writes into memory or a register immediately following the DESC output.

For the synchronous, transparent mode the SAA7194 requires a continuous clock VCLK, synchronous to its scaler input, and delivers output data qualified by various valid and gate signals:

- PXQ: qualifying the actual pixel as valid
- LNQ: telling that this line (will) carry valid data
- HRF: delay compensated HREF signal
- HGT: enveloping that part of line selected for scaling
- VGT: enveloping that part of field selected for scaling
- O/E: identifying odd and even field.

Not all these signals are needed at the same time, but their availability may simplify the design of a memory controller, or make a system more flexible and capable. For example, the presence of the false-state of the line qualifier LNQ or vertical gate VGT informs the system that there will be, for a certain time, no HFL request, and the system may undertake other access to the memory.

The demo board DTV7194 is made to demonstrate both scaler output interface modes. As all pins of the SAA7194 are available on test points, the behavior of the concerned control signals can easily be observed. The control logic for both cases is embedded in a single PLD implementation. For the PLD programming, refer to the listings in the appendix. Some aspects of the logic equations and state machine structure are explained in the following section.

FRAME BUFFER

Concept for Frame Buffer Controller

The concept for the memory control on the DTV7194 demo board is guided by the desire to:

- maximize the usage of given memory capacity
- ensure synchronous scaling and display sizing
- support interlace/non-interlace conversion
- minimize the effort on control logic.

The solution has the following main components:

Serial Stream with embedded "Marker"
The video scanning technique maps the three-dimensional video stream into a one-dimensional, serial signal stream. But some markers are inserted as dummy pixels (not to be displayed), to signal when a line, field, or frame is complete. This stream is written into memory in a strict serial one-dimensional manner.

The start-time of the read process is controlled by given display raster coordinates, and then data is read until an end-of-line marker is found in the data stream (or an end-of-field/frame marker). The read process pauses and resumes again at given display raster coordinates.

Independent of the actual input picture dimensions, the memory can get filled up to the last pixel. There is no waste by incompletely filled rows. A change of input picture dimensions, e.g., changing of scaling factor, is immediately transported to the read and display window control by the signal stream itself.

CCIR-601 reserves the codes 00 hex and FF hex for synchronization purposes. The SAA7194 ensures that the signal stream does not use these codes. The DTV7194 demo board uses the code 00 hex as end-of-line marker (eol) and the code FF hex as end-of-field (eof) marker.

Alpha "Marker"
In an extension to this eol/eof marker concept the alpha bit (color key signal) is also encoded into the data stream by means of a special marker-code. The luminance value of that pixel, which should be keyed-out, is overwritten with a code, to be interpreted as 'transparent', i.e., as a pixel not to be displayed. This approach makes the need for an additional alpha bit plane in the memory obsolete, reduces memory requirements, and enhances memory efficiency.

The SAA7194—in FIFO mode—fills up unused FIFO burst words with dummy pixels. The fill values are coded with 01hex. The DTV7194 demo board uses this code as transparent pixel, or key marker, too.

Two Field Buffer Banks
The frame buffer memory is split into two banks, one for "odd" fields the other for "even" fields, respectively, "even" and "odd" lines. The address-pointer toggle from one bank to the other can be controlled independently for read and write processes. Conversion between interlace and non-interlace schemes can easily be performed.

An interlaced source writes the first field into the "odd" FBB, and the second field into the "even" FBB (field toggling). Reading for an interlaced display will access the memory in identical order. Reading for a non-interlaced output will "de-interlace" the stored two-field picture by reading from both FBB in a line-alternating fashion (line toggling).

A non-interlaced source writes its first line, and all odd lines, into the "odd" FBB, and the interleaving even lines into the "even" FBB (line toggling). Reading for a non-interlaced display will access the memory in identical order. Reading for an interlaced output will "interlace" the stored single frame into two fields by reading one field from the "odd" FBB, and then the other field from the "even" FBB in a field-alternating fashion (field toggling).

Serial Memory: FRAMs
Because the video data stream in this application is exclusively serial, FIFO-DRAM ICs are utilized for the frame buffer circuitry. These FRAMs don't need any addressing (which saves external address generation) and therefore significantly simplifies the control logic. But VRAMs or standard DRAM memory applications could also be used and would benefit by the "marker" control concept and two field buffer bank approach.

Byte Serial, Field Serial
Most of the commonly available memory ICs have an address space which is deeper than the number of pixels in a standard video field. The used FRAMs, for example, have 262144 storage locations. A regular NTSC field with 240 lines and 640 SQ-pixels per line results into 158600 pixels total, which is about 58% of the available memory address range.

An effective way to get higher memory utilization is to place the information belonging to one pixel into two memory addresses. The 16-bit wide YUV format is converted into two consecutive bytes (byte-serialized), like a D1 or CCIR-656 data stream. A similar memory device saving effect can be achieved by writing the two fields of an interlaced source into a single FBB, one after the other. Both approaches are supported as an option by the DTV7194 demo board.

It is obvious that then only 85% of a regular NTSC-SQP field or frame will fit into the given memory space. But this conflict can be resolved either by "cropping" only the interesting area of the field, i.e., throwing peripheral information away, or by "squeezing" the picture content into fewer pixels, i.e., scale somewhat down. Both methods can be combined and are supported by the scaling function of the SAA7194. Programming of source size determines the cropping function, Destination size, relative to source size, determines the scaling factor. Both source and destination size can be defined independently in horizontal and vertical dimensions.

The memory control function of the DTV7194 demo board is capable of demonstrating various methods of optimal memory usage and minimum control effort for different application requirements. Because the demo board combines various approaches in the same hardware, the circuitry itself may show a certain amount of overhead. The various algorithms are selectable via I²C programming. As the logic is embedded in PLDs, the circuitry offers a multitude of options (by re-programming the PLDs).

The following description will focus on the core functionality.

Functional Description and Partitioning

Frame Buffer

The frame buffer memory block consists of 12 FRAM ICs. The 24-bit RGB format with interlaced signal requires that capacity. A straight 16-bit wide YUV frame buffer requires only 8 FRAMs. With some restrictions in available picture size, a set of only 4 FRAMs is needed. To support only smaller picture sizes, e.g., CIF-format, the application requires just 2 FRAM ICs.

Write Interface

The schematic sheet WRITE.SCH shows the interface between the SAA7194 scaler output port VRO and the frame buffer. The PLD PLC42VA12 named WSYNCB works as clock divider, clock driver, and timing circuit, and takes care of the interface logic to serve the FIFO output mode of the SAA7194. But it can also be switched to operate for transparent mode.

For the FIFO mode, the input signals HFL and INCADR are used, and a burst of 8 VCLK cycles is provided. For the transparent mode, the input signals PXQ, HRF, and SVS are used. In both operation modes a unified set of control signals is sent to the second PLD. These control signals are closely related to the chosen frame buffer control circuit. The signals are:

- GATE gate signal = valid data at VRO-port
- EOL end-of-line flag, to insert an end-of-line marker
- EOF end-of-field flag, to insert an end-of-field marker. If both flags (EOL and EOF) occur together, an end-of-frame is signaled to reset the write address pointer
- FBBID field buffer bank ID, to control into which frame buffer bank the actual data needs to be written.

The second PLD PML2552, which is named WPATHB, is used mainly as a huge data bus multiplexer. The data streams for YUV format and RGB format are mapped into the frame buffer in such a way that its output busses can be used directly by the SAA7199, which can accept YUV as well as RGB formats. A third data bus is provided for the Red-signal, necessary for the 24-bit RGB format.

WPATHB further inserts the marker codes for EOL, EOF, and ALPHA into the data stream. It also generates the delay adjusted write enable (WE1 and WE2) and write pointer reset (RSTR) signals for the frame buffer.

For the details of the PLD programming, refer to the listings in the appendix. The different operation modes of the write control logic are programmable via I²C, and the serial-to-parallel converter IC PCF8574 at position U20 with I²C device slave address 42 hex.

Read Interface, Window

The schematic sheet WINDOW.SCH shows the read control logic. By means of two 8-bit words the horizontal and vertical start points of display window are defined, and present the scaled picture. If the display timing is synchronized to the expansion port, this signal can be chosen as background signal. In case the display (output) timing is determined by the SAA7199 digital encoder in master mode operation, then an artificial color bar test pattern is used as background signal. The combined signal is fed to the digital encoder and to two DACs for YUV-conversion (SAA7165) and RGB-conversion (SAA7186), and is also brought to a connector (JP7). It can also be multiplexed via this connector with an external signal by means of the MUTE control signal.

The PL22V10 PLD, named READCLKB, is mainly the function of a signal source selector and clock driver. The two PML2552 PLDs share the task to define the horizontal and vertical position (start point) of the window. READVB performs a vertical counter, counting in half lines. The vertical window offset is defined by VOS[8..1] via PCF8574 at position U34 with I²C device slave address 40 hex. The vertical starting trigger is sent from READVB to READHB in the form of the auxiliary signal FS-GO. FS-GO is a kind of delayed field-ID signal, changing its state in that line where the window should start.

READHB performs a horizontal pixel count. The horizontal window offset is defined by HOS[8..1] via PCF8574 at position U35 with I²C device slave address 41 hex. When both horizontal and vertical enabling signals are true, READHB will start reading from the frame buffer. The incoming data stream is checked for the relevant marker codes. If an end-of-line or end-of-field is detected, the read process is stopped until the next horizontal or vertical enabling signal, respectively. As the FS-GO signal carries the odd/even field ID, READHB can decide from which field buffer bank to read (RE1 or RE2).

The horizontal counter is also used to generate the auxiliary signal HS2RD, to be sent to READVH. HS2RD is a half-line indication signal, staying LOW for the first half line, and then HIGH for the second half line. This enables READVB to count vertically in half lines. Comparing the vertical sync edges of VSD with the state of HS2RD defines the output ID, i.e., display field ID, and when to reset the read address pointer. The vertical counter in READVB is also used to generate a luminance and color test pattern as background signal. Further, the video overlay control signals from the MTV microcontroller can be used to add foreground signals.

For the details of the PLD programming, refer to the listings in the appendix. The different operation modes of the read control logic are selectable via I²C and the serial-to-parallel converter IC PCF8574 at position U40 with I²C device slave address 43 hex.

Implementation, control logic

The listings of the programs of the PLDs as given in the appendix contain extensive comments to improve the understanding of the logic equations and statements. A few explanations regarding the construction of the state machines are given in this section.

WSYNCB

The main state machine in WSYNCB handles the interface with the scaler output of the

SAA7194 in FIFO mode. The IDLE state is the state after regular VCLK-burst transmission, waiting for further HFL, or an INCADR=Low stimuli, to enter the INCHOT state. INCHOT has two exits.

Combining INCADR-low with HFL-high signals the end of a line and generates an EOL-flag. But the LINEND state cannot return to IDLE, otherwise it would be re-triggered by a second line-increment pulse combination, and issue a second EOL. The memory read control side would be mis-triggered by this. Therefore, the LINEND state is extended by LWAIT, and can toggle between these two states without action, in order to be insensitive in the case of a second line-increment pulse sequence. A regular HFL during LWAIT starts the normal VCLK bursts.

The second exit of INCHOT is the return to neutral HFL-INCADR combination, which signals the vertical end of processing, and issues an EOF-flag. In this VERTEND state a line-increment condition may occur to signal the begin of an odd field. Then EOL-EOF double flag is issued to indicate Field ID reset and Frame Buffer Bank pointer reset.

The state machine for the transparent mode is somewhat simpler. it is built to generate the same EOL and EOF flags.

WPATHB

WPATHB is mainly a data bus multiplexer. The control signals need to be registered to be synchronous to data. WPATHB sorts out the FIFO fill pixels, inserts the alpha marker and EOL and EOF markers. The reset of the write address pointer is delayed another clock cycle to avoid conflict with a last write of EOF.

READCLKB

In this programming, READCLKB is used mainly for clock selection and as clock driver. It also routes the horizontal and vertical sync signals depending on who the timing master is.

READVB

The main function of READVB is the vertical counter, whose bits are also used to define a signal pattern in luminance and chrominance for use as a background signal. The equal comparison with VOS generates a valid signal for two half lines, which belong in an even field to two display lines. The VWB0 state gates this two half line period with the second half of a real line. This state is reserved for resetting the read address pointer with RSTR. The following state, VWB1, stays for an entire line and represents the vertical window start for READHB, by providing FSGO.

The vertical states distinguish an idle range above and below the line, where the window start is defined. (This may be used to issue different background signals, which is not implemented here).

The VSO state is relevant for the mode that SAA7194 is master for display timing and SAA7199 is in slave mode. As the vertical counter is triggered at the trailing edge of vertical sync, and the decoder delivers a delayed vertical sync, READVB generates a VSD for the SAA7199, which starts 13 half lines ahead of this vertical trigger point.

READHB

READHB has an horizontal counter. It starts the programmable (HOS) horizontal window and also generates the half line reference signal HS2RD. The horizontal state machine is triggered by the window start condition and the end-of-line and/or end-of-field marker in the data stream. The state machine has to work around the signal delays between enabling a read cycle at the FRAMs, and placing valid data on the output bus. In the FIRST state, the marker decoding logic will not see valid data, but the tristate signal of the FRAMs. In the LAST1 (and WBLK1) state, the reading from the FRAMs has already stopped, but there may be the next marker in the signal path pipe line. If this pixel was not a marker, it was a real pixel, i.e., the first pixel of the next line. This pixel is lost for display.

DIGITAL ENCODER SAA7199B

The backend circuitry with the digital NTSC and PAL encoder is identical to the backend processing of the DTV7199 demo board. For a detailed description please refer to the application note "DTV7199 Digital Television Demonstration System," p. 2-72.

VIDEO DACS AND MATRIX

For conversion of the digital YUV data stream to analog RGB, the SAA7165 video DAC is used to convert the data stream to analog YUV, and the TDA4686 RGB matrix combination IC is used to convert the analog YUV into analog RGB with control over brightness, saturation, and contrast.

The SAA7165 (VEDA2) filters and demultiplexes the UV data and positions this chroma data with respect to the proper luminance sample and performs the D to A conversion. In addition, software controlled aperture correction and color transient improvement of the video may be performed to enhance picture quality.

The TDA4686 receives this analog YUV signal, reclamps it and converts it to RGB via an analog matrix. Two additional RGB signals may be switched into this path, assuming that they are congruent to the main RGB information (that is, they are synchronous). Brightness, saturation, and contrast control may be affected via the I^2C bus. Also, peak white and color balance may be controlled via I^2C.

The TDA4686 uses a multi-level pulse to control certain blanking and timing parameters, called a sandcastle pulse. Because this pulse is generally derived from the sync signals, it is necessary to account for the 44 clock pipeline delay introduced by the SAA7165 when generating this pulse so that the pulse has the proper positional relation with the output video from the SAA7165.

Additional circuitry at the output is used to produce proper DC and drive levels to drive 75Ω loads.

A more detailed description of this module is given in the application note titled "Digital Video Evaluation Board" (also in this chapter, p. 2-171), along with register programming for these two devices.

INTERLACED VIDEO SIGNALS

The broadcast television standards—and the related camera standards—are all interlaced. There are two fields (field rate 50Hz or 60Hz), whose scan lines are interleaved to each other. The second field scans its lines right in between the lines of the first field, but a moment—i.e., a period of the field rate—later. Both fields together form a frame. The line-to-field scan interlacing method was developed to balance achievable vertical resolution with motion resolution and required transmission bandwidth. For mainly static pictures and scenes, a high vertical resolution can be achieved by counting the information of two fields as one frame. For high motion video pictures, a time resolution of 50Hz or 60Hz is achieved; this is superior to the 24Hz of cinema film.

If both input and output of the frame buffer memory is structured in an interlaced manner, the situation is rather obvious. This is the case if the SAA7194 decodes a standard television signal and the SAA7199 encodes a standard television signal. We have to take care that the lines of the second field get displayed inbetween the two lines of the first field, as they were scanned in the first place. In a straightforward way, the two fields are written into two memory banks, and also read from them in the right sequence and phase (i.e., starting the line counting).

In the case that input and output field rates are not identical, two memory banks are clearly insufficient to ensure that field two is always and only read after the correlated preceding field one. An incorrect field sequence would generate motion disrupting artifacts (jumping back and forth).

If the vertical scan speed, i.e., time from line to line, is not the same at the write and read side of the memory, so called "tearing" can occur. The write and read pointers in the memory address space are crossing each other. The results are that information displayed as one field are originated by separate fields.

To avoid these two artifacts, memory with a capacity to store four fields and dedicated control would be necessary. The DTV7194 demo board has only two memory banks and does not solve the above mentioned problems. In the case of synchronous input and output operation, e.g., by connecting DESC and DENC by means of RTC, they don't occur.

If the input of the frame buffer memory is non-interlaced material, and the output of the memory needs to be interlaced, e.g., for the DENC, then "re-interlacing" has to take place. Non-interlaced video can get fed in via the expansion port from video decompression or artificial sources (graphics generation), or the scaling function itself can generate it by programming it to one-field-only operation (odd field only, even field only).

"Re-interlacing" can be achieved by proper modification either of the write or read control of the frame buffer. The alternating lines of a non-interlaced field can be written in a line-toggling fashion into both memory banks, but read in a field toggling manner. This kind of re-interlacing is comparable—also comparable in results—to film-to-TV conversion.

If the input of the frame buffer memory is interlaced material, and the output of the memory needs to be non-interlaced, then "de-interlacing" has to take place. Non-interlaced frame buffer output may be required for display on a computer monitor, or to drive a video printer, or to feed a compression engine. De-interlacing can be achieved by proper modification either of the write or read control of the frame buffer. The alternating fields of an interlaced frame can be written in a field-toggling fashion into both memory banks, but read in a line toggling manner. De-interlacing in that way works well for static pictures, but creates artifacts during motion. DTV7194 has no provisions, regarding memory control, against these artifacts. The more preferable approach is to select the one-field-only operation for the scaling function in the SAA7194.

If both the input and output of the frame buffer are non-interlaced data streams, the situation is transparent; one field is the same as one frame. The field toggling write mode would just write into one memory bank, depending on actual phase of vertical to horizontal sync. The read control has no chance—by any means—to know from where to read. Therefore, for this case, a line toggling mode on both sides is appropriate. This approach also allows handling (storage) of larger frames, e.g., 800 pixels by 600 lines, with the given board architecture, as it splits a frame into two 'interlaced' memory banks. But the board is not made to clock with real VGA clock rates.

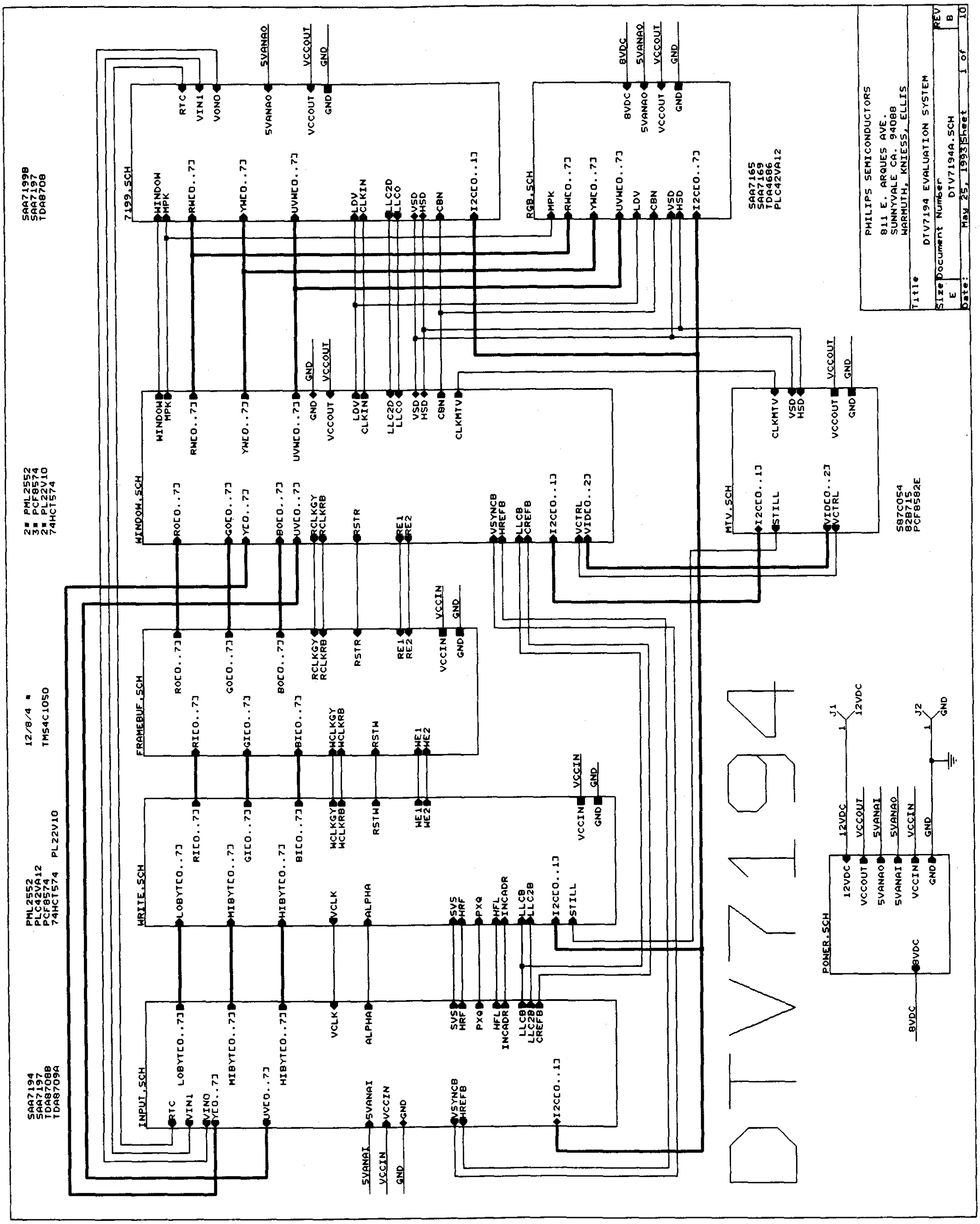
The printing sequence as part of the memory control can "field-toggle" or "line-toggle" between the two memory banks. This toggle mode is selectable via I^2C, both for writing and reading, and independently of each other. By that, interlaced and non-interlaced video signals can be handled and converted into each other.

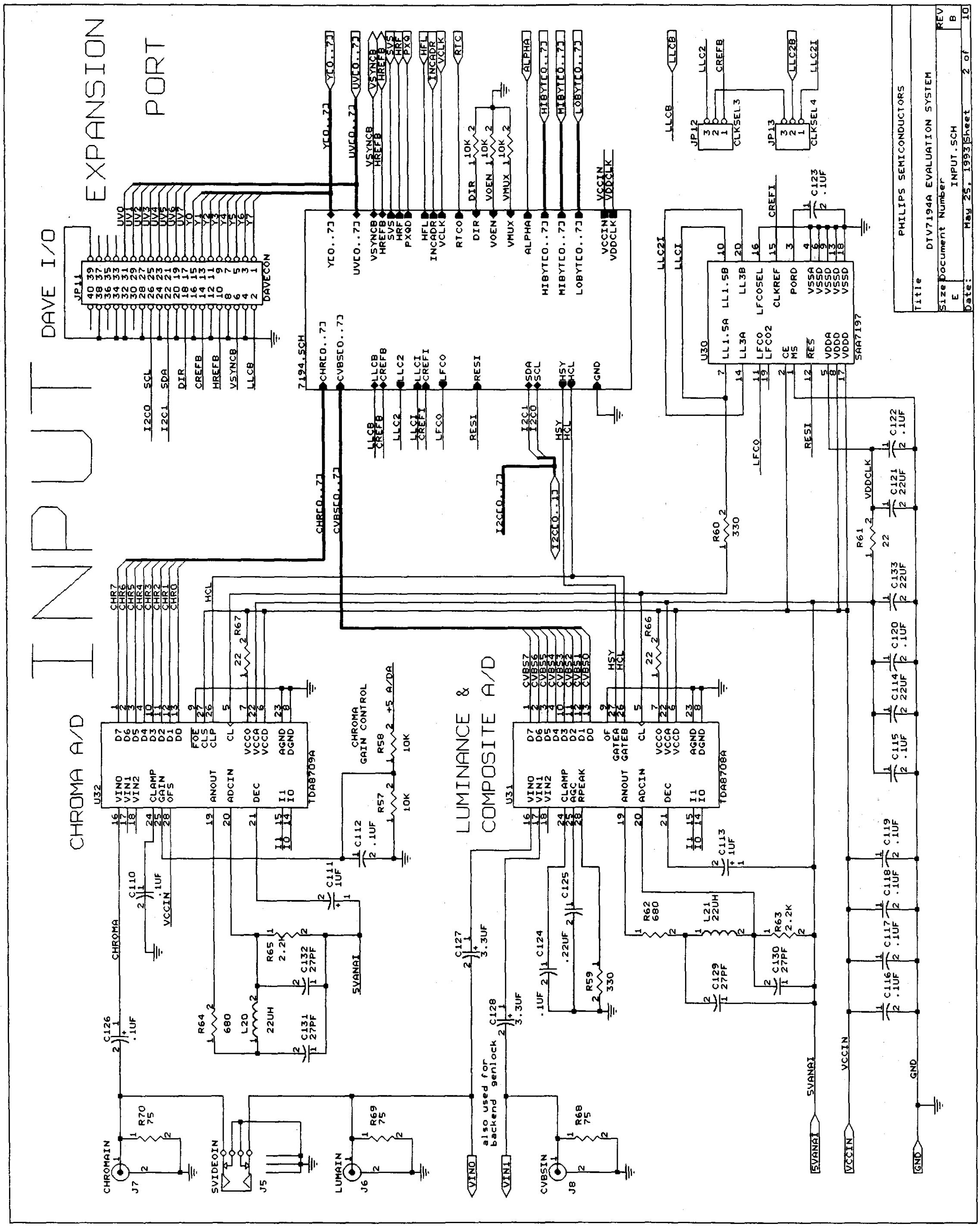
SUMMARY

Many other data output formats and memory architectures are possible using the SAA7194 and associated chips. This application note touches on just a subset of possibilities to suggest an approach that uses minimum memory and memory control devices to implement a system.

APPENDIX

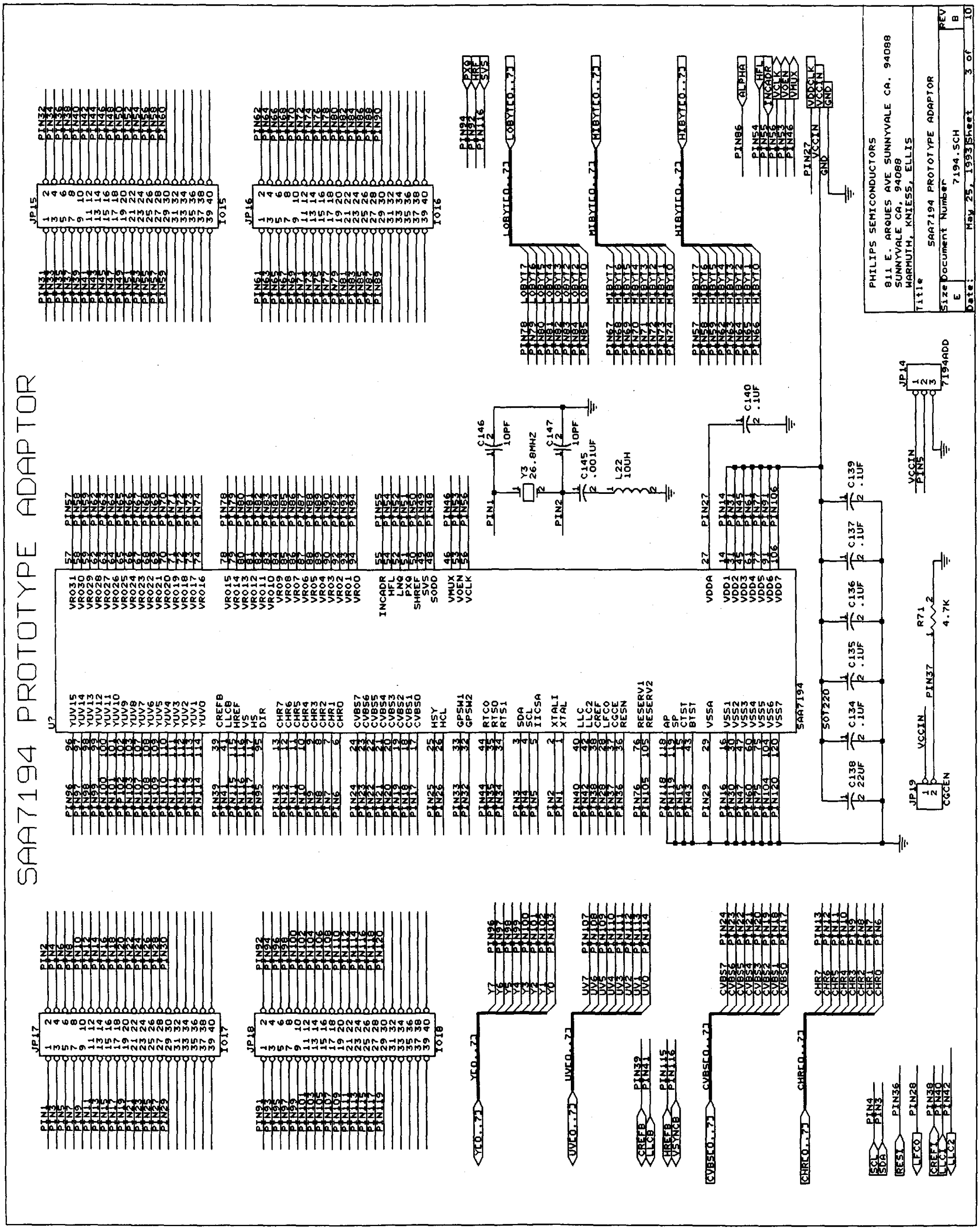
Schematics of DTV7194 demo board




INPUT
EXPANSION PORT
DAVE I/O
CHROMA A/D
LUMINANCE & COMPOSITE A/D
TDA8709A
TDA8708A
SAA7197
7194.SCH
DAVECON
PHILIPS SEMICONDUCTORS
DTV7194A EVALUATION SYSTEM
INPUT.SCH
May 25, 1993
also used for backend genlock

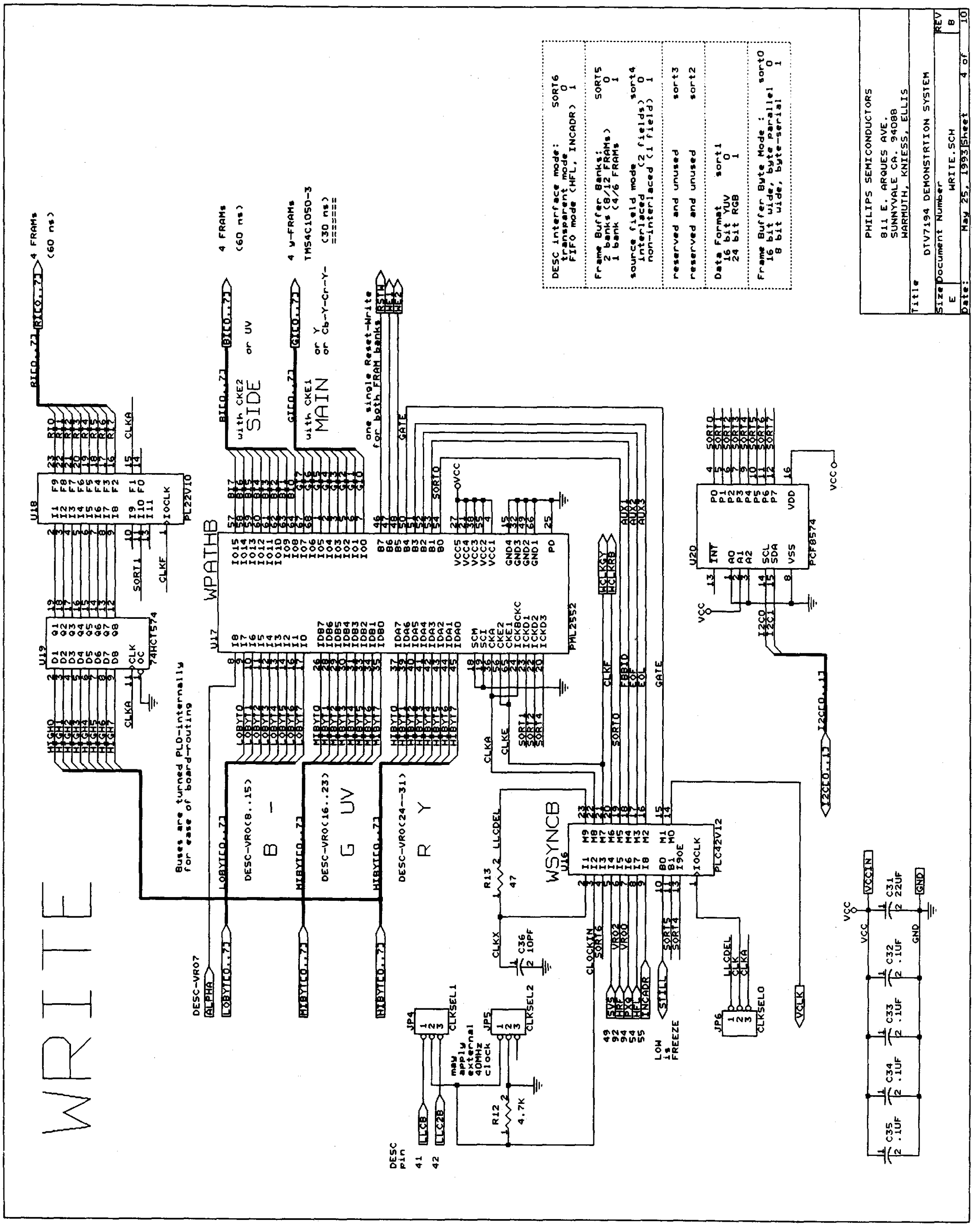
Desktop video demo board

DTV7194



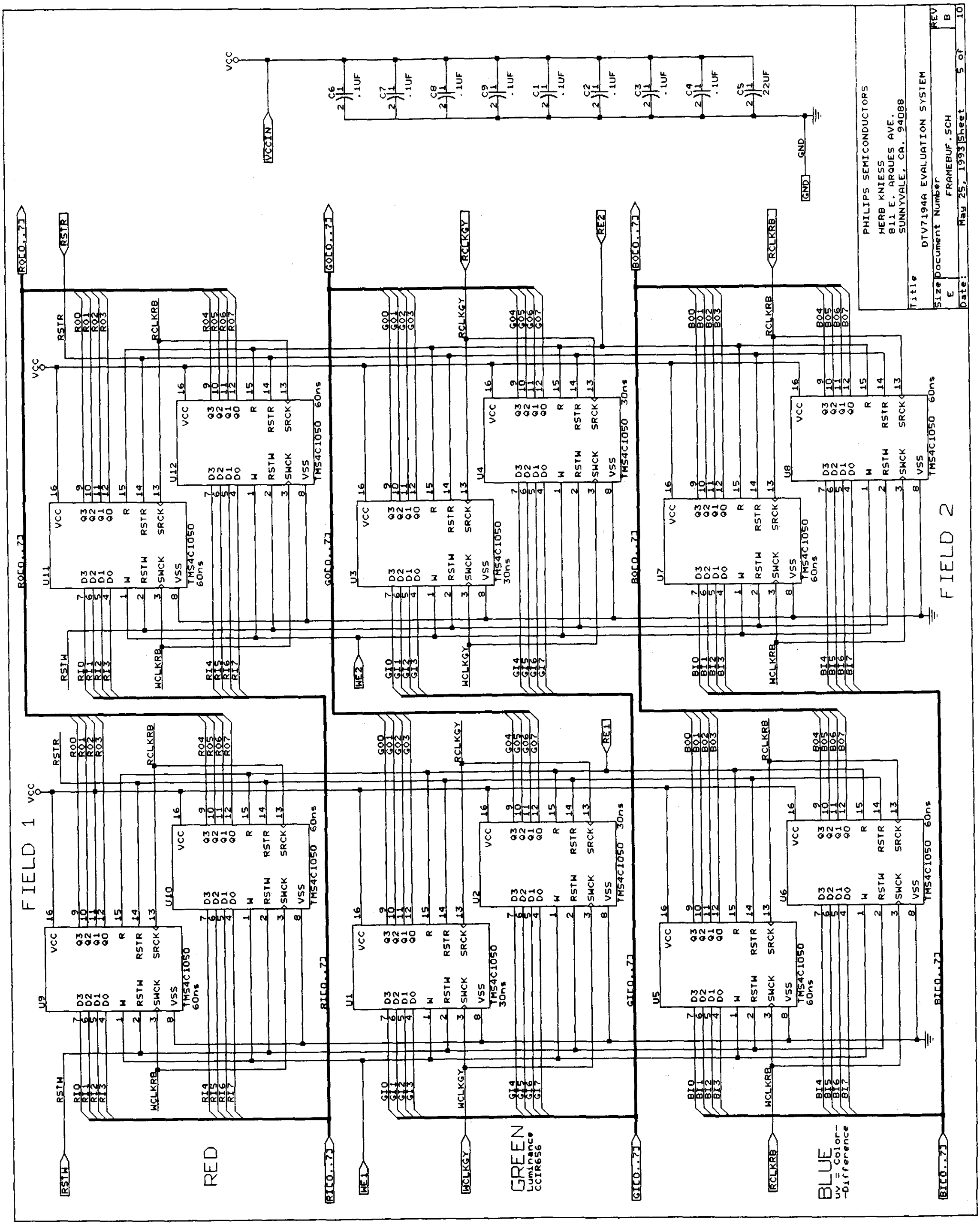
Desktop video demo board

DTV7194



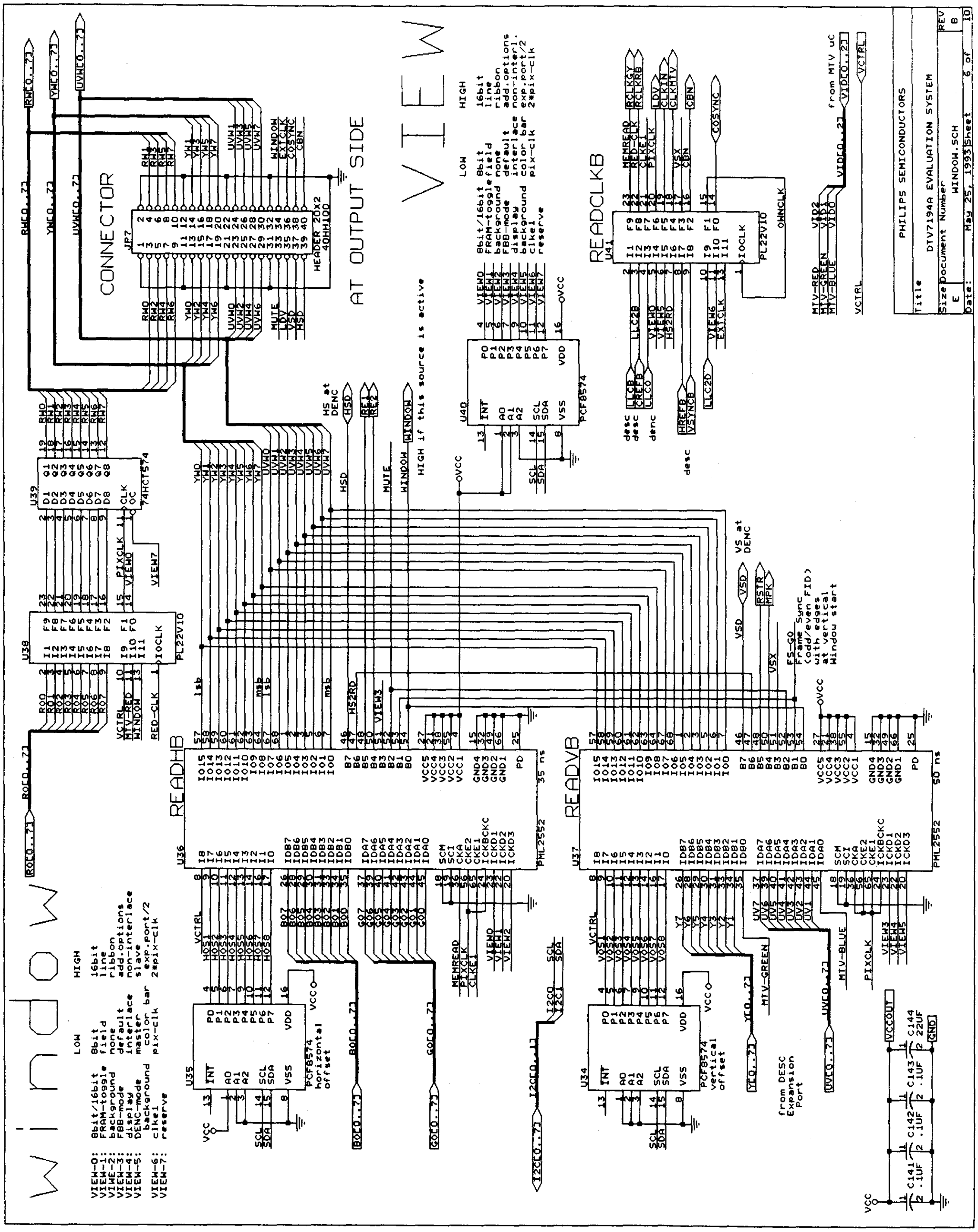
Desktop video demo board

DTV7194

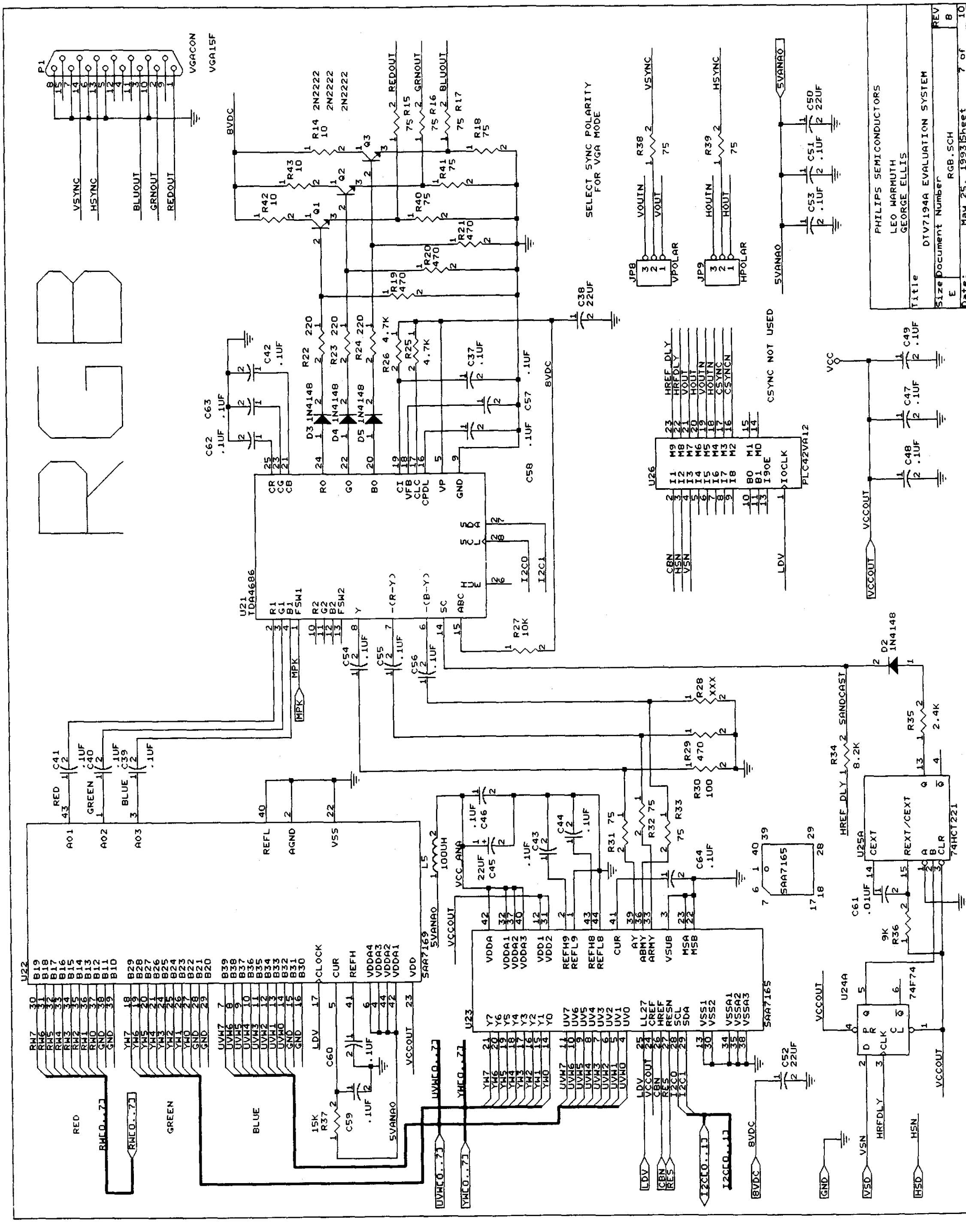


Desktop video demo board

DTV7194

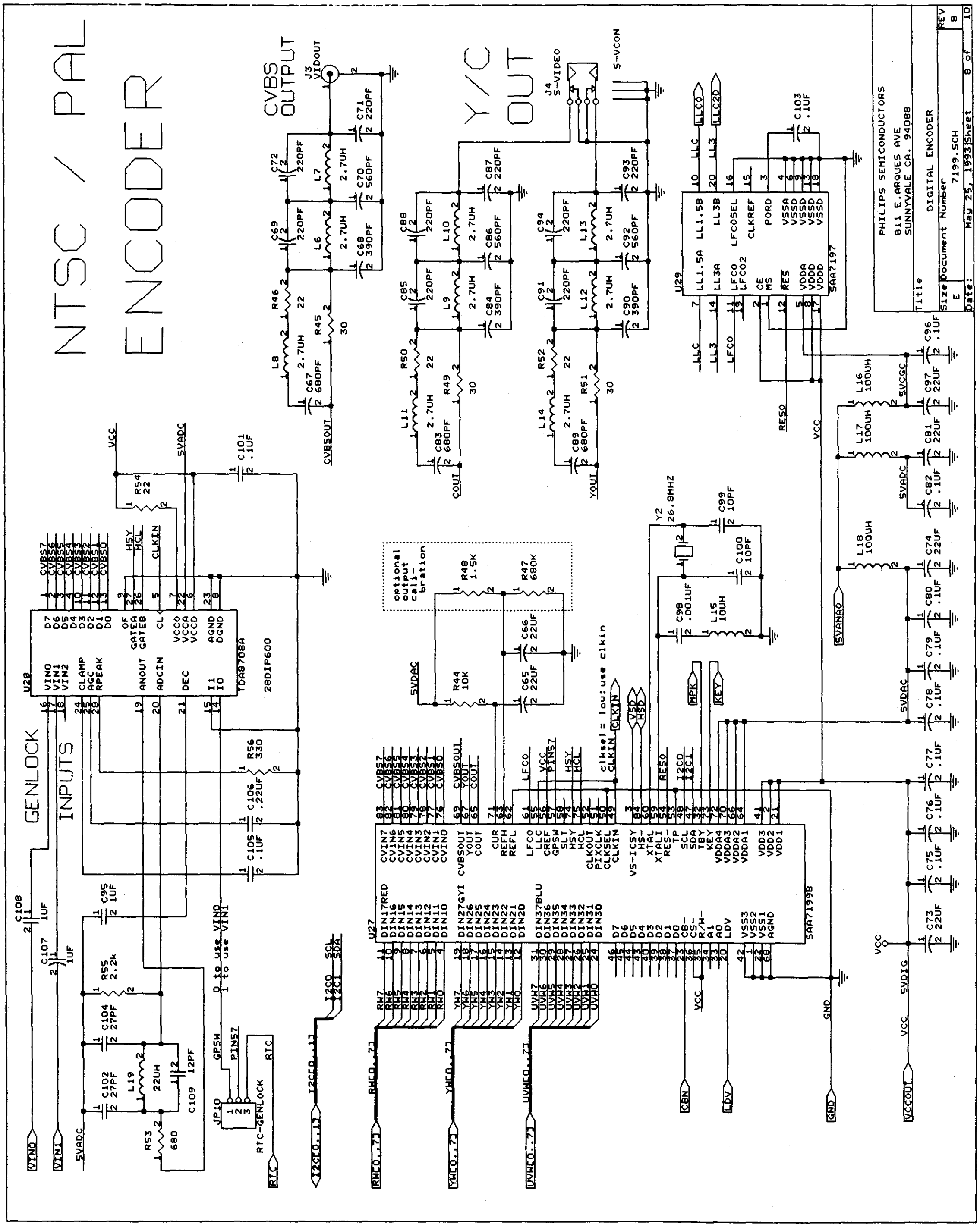


Desktop video demo board | DTV7194

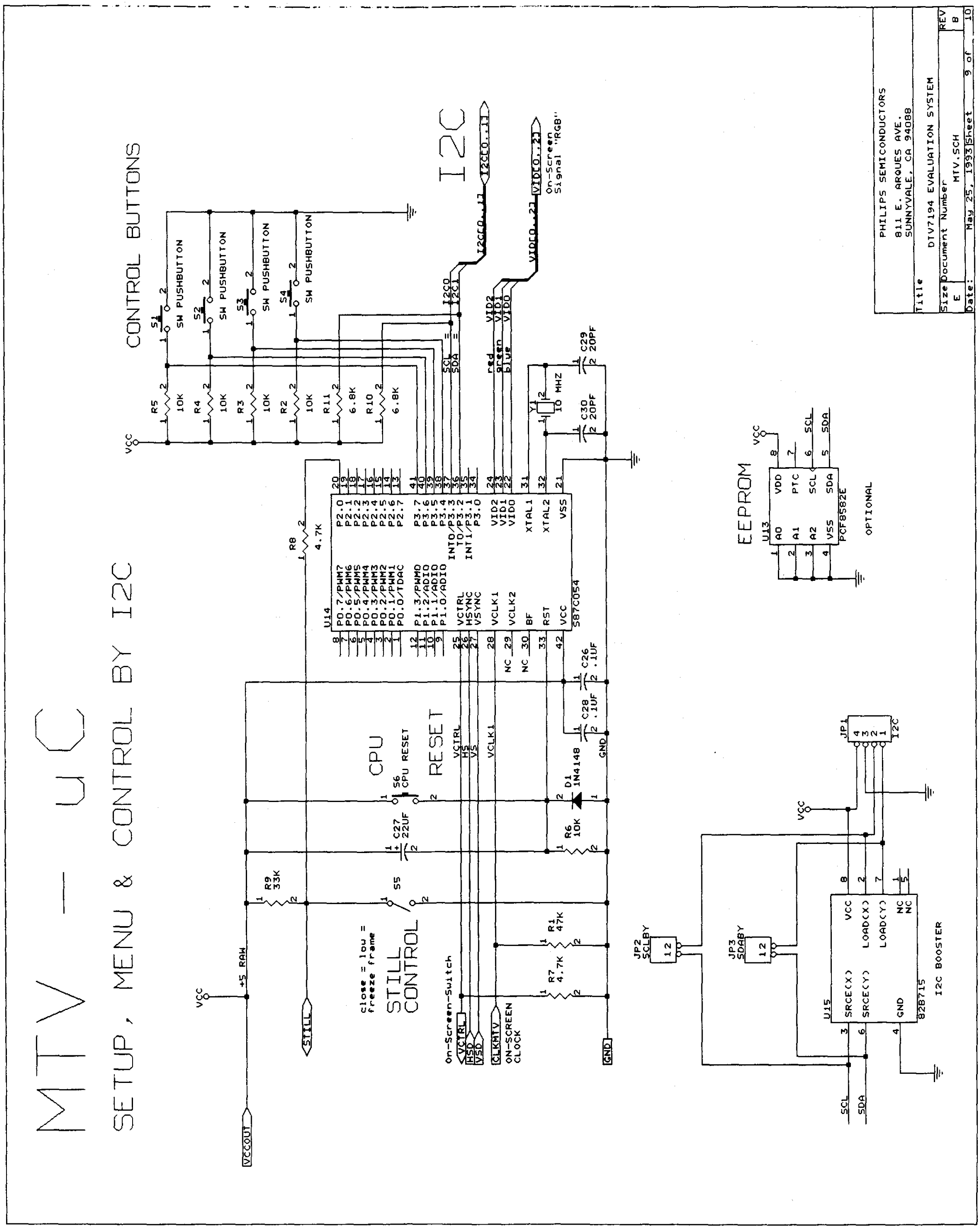


Desktop video demo board

DTV7194

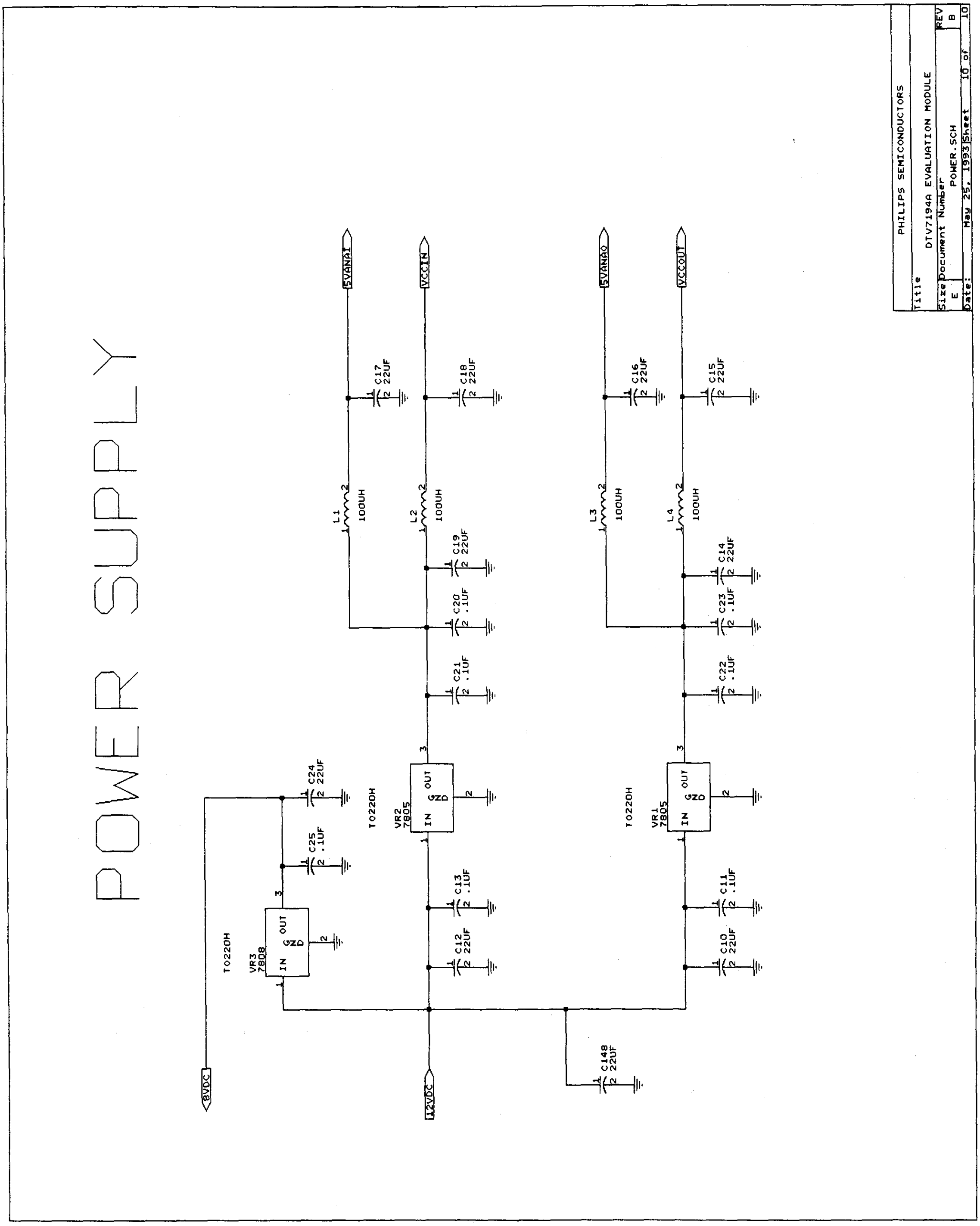


Desktop video demo board DTV7194



Desktop video demo board

DTV7194



Programs of the PLDs used on DTV7194 board

```
    " WSYNCPLB :      WRITEPLC:  clock divider, clock drivers     "
    " =========       HFL,INCADR --> VCLK, EOL, EOF for           "
    " PLC42VA12                           asynchronous FIFO mode  "
    "                 PXQ, HRF, SVS --> EOL, EOF for              "
    " U16                            synchronous TRANSPARENT mode "

@PINLIST    " pin#:      to go into PLC42VA12                     "

CLOCKIN  I ; " 3: LLC2 or 'high-clock', from CGC or EXP-port     "
CLOCKDEL O ; "23: clock pass-through, delayed out, to drive CLKX"
CLKX     I ; " 2: delayed clock-in, to adjust phase of clk-e+f   "
               "  to clk-ab and vclk, in case of clock divide    "
CLK      I ; " 1: dedicated clock input, vclk frequency          "
VCLK     O ; "14: clock at VRO-port, DESC-scaler output          "
CLKAB    O ; "22: clock at VRO-port-to-PML interface, PML-side   "
CLKE     O ; "21: clock at memory write interface, Y-G-channel   "
CLKF     O ; "20: clock at memory write interface, RB-channel    "
               "      second clock driver for FRAM memory bank   "

HFL      I ; " 8: fifo half full flag                            "
INCADR   I ; " 9: increment address, for line and field end      "

PXQ      I ; " 7: pixel qualifier in transparent data stream     "
HRF      I ; " 6: horizontal reference signal
                                   in transparent-data-stream    "
SVS      I ; " 5: vertical sync, referring to scaler output      "

GATE     O ; "15: valid pixel at VRO = in front of WPATHPMB      "
EOLPIN   O ; "16: end of line flag, to WPATHPMB                  "
EOFPIN   O ; "17: end of field flag, to WPATHPMB                 "
               " both together: reset of FB write pointer        "
FBBID    O ; "18: Frame Buffer Bank ID: where to write to        "

STILL    I ; "10: still (=0) = freeze picture, no write update   "
SORT0    I ; "19: controls clock divider:                        "
               " all clocks in pixel clock: byte-parallel = 0    "
               " write-clk = 2*pixelclock : byte-serial   = 1    "
               " byte-serial requires hi-enough clock @ CLOCKIN"
SORT4    I ; "13: Field Buffer Modes,                     sort4 "
SORT5    I ; "11: Field Buffer Modes,                 sort5      "
               " interlaced = 2 fields --> 2 FBB       0    0
                 non-interlaced = 1 f. --> 2 FBB       0    1
                 interlaced = 2 fields --> 1 FBB       1    0
                 non-interlaced = 1 f. --> 1 FBB       1    1    "
SORT6    I ; " 4: Scaler Output Interface Mode                   "
                       " transparent-mode :    SORT6 = 0         "
                       " fifo-mode        :    SORT6 = 1         "
@GROUPS
@TRUTHTABLE
```

```
@LOGIC EQUATIONS
                                          " === OPERATIONAL MODES === "
SERIAL    =  SORT0 ;                  " byte-serial write:    SORT0 =1 "
WIDE      = /SORT0 ;                  " 16 bit wide write:    SORT0 =0 "
FIFOMODE =  SORT6 ;                   " Scaler Output Interface Mode  "
                                      " fifo-mode = 1, transparent = 0"

                                                  " ===  CLOCKS === "
        " in 16 bit wide memory mode (sort0=0):
                                all clocks are 'pixel' clock frequent "
        " in 8-bit narrow = byte-serial mode (sort0=1):
           provided CLOCKIN is 2 * 'pixel' clock --> CLKE, CLKF
           divide by 2 for VRO interface clock CLKAB, VRCLK   "

CLOCKDEL     = /CLOCKIN ;             " for delayed feed back          "
CLKDIV.CLK   =  CLOCKIN ;             " clock-in must be  2 * pix-clk "
CLKDIV.J   =  1  ;                    " divide by toggle               "
CLKDIV.K   =  1  ;
"VRCLK    =  WIDE * CLOCKIN    "      " clock-in is pixel clock pixclk"
 "          + SERIAL * CLKDIV ;"      " clock-in must be  2 * pix-clk "
CLKAB   =  WIDE * CLOCKIN             " i.e. ==  VRCLK                 "
        + SERIAL * CLKDIV ;           " clock as at VRO interface      "
CLKE    =  WIDE   * CLOCKIN           " pix-clk as FRAM-write-clock   "
        + SERIAL * CLKX    ;          " properly delay adjusted,hi-clk"
CLKF    =  CLKE            ;          " just a second driver for FRAMs"
GATE0   =  /FIFOMODE                          " continuous clock       "
        +  FIFOMODE * Q3 ;                    " OR  burst of clocks    "
  GATEVCLK        =  GATE0 ;
" GATEVCLK.D      =  GATE0 ;  "           " for clean gating of vrclk:"
" GATEVCLK.CLK    = /CLKAB ;  "           " GATE is clocked by /vrclk "
VCLK    =                               " clock for VRO: vrclk * gate "
           WIDE * CLOCKIN   * GATEVCLK
         + SERIAL * CLKDIV * GATEVCLK ;

                                                 " === REGISTERS === "
Q[0..3].CLK = CLK ;     " state machine register                      "
FBBID   .CLK = CLK ;    " Frame Buffer Bank ID, where to write to"
FREEZE .CLK = CLK ;

                                                   " === CONTROL === "
GATEVRO =    /FIFOMODE * PXQ              " valid PXQ  data at VRO "
           + FIFOMODE * Q3  ;             " valid FIFO data at VRO "
FREEZE.D =      EOF * /STILL              " STILL is active low    "
            + /EOF * FREEZE ;             " freeze complete fields "
GATE     = GATEVRO * /FREEZE ;          " valid data at input of PML "
EOLPIN   = EOL ;
EOFPIN   = EOF ;
```

```
@INPUT VECTORS
     [ FIFOMODE,SVS,HRF,PXQ ]          " vector for TRANSPARENT mode"
PX      =   0     -    -    1   B ;    " valid pixel, set LA and FA "
HREF    =   0     0    1    -   B ;    " horizontal reference, also :
                                         end of VS in even field     "
BLANK   =   0     0    0    0   B ;    " horizontal blanking, rst LA,
                                         also:end of VS in odd field"
VS      =   0     1    -    -   B ;    " vertical sync pulse          "

     [ FIFOMODE, INCADR, HFL]            " vector for FIFO mode         "
NEUTRAL  =  1         1    0   B ;       " default input, no action "
FLAG     =  1         1    1   B ;       " regular HFL, start burst "
INCLO    =  1         0    0   B ;       " incadr-up --> field incr."
LINC     =  1         0    1   B ;       "    hfl-up --> line incr. "

          [ EOL, EOF, SORT5, SORT4 ]             " vector for FBBID "
ENDFRAME =   1    1     -      -    B;
FTOGGLE  =   0    1     0      0    B;
LTOGGLE  =   1    0     0      1    B;
EVERYF   =   0    1     -      1    B;
@OUTPUT VECTORS
            [EOF,EOL]              " same flags/vector for BOTH modes "
EOLINE   =   0    1    B ;            " write EOL, then L-toggle FB    "
EOFIELD  =   1    0    B ;            " write EOF, then F-toggle FB    "
BODD     =   1    1    B ;            " Begin of ODD field, FB-reset-W"
@STATE VECTORS
                                 " two state machines in one vector set "
          [ Q3,Q2,Q1,Q0 ]  " idle + 3 states for transparent mode "
IDLE     =  0  0  0  0  B ;            "        idle                  "
LAFA     =  0  0  1  1  B ;            " this Line  is/was Active "
FA       =  0  0  1  0  B ;            " this Field is/was Active "
VP       =  0  0  0  1  B ;            " vertical pause & reset    "
INCHOT   =  0  1  0  0  B ;        " incadr is low (hot to act)    "
LINEND   =  0  1  0  1  B ;        " hfl after inc-hot, issue eol "
LWAIT    =  0  1  1  1  B ;        " to iron out 2nd linc->eol      "
VERTEND  =  0  1  1  0  B ;        " rising edge of incadr @ hfl=0"
                                   " (field end) till 'next' event"
                                   " to investigate for odd field "

COUNT0   =  1  0  0  0  B ;
COUNT1   =  1  0  0  1  B ;
COUNT2   =  1  0  1  0  B ;
COUNT3   =  1  0  1  1  B ;        " count through the VCLK burst "
COUNT4   =  1  1  0  0  B ;        " Q3 to feed GATE.D for PML     "
COUNT5   =  1  1  0  1  B ;        " Q3 to enable VCLK for VROport"
COUNT6   =  1  1  1  0  B ;
COUNT7   =  1  1  1  1  B ;
         [ FBBID ]                 " for FBBID : Field Buffer Bank"
ODD      =  1     B;               " this is not field ID, but is "
EVEN     =  0     B;               " set to it at frame start     "
```

```
@TRANSITIONS
                                  " CASE-statements for FIFO mode"
WHILE [IDLE]
  CASE   [FLAG]                   :: [COUNT0]
         [INCLO]                  :: [INCHOT]   ENDCASE
WHILE [INCHOT]
  CASE   [LINC]     WITH [EOLINE] :: [LINEND]
         [NEUTRAL] WITH [EOFIELD] :: [VERTEND]  ENDCASE
    " !! no line increment may occur before field increment !!  "
WHILE [LINEND]
  CASE   [NEUTRAL]                :: [LWAIT]    ENDCASE
WHILE [LWAIT]
  CASE   [FLAG]                   :: [COUNT0]
         [LINC]                   :: [LINEND]   ENDCASE
WHILE [VERTEND]
  CASE   [FLAG]                   :: [COUNT0]
         [LINC]     WITH [BODD]   :: [LINEND]   ENDCASE
WHILE [COUNT0]   CASE []   ::   [COUNT1]    ENDCASE
WHILE [COUNT1]   CASE []   ::   [COUNT2]    ENDCASE
WHILE [COUNT2]   CASE []   ::   [COUNT3]    ENDCASE
WHILE [COUNT3]   CASE []   ::   [COUNT4]    ENDCASE
WHILE [COUNT4]   CASE []   ::   [COUNT5]    ENDCASE
WHILE [COUNT5]   CASE []   ::   [COUNT6]    ENDCASE
WHILE [COUNT6]   CASE []   ::   [COUNT7]    ENDCASE
WHILE [COUNT7]   CASE []   ::   [IDLE]      ENDCASE

                              " IF-statements for TRANPARENT mode "
WHILE [IDLE]
   IF    [PX]                        THEN    [LAFA]
WHILE [LAFA]
   IF    [BLANK] WITH [EOLINE]       THEN    [FA]
WHILE [FA]
   IF    [PX]                        THEN    [LAFA]
   IF    [VS]    WITH [EOFIELD]      THEN    [VP]
WHILE [VP]
   IF    [BLANK] WITH [BODD]         THEN    [IDLE]
   IF    [HREF]                      THEN    [IDLE]

WHILE [EVEN]                                " transitions of FBBID "
   IF    [ENDFRAME]       THEN    [ODD]
   IF    [LTOGGLE]        THEN    [ODD]
   IF    [FTOGGLE]        THEN    [ODD]
   IF    [EVERYF]         THEN    [ODD]
WHILE [ODD]
   IF    [LTOGGLE]        THEN    [EVEN]
   IF    [FTOGGLE]        THEN    [EVEN]
```

```
        " WPATHB    :    DATA PATH interface VRO to frame buffer "
        " ==========     multiplex for YUV and RGB bus formats   "
        " PML2552        marking data with eol, eof, alpha       "
        "                byte-serializing                        "
        " U17            frame buffer write enable and reset     "

@PINLIST

CLKA     I ;            " clock for input register            "
CLKB     I ;            " clock for input register            "
CLKE1    I ;            " clock for output register (main)    "
CLKE2    I ;            " clock for output register (side)    "

HIBYT[7..0]  I ;        " Y     in case of YUV-16             "
                          " RED   in case of RGB-24               "
MIBYT[7..0]  I ;        " UV    in case of YUV-16             "
                          " GREEN in case of RGB-24               "
LOBYT[7..0]  I ;        " not used in YUV-16 format           "
                          " BLUE  in case of RGB-24               "
ALPHA        I ;        " alpha-bit,    color key             "

MAIN[7..0]   O ;        "  GI - channel to FRAMs, also serial  "
SIDE[7..0]   O ;        "  BI - channel to FRAMs              "

GATEPIN I ;             " gate over VCLK-bursts,i.e.valid pixels"
EOLPIN  I ;             " end-of-line (frame) marker          "
EOFPIN  I ;             " end-of-field/frame marker           "
FBBIDIN I ;             " frame buffer bank ID, to write to   "

RSTW    O ;             " reset of frame buffer write pointer  "
WE1     O ;             " write enable for frame buffer bank 1 "
WE2     O ;             " write enable for frame buffer bank 2 "

SORT0   I ;             " byte-parallel / serial memory mode:  "
                          " 16 bit wide parallel: sort0 = 0
                            8-bit 'byte-serial   : sort0 = 1       "
SORT1   I ;             " data format select:   YUV : sort1 = 0 "
                          "                            RGB : sort1 = 1 "
SORT2   I ;             " reserved, not used in this programming"
SORT4   I ;             " FB-reset mode: field = 0, frame = 1  "

@GROUPS
FILLV   =  [ 0,0,0,0, 0,0,0,1 ] ;       " fifo fill pixel value "
KEYMARK =  [ 0,0,0,0, 0,0,0,1 ] ;       "transparent ALPHA pixel"
EOLMARK =  [ 0,0,0,0, 0,0,0,0 ] ;       " end of line marker    "
EOFMARK =  [ 1,1,1,1, 1,1,1,1 ] ;       " end of field marker   "


@TRUTHTABLE
```

```
@LOGIC EQUATIONS
                                              " === INPUT REGISTER === "
IDA[7..0].ID =    HIBYT[7..0]   ;
IDB[7..0].ID =    MIBYT[7..0]   ;
IDC[7..0].D  =    LOBYT[7..0]   ;                   "     JKPR552     "
KEY      .D  =    ALPHA    ;
EOL      .D  =    EOLPIN   ;                        "     JKCL552     "
EOF      .D  =    EOFPIN   ;
GATE     .D  =    GATEPIN ;
FBBID    .D  =    FBBIDIN ;

                                                        " === TWIST === "
" brings YUV and RGB into channel order according to DENC inputs
  and byte-SERIALizes (YUV only) as an option for memory saving "
YUV       =  /SORT1 ;
RGB       =   SORT1 ;
PARALLEL  =  /SORT0 ;              " 16 bit wide YUV, 24 bit RGB "
SERIAL    =   SORT0 ;              " Cb-Y-Cr-Y-, D! like format  "
PHASE1    =   CLKB  ;                        " first color diff."
PHASE2    =  /CLKB  ;                        " then luminance    "
MAINTW[7..0]  =    YUV * PARALLEL         * IDA[7..0]
                   + YUV * SERIAL * PHASE1 * IDB[7..0]
                   + YUV * SERIAL * PHASE2 * IDA[7..0]
                   + RGB                   * IDB[7..0] ;
SIDETW[7..0]  =    YUV                    * IDB[7..0]
                   + RGB                   * IDC[7..0] ;

                                                  " === MASK & MARK === "
MAINMK[7..0]  =    GATE * /KEY    * MAINTW[7..0]
                   + GATE *  KEY    * KEYMARK
                   +        EOLFLG  * EOLMARK
                   +        EOFFLG  * EOFMARK ;
SIDEMK[7..0]  =    SIDETW[7..0] ;

                                     " ==== WRITE & RESET CONTROL ==== "
EOLFLG    =   EOL   * /EOF ;
EOFFLG    =  /EOL   *  EOF ;
EOFRAME   =   EOL   *  EOF ;
EOFIELD   =            EOF ;
FILLPIX   =  ( IDA[7..0] == FILLV ) ;
VALID     =  GATE * /FILLPIX ;
WEGATE    =  VALID  + EOLFLG + EOFFLG ;
FRAMERST = /SORT4 ;
FIELDRST =  SORT4 ;
RSTW0.D   =  FRAMERST * EOFRAME      " extra clock cycle delay     "
           + FIELDRST * EOFIELD ;   "to reset pointer after write"
```

```
                                          " === OUTPUT REGISTER === "
MAIN[7..0].OD    =  MAINMK[7..0] ;
SIDE[7..0].OD    =  SIDEMK[7..0] ;
RSTW     .D      =  RSTW0 ;
WE1      .D      =  WEGATE *  FBBID ;
WE2      .D      =  WEGATE * /FBBID ;


                                          " === REGISTER & CLOCK === "
IDA[7..0] .CLK  =  CLKA  ;
IDB[7..0] .CLK  =  CLKB  ;
IDC[7..0] .CLK  =  CLKB  ;
MAIN[7..0].CLK  =  CLKE1 ;
SIDE[7..0].CLK  =  CLKE2 ;
                                          " ---- declarations ---- "
KEY      .CLK   =  CLKB ;
EOL      .CLK   =  CLKB ;
EOF      .CLK   =  CLKB ;
GATE     .CLK   =  CLKB ;
FBBID    .CLK   =  CLKB ;
WE1      .CLK   =  CLKB ;
WE2      .CLK   =  CLKB ;
RSTW0    .CLK   =  CLKB ;
RSTW     .CLK   =  CLKB ;

IDC[7..0].SET   =   1  ;
KEY      .RST   =   1  ;
EOL      .RST   =   1  ;
EOF      .RST   =   1  ;
GATE     .RST   =   1  ;
FBBID    .RST   =   1  ;
WE1      .RST   =   1  ;
WE2      .RST   =   1  ;
RSTW0    .RST   =   1  ;
RSTW     .RST   =   1  ;

@INPUT VECTORS
@OUTPUT VECTORS
@STATE VECTORS
@TRANSITIONS
```

```
        " READCLKB     : select clock and sync system      "
        " ========       clock divider, clock drivers      "
        " U41                                              "

@PINLIST          " for (slow) PL22V10-15                      pin# "

CLOCK    I;       " dedicated clock input for PLD = pixclk    :  1 "
LLCB     I;       " double pixel clock of eXpansion port      :  2 "
CREFB    I;       " clock reference (qualifier) of eXp.port   :  3 "
LLCD     I;       " system clock of CGC at DENC SAA7199B      :  4 "
LLC2D    I;       " DENC-CGC pixel clock                      : 10 "

PIXCLK   B;       " pixel clock for output/display/DENC, LDV : 20 "
                  " O : with DESC or DENC as master                "
                  " I : if provided thru external connector        "
PX2CLK   I;       " external double pixel clock at connector : 13 "

MEMREAD O;        " read clock for FRAMs, luma/green channel : 23 "
REDCLK   O;       " read clock for FRAMs, red & blue channel : 22 "
CLKE1    O;       " inverted pixel clock, for de-serializing : 21 "
CLKIN    O;       " delayed clock for DENC, (inverted LDV)   : 19 "
CLKMTV   O;       " half pixel clock for MTV micro controller: 18 "
OWNCLK   O;       " selected clock, to feed dedic. clock inp.: 15 "

HREFB    I;       " horizontal reference at expansion port    :  8 "
CBN      B;       " CBN to DENC, jumpered with HSD at connect: 16 "
HS2RD    I;       " half line signal from PML1, here not used:  7 "
VSYNCB   I;       " vertical sync at DESC's expansion port    :  9 "
VSX      B;       " Vertical Sync, from Xport to PML2 & DENC : 17 "
COSY     O;       " optional auxiliary signal: combined sync : 14 "

VIEW0    I;       " memory mode: 0 = default: byte parallel. :  5 "
                  " 1=serial: clka=2*pix-clk, clkel=invpixclk      "
VIEW5    I;       " 0: DENC = master; 1: eXpans.Port = master:  6 "
VIEW6    I;       " optional: external master thru connector : 11 "

@GROUPS

@TRUTHTABLE
```

```
@LOGIC EQUATIONS

PARALLEL = /VIEW0;
SERIAL   =  VIEW0;                            " byte serial     "
DENC     = /VIEW5*/VIEW6;             " DENC is timing master "
XPORT    =  VIEW5*/VIEW6;  " timing signals from expansion port "
EXT      =         VIEW6;  " timing from output side connector  "
LLC2B    = CREFB ;

PIX2        =  DENC   * LLCD
             + XPORT  * LLCB                  " double pixclk "
             + EXT    * PX2CLK    ;
PIX1        =  DENC   * LLC2D
             + XPORT  * LLC2B                 " pixel clock    "
             + EXT    * PIXCLK    ;
OWNCLK      =  /PIX1  ;              " pixel clock for external
                                       feedback to CLOCK input"

MEMREAD     =  PARALLEL * CLOCK          " clock for FRAM-    "
               + SERIAL   * PIX2 ;       "     -read interface"
REDCLK      =  MEMREAD ;                 " second driver      "
PIXCLK      =   CLOCK  ;                 " pixel clock = LDV "
PIXCLK.OE   =  /EXT ;
CLKE1       =  PARALLEL *  CLOCK
               + SERIAL   * /CLOCK ;     " >50% phase shift   "
CLKIN       =  /PIXCLK;                   " CLK-IN for DENC   "
CLKMTV.D    = /CLKMTV ;                " 1/2 pixel clock for uC"
CLKMTV.CLK  =  CLOCK  ;                " toggle by pixclk       "

CBN     = HREFB ;
CBN.OE  = XPORT ;
VSX     = VSYNCB ;
VSX.OE  = XPORT  ;
COSY    = /(XPORT*VSYNCB + DENC*VSX + CBN) ;
COSY.OE = /EXT ;                    " negative going block sync "

@INPUT VECTORS

@OUTPUT VECTORS

@STATE VECTORS

@TRANSITIONS
```

```
        " READVB     :      vertical definition of display window     "
        " ==========        memory read pointer reset, generate VSD   "
        " PML2552-50        background data path pass through,        "
        "                   vertical test (color bar) generation      "
        "                   VCTRL check for MTV micro RGB overlay     "
        " U37               OVL = overlay insert, generate MPK        "

@PINLIST

CLKA      I ;               " pixel-clock,            all clocks    "
CLKB      I ;               " pixel clock,            same as LDV,  "
CLKE1     I ;               " pixel clock,            for display,  "
CLKE2     I ;               " pixel clock,            i.e. output   "

VOS[8..1]         I ;       " Vertical OffSet of inserted window     "
BY[7..1]          I ;       " background luminance channel, Y        "
BUV[7..1]         I ;       " background chrominance channel, UV     "
                            " background = signal at expansion port "
YW[7..0]      "B" O ;       " luminance output, respectively Green  "
UVW[7..0]     "B" O ;       " colour difference output, resp. Blue  "

VSD       B "I" ;           " VSN of DENC, vertical sync, active LOW"
                            " if output, then triggered by VSX/DESC "
HS2RD     I ;               " half line pulse from READPML1,        "
                            " 1.half-line LOW, 2nd half of line HIGH"
RSTR      O ;               " reset read pointer for both FRAM banks"
MPK       O ;               " Multi-Purpose-Key, switches RGB-yuv   "
VSX       B "I" ;           " input: vertical sync at expansion port"
MUTE      I ;               " from external, tristates outputs      "
FSGO      O ;               " indicates vertical start of window    "
                            " INL2FB : FSGO takes FID     at VWbegin,
                              others : FSGO = line pulse at VWBegin "
WINDOW    I ;               " active (1) during inserted picture    "
                            "       to control data output enable   "

VIEW3     I ;               " frame buffer banks & interlace modes  "
VIEW4     I ;               " frame buffer banks & interlace modes  "
        " mode:     FBBanks:  VIEW-3,-4     FID      FSGO     RSTR
          INterLaced, 2           0  0     odd/evn   fid      oddF
          NonINterlaced,1,2       0  1       na      line    everyF
          INterLaced, 1           1  0     odd/evn   line     oddF "
        " reserved, unused        1  1                               "
VIEW5     I ;               " timing master,      background signal "
                " 0         DENC                     color pattern
                  1         DESC-eXpansion-Port          XPORT/2     "

VCTRL     I ;               " RGB overlay from micro controller->MPK"
MTVG      I ;               " green overlay from MTV         "
MTVB      I ;               " blue overlay from MTV          "

@GROUPS
```

```
@TRUTHTABLE                    " vertical test color bar in UV space "
[ COUNT8,COUNT7,HS2 :                    " in simplified binary code "
         " u " PATU7,PATU6,PATU5,PATU4,
                       " v " PATV7,PATV6,PATV5,PATV4]
  0 0 0 :  1 0 0 0    1 0 0 0  ;              " white    "
  0 0 1 :  0 0 0 1    1 0 1 0  ;              " yellow   "
  0 1 0 :  1 0 1 0    0 0 0 1  ;              " cyan     "
  0 1 1 :  0 0 1 1    0 0 1 1  ;              " green    "
  1 0 0 :  1 1 0 0    1 1 0 0  ;              " magenta  "
  1 0 1 :  0 1 0 1    1 1 1 0  ;              " red      "
  1 1 0 :  1 1 1 0    0 1 0 1  ;              " blue     "
  1 1 1 :  0 1 1 1    0 1 1 1  ;              " black    "

@LOGIC EQUATIONS
                                          " === MODE CONTROL TABLE === "
NIL     =           VIEW4 ;       " non-interlaced display "
INL     =          /VIEW4 ;       " interlaced display     "
INL2FB  = /VIEW3 * /VIEW4 ;       " interlaced, 2 FB banks "
INL1FB  =  VIEW3 * /VIEW4 ;       " interlaced, 2 F in 1 FB bank "
DENC    = /VIEW5 ;                " DENC is sync master "
PATTERN = /VIEW5 ;                " background = test pattern "
XPORT   =  VIEW5 ;                " eXpansion Port is timing master
                                    background = Xport signal / 2 "

                                          " === HORIZONTAL CLOCKS === "
PIXCLK  =  CLKB ;
HS2.D   =  HS2RD ;                 " 1st half line LOW, then HIGH "
H1C     =  HS2 * /HS2RD ;            " 1-pix-pulse at line begin "
H2CLK   =  HS2RD != HS2 ;            " ----  HALF LINE CLOCK --- "
         " i.e. two 1-pix-pulses per line, to count field length"

                                              " === COUNT VERTICAL ==="
COUNT[9..0].RST = /COUNTRST ;                 " .rst guides snap to   "
COUNT[9..0].J   = 1  ;                        " use the 10 * JKCL552  "
COUNT[9..0].K   = 1  ;                        " with individual clock "
COUNT0.CLK = / H2CLK ;
COUNT1.CLK = /(H2CLK * COUNT0) ;
COUNT2.CLK = /(H2CLK * COUNT0*COUNT1) ;
COUNT3.CLK = /(H2CLK * COUNT0*COUNT1*COUNT2) ;
COUNT4.CLK = /(H2CLK * COUNT0*COUNT1*COUNT2*COUNT3) ;
COUNT5.CLK = /(H2CLK * COUNT0*COUNT1*COUNT2*COUNT3*COUNT4) ;
COUNT6.CLK = /(H2CLK * COUNT0*COUNT1*COUNT2*COUNT3*COUNT4
                       *COUNT5) ;
COUNT7.CLK = /(H2CLK * COUNT0*COUNT1*COUNT2*COUNT3*COUNT4
                       *COUNT5*COUNT6) ;
COUNT8.CLK = /(H2CLK * COUNT0*COUNT1*COUNT2*COUNT3*COUNT4
                       *COUNT5*COUNT6*COUNT7) ;
COUNT9.CLK = /(H2CLK * COUNT0*COUNT1*COUNT2*COUNT3*COUNT4
                       *COUNT5*COUNT6*COUNT7*COUNT8) ;
```

```
                                              "=== VERTICAL EVENTS ==="
                                        " --- VERTICAL WINDOW BEGIN --- "
VOS9     =  0 ;                               " first RSTR, then FSGO "
VWB      =  COUNT[9..1] == VOS[9..1] ;        " valid for 2 half lines"
                                              " input to state machine"

                                      " --- RESET READ ADDR.POINTER --- "
RSTR     =  /VQ2 * VQ1 * /VQ0                 " state VWB0 : rst Read "
           * (  NIL                                  " in every field "
              + INL * FID ) ;                       " in odd field only "

                                          " --- VSD / VSX --- I / O --- "
VSI      =  VSD *  DENC                       " VSD from denc or extnl"
           + VSX *  XPORT ;                   " VSX from desc exp.port"
                                         " leading edge of VSD for DENC "
V13   =  COUNT[9..0] == 1FFH ;                " 60Hz: set at 525-1-13=511 "
"V13   =  COUNT[9..0] == 263H ;   "           " 50Hz: set at 625-1-13=611 "
VSD      = /(VQ2*/VQ1*VQ0) ;                 " VSO state: VSD (active low)"
VSD.OE   =  XPORT ;                           " output if VSX from Xport "
VSX      =  VSD ;                                    " option: VSX = FID "
VSX.OE   =  DENC ;                                   " VSD/FID pass back "

                                            " === REGISTER & CLOCK === "
HS2      .SET     =  1 ;                        "  declarations  "
HS2      .CLK     =  PIXCLK ;
CPHASE   .SET     =  1  ;                       " u/v multiplex phase "
CPHASE   .CLK     =  PIXCLK ;                   " for color pattern    "
FID      .SET     =  1 ;
FID      .CLK     =  PIXCLK ;                " auxiliary output state "
FID .J   =  FIDJ ;
FID .K   =  FIDK ;
VQ[2..0].SET      =  1 ;
VQ[2..0].CLK      =  PIXCLK ;                 " state machine register "
FSGO     .SET     =  1 ;
FSGO     .CLK     =  PIXCLK ;                 " output state register "

                                              "= COLOR TEST PATTERN = "
                        " vertical color pattern in YUV 4:2:2 space"
                        " ---------------------------------------- "
PATL[7..4] = /COUNT[8..5] ;                          " 14 grey values "
PATL[3..0] = FH ;                                    "  (CCIR offset) "
CPHASE.J    = 1  ;                            " cphase = phase of U/V "
CPHASE.K    = /H1C    ;                       " toggles, reset at H1C "
PATC[7..4] =    CPHASE * PATU[7..4]                  " def. of MSBs of"
            + /CPHASE * PATV[7..4] ;                 " U & V pattern  "
PATC[3..0] = 0H ;                                    " see truthtable "

IDB[7..1].ID   = BY [7..1] ;                  " luminance background  "
LUMA[6..0]     = IDB[7..1] ;                  " ==================    "
LUMA7    =        LUMA6 ;                     " sign extension        "
IDB[7..1].CLK = CLKB ;
```

```
IDA[7..1].ID  = BUV[7..1] ;                " color diff. background"
COLR[6..0]    = IDA[7..1] ;                " ====================="
COLR7         = COLR6 ;                    " sign extension        "
IDA[7..1].CLK = CLKA ;

                                           "=== MTV RGB OVERLAY ==="
OVLCTRL.D =    VCTRL ;
MPK        =  OVLCTRL ;
OVLG       =  MTVG ;     " IDB0 "          "  100% saturation 75%  "
OVLB       =  MTVB ;     " IDA0 "          " dec   hex  :  dec   hex "
BLACK[7..0] =  10H ;                       "  16    10  :   16    10 "
GREEN[7..0] =  EBH ;                       " 235    EB  :  191    BF "
BLUE [7..0] =  EBH ;                       " 235    EB  :  191    BF "
OVLGREEN[7..0] = VCTRL                  " green overlay foreground "
                * ( /OVLG * BLACK[7..0]
                   + OVLG * GREEN[7..0] );
OVLBLUE[7..0] = VCTRL                    " blue overlay foreground "
                * ( /OVLB * BLACK[7..0]
                   + OVLB * BLUE [7..0] );
OVLCTRL .SET = 1 ;
OVLCTRL .CLK = PIXCLK ;

                                               " ===DATA OUTPUT ==="
Y [7..0].OD    =  /OVLCTRL * ( PATTERN * PATL[7..0]
                             + XPORT * LUMA[7..0] )
               +  OVLGREEN[7..0] ;
UV[7..0].OD    =  /OVLCTRL * ( PATTERN * PATC[7..0]
                             + XPORT * COLR[7..0] )
               +  OVLBLUE[7..0] ;
Y [7..0].CLK   =  CLKE2 ;
UV[7..0].CLK   =  CLKE1 ;
YW [7..0]      =   Y [7..0] ;
UVW[7..0]      =   UV[7..0] ;
YW [7..0].OE   =  /WINDOW * /MUTE ;
UVW[7..0].OE   =  /WINDOW * /MUTE ;
```

```
@INPUT VECTORS                                   " for vertical states     "
        [ VSI,HS2,H1C,VWB,V13,FID,INL2FB ]
VSODD   =  0   0   -   -   -   -  - B;   " trailing VS edge -->O "
VSEVN   =  0   1   -   -   -   -  - B;   "       in 2nd hl --> E "
VWBHL2  =  -   1   -   1   -   -  - B;   " VWB in 2nd half line  "
HL1P    =  -   0   -   -   -   -  0 B;   " next line : pulse fsgo"
HL1E    =  -   0   -   -   -   0  1 B;   " next line : ldevn     "
HL1O    =  -   0   -   -   -   1  1 B;   " next line : ldodd     "
HC1P    =  -   -   1   -   -   -  0 B;   " H clock : clear pulse "
HC1     =  -   -   1   -   -   -  1 B;   " H clock :  keep fsgo  "
VSOB    =  -   -   -   -   1   -  - B;   " start VS out, to DENC "
VSIP    =  1   -   -   -   -   -  - B;   " VS pulse from source  "

@OUTPUT VECTORS
        [ FIDJ,FIDK,COUNTRST ]              " field ID register        "
FIDODD  =   1     0     1    B;             "  first field = odd   = 1 "
FIDEVN  =   0     1     1    B;             " second field = even = 0 "
        [ FSGO ]                      " vertical window indicator, reg"
GOPULSE =  1  B;
GOCLEAR =  0  B;
FSODD   =  1  B;
FSEVN   =  0  B;

@STATE VECTORS
        [ VQ2,VQ1,VQ0 ]               " vertical states                "
VS      =  0   0   0  B;              " vertical sync at input         "
IDLETOP =  0   0   1  B;              " before vertical window begin  "
VWB0    =  0   1   0  B;              " 2nd half line, to reset read p"
VWB1    =  0   1   1  B;              " flag window start, rise/change"
IDLEBOT =  1   0   0  B;              " after window begin, till VS   "
VSO     =  1   0   1  B;              " generate vertical sync output "

@TRANSITIONS
WHILE [VS]
   IF    [VSODD] WITH [FIDODD]    THEN [IDLETOP]
   IF    [VSEVN] WITH [FIDEVN]    THEN [IDLETOP]
WHILE [IDLETOP]
   IF    [VWBHL2]                 THEN [VWB0]
WHILE [VWB0]
   IF    [HL1P]                   THEN [VWB1]      WITH [GOPULSE]
   IF    [HL1E]                   THEN [VWB1]      WITH [FSEVN]
   IF    [HL1O]                   THEN [VWB1]      WITH [FSODD]
WHILE [VWB1]
   IF    [HC1P]                   THEN [IDLEBOT]   WITH [GOCLEAR]
   IF    [HC1]                    THEN [IDLEBOT]
WHILE [IDLEBOT]
   IF    [VSOB]                   THEN [VSO]
   IF    [VSIP]                   THEN [VS]
WHILE [VSO]
   IF    [VSIP]                   THEN [VS]
```

```
        " READHB :    horizontal definition of display window "
        " ==========    horizontal test signal generation, HS2  "
        " PML2552-35    memory read control, FBBID, window      "
        "               data path check for eol/eof/key marker  "
        " U36           data path gating, de-serializing, OE    "

@PINLIST

CLKA     I ;          " MEMREAD, memory read clock, pixel clock,
                        for byte-serial-mode, this is 2* pixel-clk"
CLKB     I ;          " pixel clock, also for internal count      "
CLKE2    I ;          " pixel clock, same as LDV, for YW,
                                        for output, i.e. display  "
CLKE1    I ;          " for UVW, parallel-mode: same as LDV = clke2
                        serial-mode: clkel = /LDV, i.e.like clkin;
                        half period shifted clock = inverted clock"

GO[7..0]   I ;            " luma input channel, Y,Green, or serial"
BO[7..0]   I ;            " color diff. input channel, UV, Blue   "
HOS[8..1]  I ;            " Horizontal OffSet of inserted window  "
YW[7..0]   O "B" ;        " luminance output, respectively Green  "
UVW[7..0]  O "B" ;        " colour difference, resp. Blue         "

HSD      I "B" ;          " HSN of DENC, horiz.sync,   active LOW "
HS2RD    O ;              " 1st half line LOW, 2nd half line HIGH "
RE1      O ;              " read enable FRAM bank 1               "
RE2      O ;              " read enable FRAM bank 2               "
MUTE     I ;              " from external, tristates data outputs "
FSGO     I ;              " indicates vertical start of window    "
                          " interlaced output (view1=0):
                                  FSGO changes to FID at VW-start "
                          " non-interl.output (view1=1):
                                  FSGO = line pulse at VW-start   "
WINDOW   O ;              " active (H) during inserted signal     "

VIEW0    I ;              " byte-parallel = 0, byte-serial = 1    "
VIEW1    I ;              " field toggle = 0, i.e. for interlaced
                             line toggle = 1, i.e. for non-interl."
VIEW2    I ;              " background/test signal mode:
                            window only (0), ramp test signal (1) "
VIEW3    I ;              " 0 = default; (1) not used in this prog.
                            reserved for optional mode variations "
VCTRL    I ;              " RGB overlay from MTV micro controller "

@GROUPS
EOLMARK = [ 0,0,0,0, 0,0,0,0 ] ;          " end of line marker  "
EOFMARK = [ 1,1,1,1, 1,1,1,1 ] ;          " end of field marker "
KEYMARK = [ 0,0,0,0, 0,0,0,1 ] ;          " color key marker,i.e.
                                            a transparent pixel "

@TRUTHTABLE
```

```
@LOGIC EQUATIONS
                                              " === HORIZONTAL COUNT === "
PIXCLK  =   CLKB  ;
COUNT[9..0].RST = /COUNTRST ;                    " .rst guides snap       "
COUNT[9..0].J    = 1   ;                         " 10 * JKCL552 with      "
COUNT[9..0].K    = 1   ;                         " individual clock       "
COUNT0.CLK = /PIXCLK ;
COUNT1.CLK = /(PIXCLK * COUNT0) ;
COUNT2.CLK = /(PIXCLK * COUNT0*COUNT1) ;
COUNT3.CLK = /(PIXCLK * COUNT0*COUNT1*COUNT2) ;
COUNT4.CLK = /(PIXCLK * COUNT0*COUNT1*COUNT2*COUNT3) ;
COUNT5.CLK = /(PIXCLK * COUNT0*COUNT1*COUNT2*COUNT3*COUNT4) ;
COUNT6.CLK = /(PIXCLK * COUNT0*COUNT1*COUNT2*COUNT3*COUNT4
                       *COUNT5) ;
COUNT7.CLK = /(PIXCLK * COUNT0*COUNT1*COUNT2*COUNT3*COUNT4
                       *COUNT5*COUNT6) ;
COUNT8.CLK = /(PIXCLK * COUNT0*COUNT1*COUNT2*COUNT3*COUNT4
                       *COUNT5*COUNT6*COUNT7) ;
COUNT9.CLK = /(PIXCLK * COUNT0*COUNT1*COUNT2*COUNT3*COUNT4
                       *COUNT5*COUNT6*COUNT7*COUNT8) ;


                                             " === HORIZONTAL EVENTS === "
HOS9     =  0 ;
HOS0     =  1 ;                              " to adjust for uv-sequence "
HWB      =  COUNT[9..0] == HOS[9..0] ;
HBL.D    =  /HSD ;                              " HBL: horiz. blanking "
HBLE     =  HSD * HBL ;                         " HBLE: blanking end   "
COUNTRST = HBLE ;
LLENGTH[10..0] =  30BH ;          " 60 Hz, SQP:  780-1 = 30B hex "
                                  " 50 Hz, SQP:  944-1 = 3AF hex "
                                  " 60 Hz, CCIR: 858-1 = 359 hex "
                                  " 50 Hz, CCIR: 864-1 = 35F hex "
HALFLINE = COUNT[9..0] == LLENGTH[10..1] ;           " half line "
HS2RD.J =  HALFLINE ;                                " set       "
HS2RD.K =  COUNTRST ;                                " clear     "


HBL      .CLK    =  PIXCLK ;         " === REGISTER & CLOCKS === "
HS2RD    .CLK    =  PIXCLK;              "    declarations    "
WINDOW   .CLK    =  PIXCLK;
RQ[2..0].CLK     =  PIXCLK ;
FBBID    .CLK    =  PIXCLK ;
HBL      .SET = 1;
HS2RD    .SET = 1;
WINDOW   .SET = 1;
RQ[2..0].SET = 1;                            " state registers "
FBBID    .SET = 1;                   " auxiliary state register "
```

```
                                              " === CONTROL & OUT === "
EOL       =  IDA[7..0] == EOLMARK ;
EOF       =  IDA[7..0] == EOFMARK ;
KEY       =  IDA[7..0] == KEYMARK ;          " transparent pixel,    "
TPIX      =  EOL + EOF + KEY ;               " not a pixel to display"
INTRL     =  /VIEW1 ;                        " interlaced display    "
FBBID    .J    = FBBIDJ ;                    " set and toggle        "
FBBID    .K    = FBBIDK ;                    "control by statemachine"
RE1       =  RE *  FBBID ;                   " when and where enable "
RE2       =  RE * /FBBID ;                   "   to read from memory "
WINDR     =  /RQ2*RQ1*RQ0 ;                  " have read data        "
WINDO     =  WINDR * /TPIX ;                 " have data for output  "
WINDT     =  RQ2 ;                           " add.test signal region"
WINDOW.D = /VCTRL * (          WINDO            "data path out enable"
                     + VIEW2 * WINDT);          " - with test signal "
DPOE      = WINDOW * /MUTE ;                 " .. but not if MUTE .. "

                                              " === TEST  PATTERN === "
PATL[7..0] = /COUNT9*/COUNT8 * 80H                       " flat grey "
           +          COUNT8 * COUNT[7..0]               " grey ramp "
           + COUNT9          * COUNT[1..8] ;             " oscillat. "
PATC[7..0] =         /COUNT8 * COUNT[7..0]               " color ramp"
           +          COUNT8 * 80H ;                     " no color  "


                                            " === DATA PATH THRU === "
PARALLEL = /VIEW0 ;
SERIAL   =  VIEW0 ;
IDA[7..0].ID   =  GO[7..0] ;       " IDA carries also byte-serial "
IDA[7..0].CLK =  CLKA ;    " in serial-mode: double pixel clock "
IDB[7..0].ID   =  BO[7..0] ;
IDB[7..0].CLK =  CLKB ;
Y  [7..0].OD   =  /WINDR * PATL[7..0]
                 + WINDR *  IDA[7..0] ;
UV [7..0].OD   =  /WINDR * PATC[7..0]
                 + WINDR * ( PARALLEL * IDB[7..0]
                           + SERIAL   * IDA[7..0] ) ;
Y  [7..0].CLK =  CLKE2 ;                    " regular pixel clock  "
UV [7..0].CLK =  CLKE1 ;  " in serial-mode: inverted pixel clock"
YW [7..0]      =  Y [7..0] ;
UVW[7..0]      =  UV[7..0] ;
YW [7..0].OE   =  DPOE ;
UVW[7..0].OE   =  DPOE ;
```

```
@INPUT VECTORS
        [ FSGO, HBL, HWB, EOL, EOF, INTRL ]
RIBO    =   1    1    -    -    -     -  B;   " also FSGO line p"
RIBE    =   0    1    -    -    -     -  B;
START   =   -    -    1    -    -     -  B;
LINE    =   -    0    -    -    -     -  B;
HBLK    =   -    1    -    -    -     -  B;
NONE    =   -    0    -    0    0     -  B;
BLANK   =   -    1    -    0    0     -  B;
STOPHI  =   -    -    -    1    -     1  B;
STOPHN  =   -    -    -    1    -     0  B;   "fbbid line toggle "
STOPOI  =   1    -    -    -    1     1  B;   "fbbid field toggle"
STOPON  =   1    -    -    -    1     0  B;
STOPE   =   0    -    -    -    1     -  B;   " set fbbid anyhow "

@OUTPUT VECTORS
        [ RE,FBBIDJ,FBBIDK ]      " FBBID : where to read from     "
READ    = 1    0      0    B;     " RE    : when to enable read    "
TOGGLE  = 0    1      1    B;     " line (NIL2FB) or field toggle "
FBBODD  = 0    1      0    B;     " reset to odd field buffer bank"

@STATE VECTORS
        [ RQ2,RQ1,RQ0 ]                     " === for WINACT === "
PAUSE   = 0   0   0   B;
IDLO    = 0   0   1   B;
IDLE    = 0   1   0   B;                    " display zones and "
WINACT  = 0   1   1   B;                    " window generation "
RIBBON  = 1   0   0   B;
FIRST   = 1   0   1   B;                    " read 1st tristate "
WBLK1   = 1   1   0   B;                    " check for eol, eof"
LAST1   = 1   1   1   B;                    " check for eof     "
```

```
@TRANSITIONS

WHILE [IDLE]                                      " for parity,         "
   IF    [RIBO]  WITH [READ]  THEN  [RIBBON] " throw a pixel away"
WHILE [IDLO]
   IF    [RIBE]               THEN  [RIBBON]
WHILE [RIBBON]
   IF    [START] WITH [READ]  THEN  [FIRST]
                                          " don't look for eol "
WHILE [FIRST]          " still rubbish in pipe from tristate FB "
   IF    []      WITH [READ]  THEN  [WINACT]

WHILE [WINACT]
   IF    [NONE]   WITH [READ]     THEN   [WINACT]
   IF    [STOPHI]                 THEN   [LAST1]   " last pixel + 1 "
   IF    [STOPHN] WITH [TOGGLE]   THEN   [LAST1]
   IF    [STOPOI] WITH [TOGGLE]   THEN   [IDLO]
   IF    [STOPON]                 THEN   [IDLO]
   IF    [STOPE]  WITH [FBBODD]   THEN   [IDLE]
   IF    [BLANK]                  THEN   [WBLK1]   " if no eol, oef "

WHILE [WBLK1]     " check 1 more 'read' in the pipe for eol, eof "
   IF    [STOPHI]                 THEN   [LAST1]   " last pixel + 1 "
   IF    [STOPHN] WITH [TOGGLE]   THEN   [LAST1]
   IF    [STOPOI] WITH [TOGGLE]   THEN   [IDLO]
   IF    [STOPON]                 THEN   [IDLO]
   IF    [STOPE]  WITH [FBBODD]   THEN   [IDLE]
   ELSE                                  [PAUSE]

WHILE [LAST1]                          " check last+1 'read' for eof "
     "last+1 pixel = first pixel of next line, lost in the pipe "
   IF    [STOPOI] WITH [TOGGLE]   THEN   [IDLO]
   IF    [STOPON]                 THEN   [IDLO]
   IF    [STOPE]  WITH [FBBODD]   THEN   [IDLE]
   ELSE                                  [RIBBON]

WHILE [PAUSE]
   IF    [LINE]  WITH [READ]  THEN  [FIRST]
```

Crystal specifications

The Philips line of digital decoders requires crystals which meet specific specifications. Picking a crystal vendor solely on the basis of frequency will not guarantee satisfactory performance.

Operational failures that could be related to crystal dysfunction are:

1. Inability to achieve line lock (horizontal lock)
2. Inability to achieve chroma lock
3. Slowness of lock acquisition.

The crystal specifications are:

Nominal frequency:	26.800000MHz (square pixel decoders) 24.576000MHz (CCIR decoders)
Load capacitance C_l:	8pf
Adjustment tolerance:	±40ppm
Resonance resistance R_r:	50 Ω (square pixel) 60 Ω (CCIR)
Drive level dependency:	80 Ω
Motional capacitance C_1:	1.1 fF (square pixel) 1.0 fF (CCIR)
Parallel capacitance C_o:	3.5 pF (square pixel) 3.3 pF (CCIR)
Temperature range T_0:	0 to 70 °Celsius
Frequency stability:	±20ppm

The Philips part numbers for these crystals are:
9922 520 30004 for the square pixel systems (26.800000MHz)
9922 520 30009 for the CCIR system (24.576000MHz)

The Philips crystals can be obtained from:
Philips Components Passive Group, phone: (803) 772-2500

The crystals are also available from Ecliptek. Their part numbers are:
ECX-2194-26.800MHz and
ECX-2097-24.576MHz
Ecliptek can be reached at (714) 433-1200. The contact sales representative is Rodney Mills.

TDA8708 black level and gain modulation circuit

Author: Herb Kniess

The Philips TDA8708 8-bit A/D converter digitizes video signals and contains black level and automatic gain control circuits. The binary levels for sync and black are internally fixed in the device. Sync tip is maintained at 00H and black level is maintained at 40H. It may be desirable to allow manual override of these automatic features. The following circuit describes a method for overriding the automatic features of the TDA8708 as well as retaining them.

MANUAL GAIN CONTROL

Normal operation and connections of the TDA8708 are shown on page 2 of the schematic when it is used in conjunction with the Philips SAA71XX series Digital Video Decoders. The only changes to the normal circuit are made through connections labeled "Black" and "Gain." Normally, a capacitor is connected to ground at Pin 25 of the data converter. This capacitor holds a charge dependent on the level of the input video signal and the control voltage necessary at Pin 25 to maintain sync level of 00H. Currents near 50-100 microamps are generated within the converter during horizontal blanking times to charge or discharge the capacitor as necessary, in order to maintain the preset binary output levels of the converter. The voltage on Pin 25 controls the gain of the input amplifier of the converter.

A similar circuit and current source is implemented on Pin 24. However, its only function is to provide the proper DC offset voltage necessary to maintain the black level at 40H regardless of changes of input signals or bias changes on input pins 16, 17, or 18.

Under normal operation, the data converter binary outputs are maintained at precise digital values.

Page 1 of the application schematic shows that the gain connection to Pin 5 of the TDA8708 is connected to capacitor C1 via an analog switch at U2. During horizontal blanking time the analog switch maintains a connection from Pin 25 of the converter to capacitor. Thus, sync levels are maintained via the automatic circuits in the converter. However, if necessary, the control voltage on Pin 25 can be switched to the input voltage at Pin 12 of analog U2 switch during the active video time of each scan line. DAC7 of U1 and bias resistors R1, R2, and R3 provide a variable control voltage for manual control of gain only during the active video portion of the scan line.

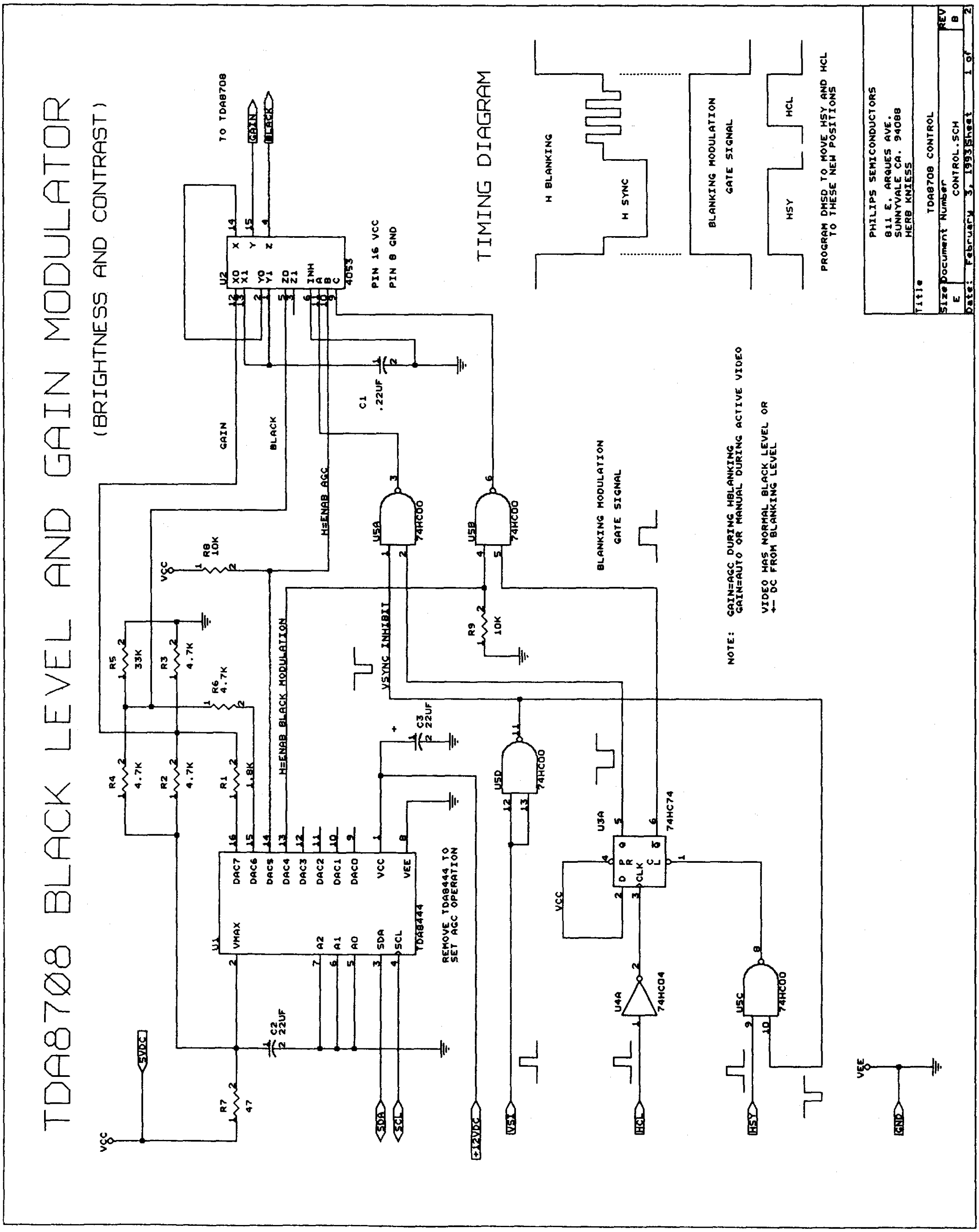
The bandwidth of the control voltage on Pin 25 of the converter can be as high as 5 Mhz so that a precise match of the timing of the gain change is possible at the beginning and ending of blanking times. Noise on the gain control pin must be kept to a minimum in order to avoid AM modulation of the input video signal. The digital decoder can be reprogrammed to adjust the timing of the HCL and HSY timing signals to carefully match the timing diagram of page 1 of the schematic. Refer to the TDA8708 data sheet for a discussion of the operation of these signals in the TDA8708. Do not worry that the modified positions of the HSY and HCL signals might affect the operation of the converter. They will not because the change in position is small compared to the overall width of the pulses. For optimum performance, the beginning and ending of the gate signal at Pins 5 and 6 of U3 should be set within the minimum blanking time of any signal being digitized.

BLACK LEVEL CONTROL

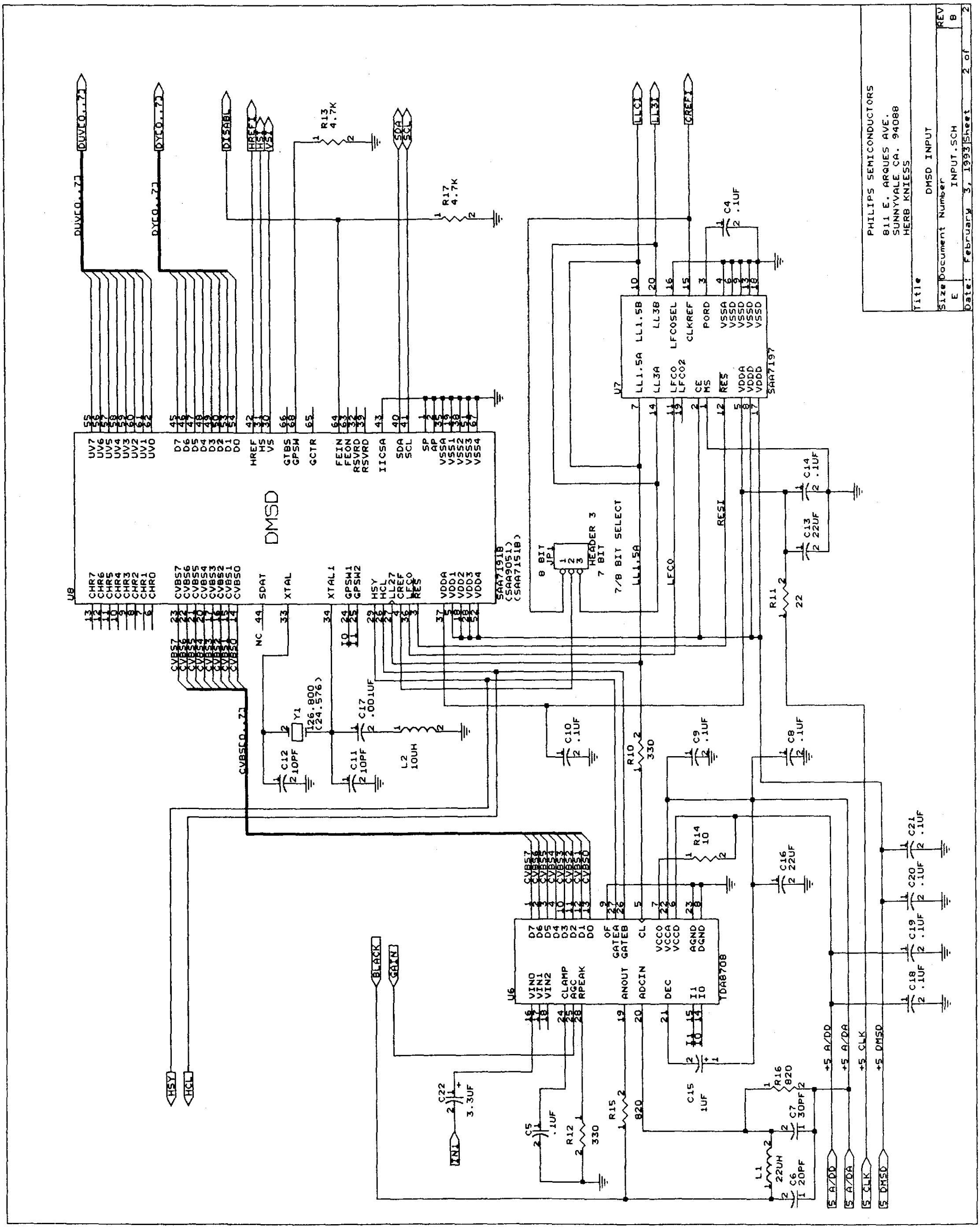
Analog switch U2 provides another function besides control of the gain voltage at Pin 25 of the TDA8708 converter. It can be switched to inject a DC pulse on Pin 4 to R15 at Pin 19 of the data converter. Pin 19 is the video output of the input amplifier of the TDA8708. It is nominally about 1V PP. If a DC pulse is added to the video signal at R15 during active video time, the DC level between blanking and active video can be modified. The data converter still provides a constant black level of 40H during blanking time but the data converter can produce other levels for black during active video depending on the polarity and level of the injected signal. DAC6 and bias resistors R6, R4, and R5 provide a variable bias at Pin 5 of U2, which is gated onto the video signal by gate pulse at Pin 3 of U5.

It is desirable to inhibit the modulation of black and gain signals during the vertical sync area so that proper integration of the vertical sync will be maintained by processing circuits. This is accomplished by VSYNC INHIBIT at Pin 11 of U5. Additional control functions are provided by logic levels of DAC5 and DAC4, which turn on and off the black level and gain modification signals at U2. It should be noted that different bias resistors can be selected on DAC7 and DAC6 pins to affect the allowable range of control but the DAC full range of 00H to 3FH should be used in order to give the finest degree of control.

TDA8708 black level and gain modulation circuit



TDA8708 black level and gain modulation circuit



TDA9141 analog decoder application

Author: George Ellis

OVERVIEW

Analog solutions for video decoding and digitization are available in addition to the digital methods mentioned elsewhere in this book. The individual components are generally of lower cost; however, trade-offs with regard to the total number of components to perform a specific function must be considered.

SYSTEM CONFIGURATION

This application is divided into four blocks:

1. Analog video to analog YUV decoding
2. A/D converter with clock and support circuitry
3. Level control circuit for block 2
4. Optional RGB output block

Various elements of this application need not be used if not called for by the application. The intent here is to demonstrate a full featured solution.

DECODER

Composite, S-video, or analog RGB can be input to the Philips TDA9141 multi-standard decoder. This device, in conjunction with the TDA4661 delay line, will decode the NTSC, Pal and Secam standards, and output them as analog Y (luma) and UV (chroma) outputs. The luma-to-chroma delay is matched; therefore, no luminance delay line is necessary. If NTSC is desired exclusively, the TDA4661 delay line need not be used.

The delay line is used as a chroma comb filter for NTSC, and although not strictly required, it does reduce undesirable cross-color effects. Note that unlike older delay lines that work in the subcarrier base-band, the TDA4661 works in the demodulated UV color-difference band, and is implemented with charged-coupled technology instead of using a bulky glass delay line.

Optional color transient improvement and peaking can be applied to the YUV signal by use of the TDA4670; again, this may be deleted in a no-frills application.

Two comparators are used to extract horizontal blanking and clamp signals from the sandcastle pulse generated by the TDA9141, and are used for the A/D converters. The TDA9141 also outputs a line-locked 6.75MHz clock that is used in the conversion process.

The decoder and color transient device are controlled via the IIC two-line interface bus. The decoder can be programmed for automatic detection of the three video standards.

A/D CONVERSION AND CLOCK

The analog Y, U, and V signals are applied as AC coupled inputs to three TDA8709 A/D converters. Gain controls for all three converters and a black level control for the Y converter are provided by the level control block.

The Clamp Select pin (pin 27) is set to adjust the DC level of the U and V converters to a value corresponding to decimal value 128 during the application of the positive clamp pulse derived from the decoder block. The Clamp Select pin of the Y converter is set to force the DC input level to correspond to a value of decimal 16. This sets the converters to the appropriate digital value during blanking.

Each converter is capable of selecting one of three inputs applied, and a simple low-pass filter is inserted between the selected signal and the A/D input to remove any possible high frequency noise that could cause aliasing effects.

The 6.75MHz clock from the TDA9141 is a low level sawtooth with an amplitude of about 1 Vpp. This signal is very similar to the LFCO signal available from the digital chip decoders, thereby making it possible to generate 13.5MHz, 27MHz, and CREF signals using the same device as that used by the digital chip set, the SAA7197.

The UV bandwidth is one half the 13.5MHz luma bandwidth, therefore, the 13.5MHz clock is divided by two. The 13.5MHz signal and the CREF signal are delayed to match the delay introduced in producing the 6.75 clock.

The 6.75 clock is used for the conversion process of the U and V converters and for the multiplexers that follow. This results in one UV pair for every two luminance samples. The outputs of the multiplexers and the luma A/D converter are latched with D flip-flops using the 13.5 clock.

The resulting digital format is the 16 bit 4:2:2 format used by various digital systems, including the Philips video scaler (SAA7186) and encoder (SAA7199B). This is also an efficient storage mode for video as it uses 16 bit wide memory structures instead of 24.

A new triple input YUV A/D converter has been added to the Philips line, the TDA8758, which outputs the 4:2:2 format; however, it will not be available until the end of 1993, and therefore has not been included in the handbook.

LEVEL CONTROL

An IIC controllable level control circuit is achieved using a TDA8444 6-bit octal DAC to produce DC control of the gain control inputs of the data converters. A fourth DAC output is gated to be applied only during blanking, and is added to the Y input signal to produce a DC offset of the luma signal, thus allowing control over the black level. These DC levels could as easily be derived from resistors instead of the DAC, for use in systems that have these parameters preset at the factory.

RGB OUTPUT AND YUV BUFFER STAGE

If YUV to RGB conversion is necessary for output to a monitor or for RGB digitizing, the TDA4686 is useful. This device has a YUV to RGB analog matrix with two additional RGB inputs that can be switched in at a pixel-by-pixel rate.

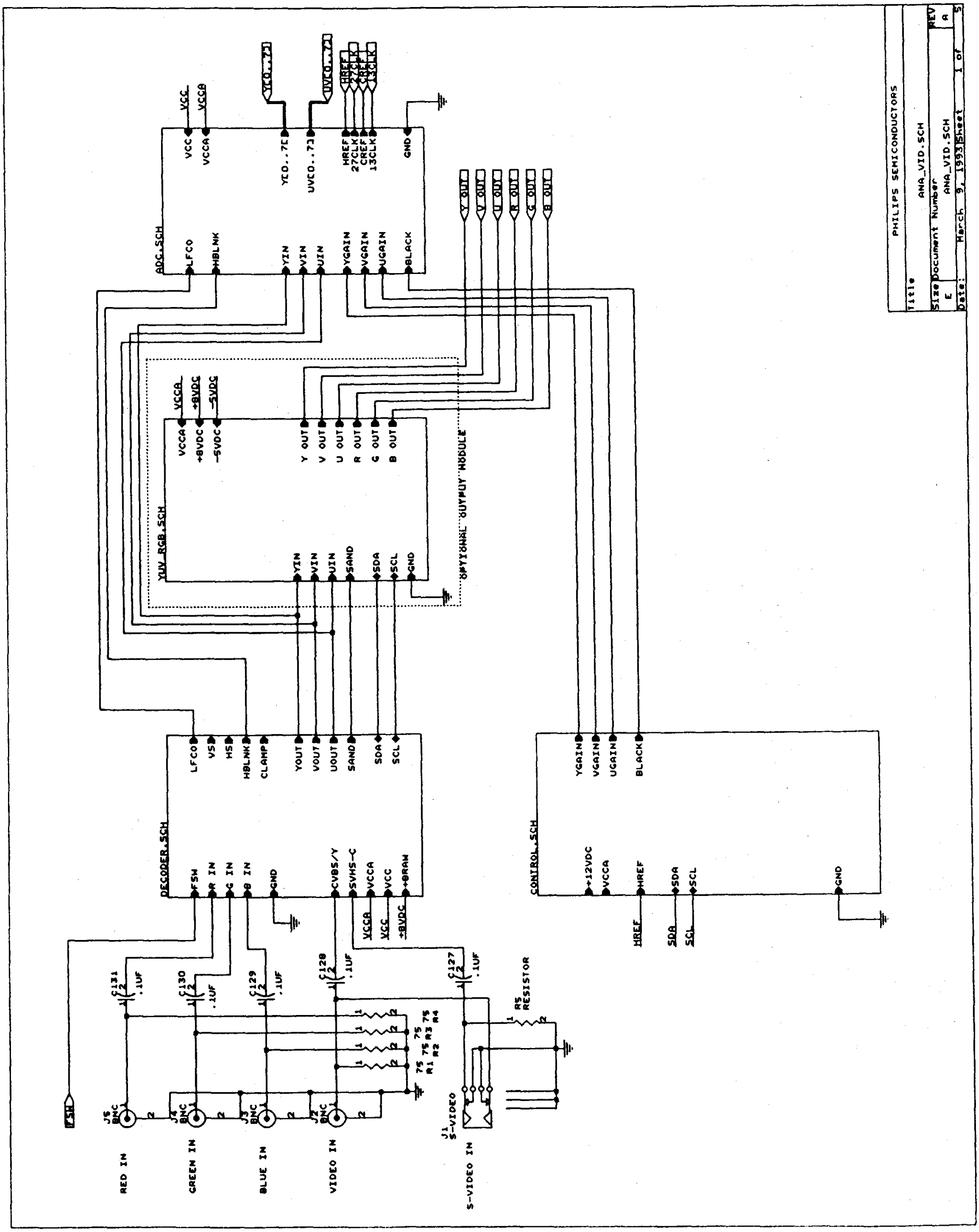
The circuit shown here will drive an analog RGB monitor with 75 Ω loading. It may also be used to drive the inputs of three RGB digitizing A/D converters (same circuit as the Y converter, times three). Because the TDA4686 has brightness, contrast, and saturation controls via IIC bus, the input circuit previously described would not be necessary, as all gain and black level adjustments can be made with the TDA4686.

If YUV analog component video output is desired, the YUV levels that are input to the TDA4686 can be buffered by high speed op amps to drive 75 Ω loads. For component video, the output levels are set to .7 Vpp for full scale U, V, and non-composite Y (Y without sync) driven into 75 Ω. A series resistor is needed to match the cable impedance and the driven device would have a 75 Ω termination load. This requires that the gain of the op amps be set such that full scale output is 1.4 Vpp before the series matching resistor.

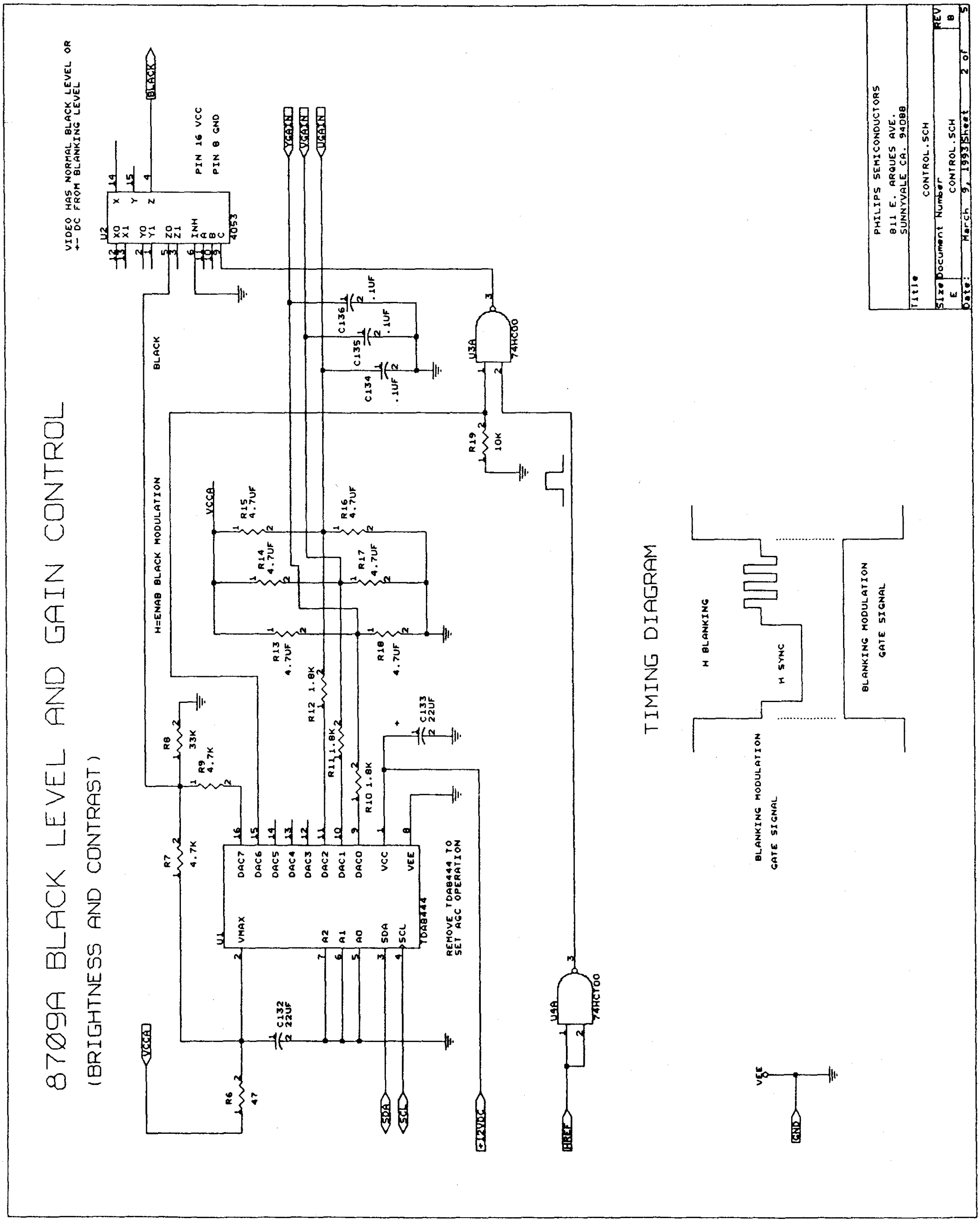
SUMMARY

Full featured desktop video solutions can generally be met with far fewer parts if a digital chip set is used. This is due to the fact that these digital solutions were designed for this market, where the analog methods were originally designed for consumer (TV) applications where there is no requirement for digitization and data format. There are, however, many low end applications where various portions of this application could be useful.

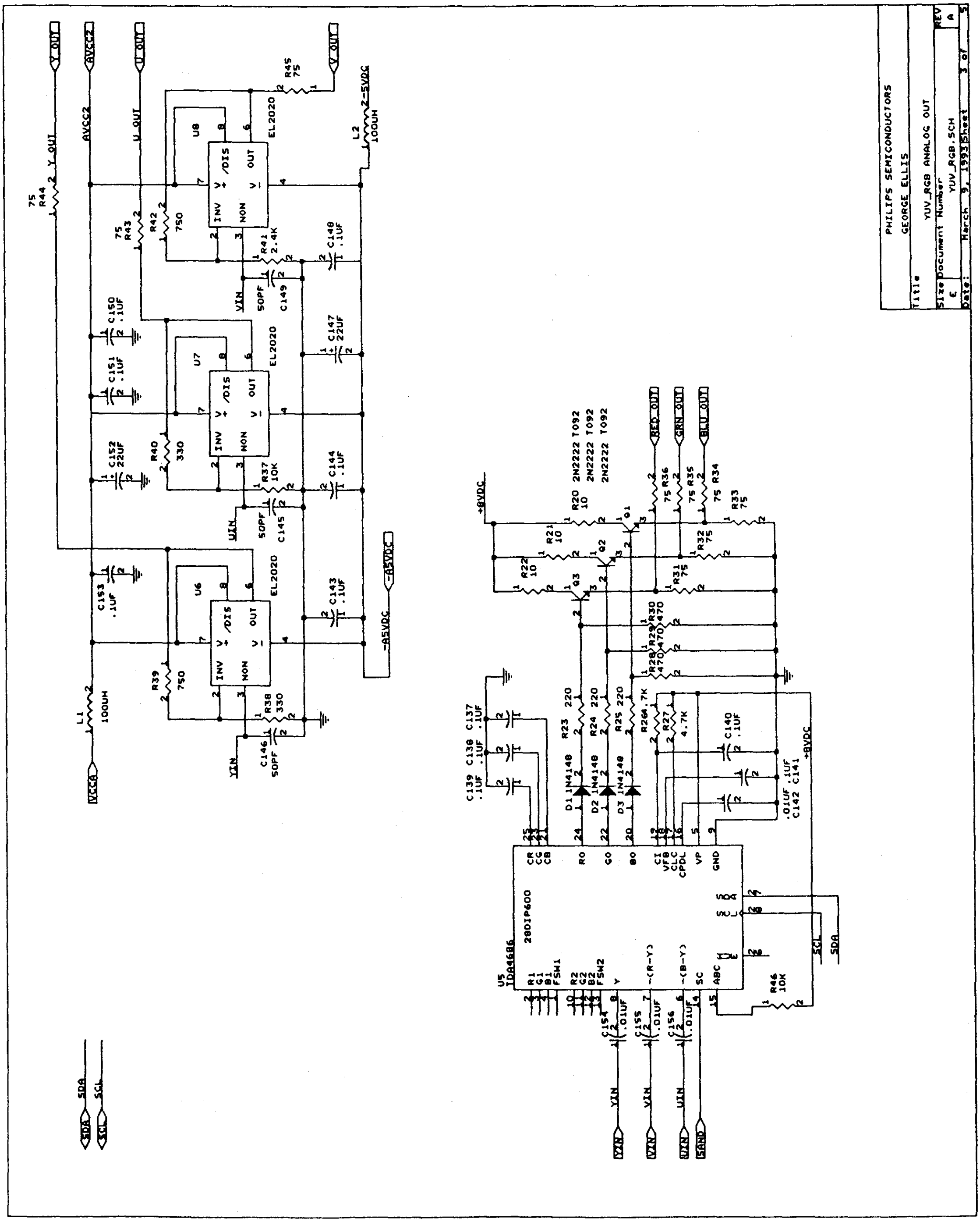
TDA9141 analog decoder application



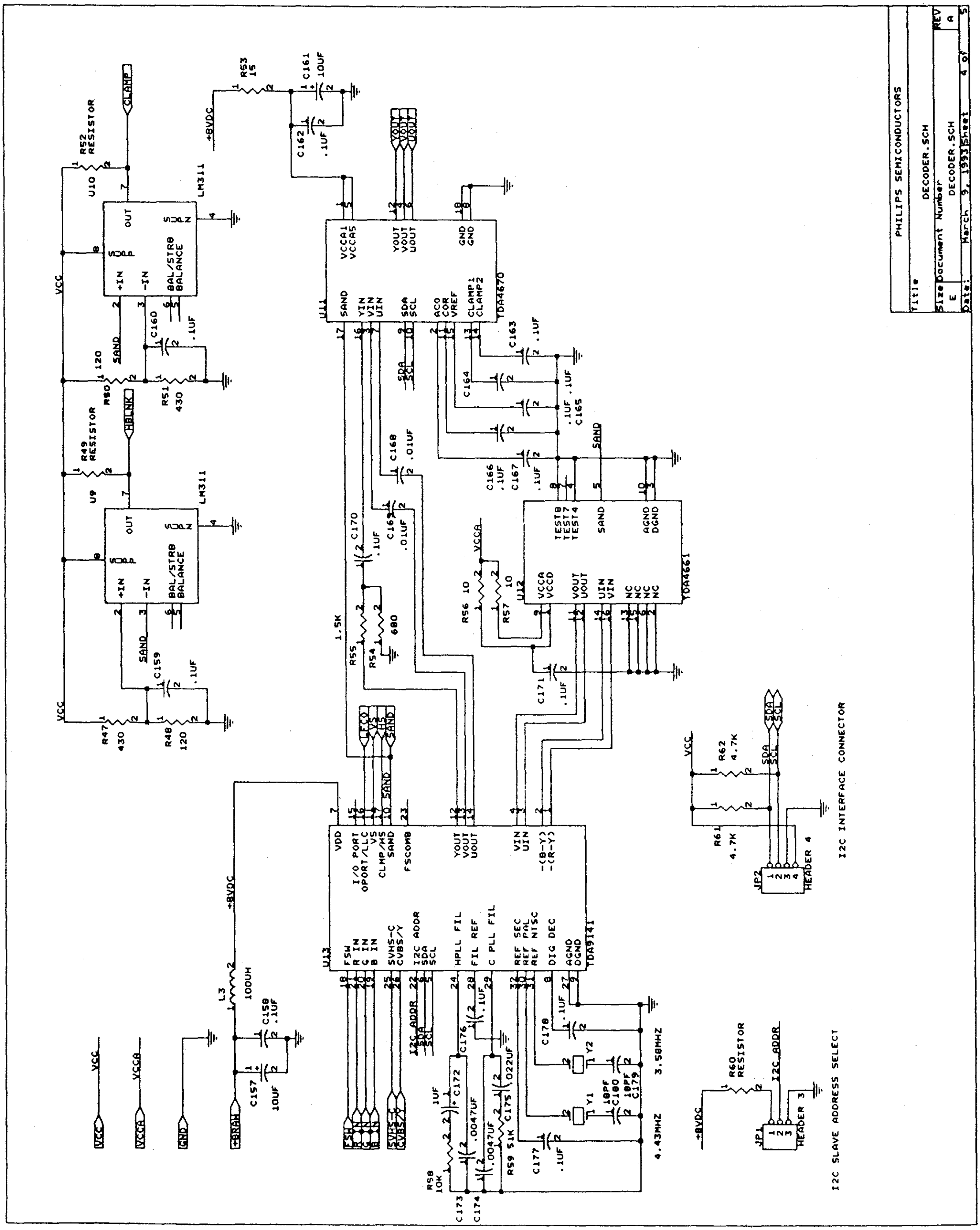
TDA9141 analog decoder application



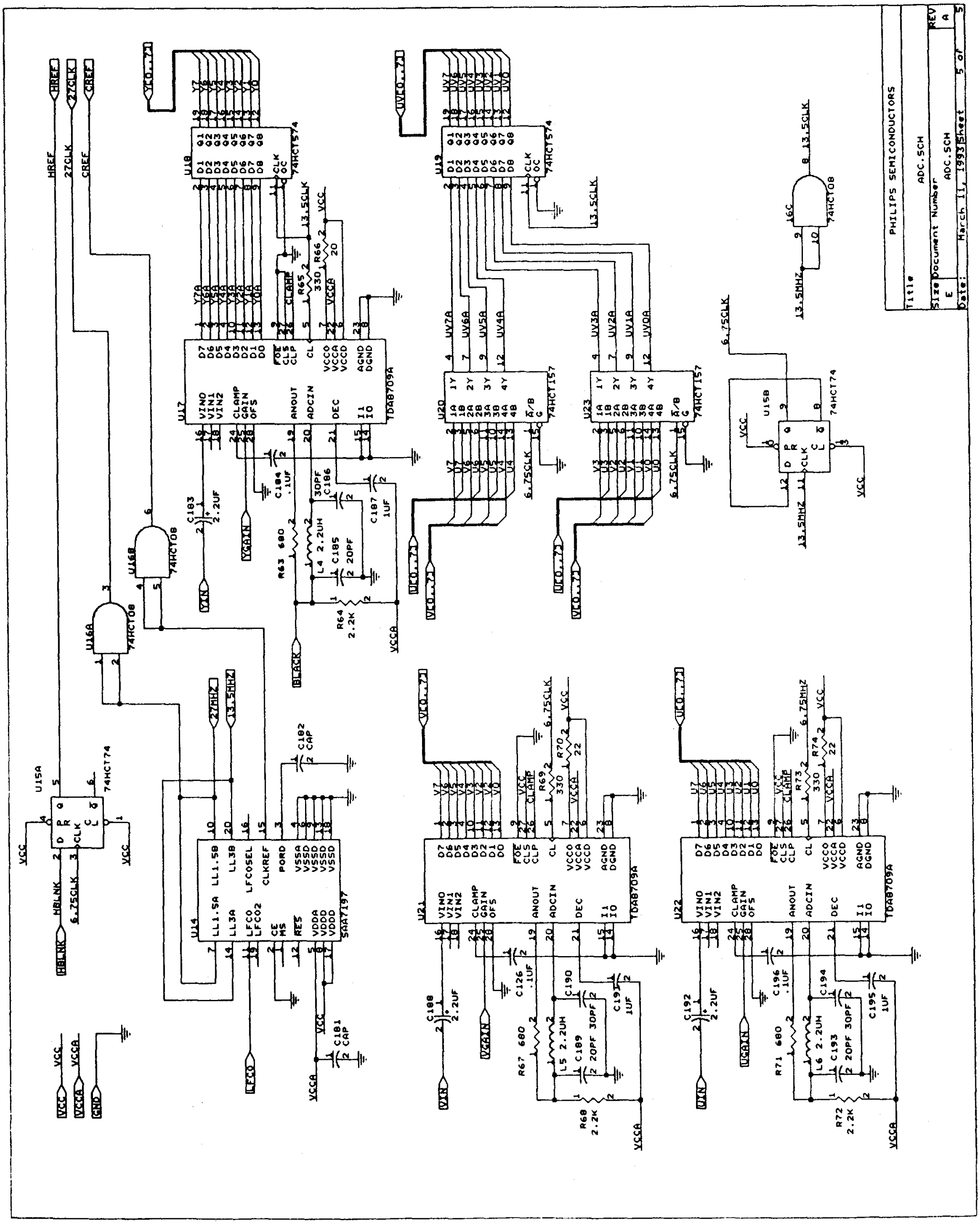
TDA9141 analog decoder application



TDA9141 analog decoder application



TDA9141 analog decoder application



Digital video evaluation board

Author: George Ellis

OVERVIEW

In order to individually evaluate the Philips digital video encoding and video DAC systems, the SAA7199B and SAA7165 (SAA9065) chips, respectively, a demo board was developed that is capable of receiving digital data from a broadcast quality video test generator.

This board receives input in the D1 digital video format, converts the data to the 16 bit 422 data format used by the Philips system, and produces the clocks and sync signals necessary to drive the encoder and video DAC. The board generates analog composite video and S-video using the SAA7199B digital encoder, and it produces analog YUV (Y, Cb, Cr) using the SAA7165. It also converts the analog YUV into analog RGB using the TDA4686, thus demonstrating a complete digital-to-analog video output solution.

D1 DIGITAL VIDEO FORMAT

D1 digital video (parallel mode) is an industry standard used to transfer video without any loss of quality. Being digital in nature, this signal can be duplicated indefinitely, and therefore is used in many broadcast production facilities.

D1 is transferred as a nine-pair (8 bit D1) or as an eleven-pair (10 bit D1) ECL cable configuration; the 8 bit D1 format is used for this demo board.

Upon input to the demo board, these signals are converted to TTL levels consisting of 8 data bits and one 27MHz clock stream.

The luminance (Y) and chrominance (Cb, Cr) are multiplexed onto the 8 bit data path in the order: Cb, Y, Cr, Y, etc. (see Figure 1). For each two clock cycles, one luminance and one of the two chrominance signals are transmitted. This is the same luminance and chrominance data bandwidth used by the Philips chip set, with the exception that it is multiplexed.

De-multiplexing the luma and chroma data produces 8 bit data paths each for luminance and chrominance, clocked at a 13.5 MHz clock rate. There is now one luma byte delivered for each 13.5MHz clock and one pair of chroma axis bytes for every two clock intervals; this is exactly the data format required by the digital chip set.

The D1 format also inserts markers into the data path that define the beginning and end of active video. These markers consist of 4 hex bytes: FF, 00, 00, XY. The series, FF 00 00 is used to initiate the start or end of active video and to latch the XY byte information.

The XY byte contains three bits that define the following (see Figure 2):

- End or Start of Horizontal Blanking
- End or Start of Vertical Blanking
- Field 1 or Field 2 Status.

Although horizontal and vertical sync are not included in these codes, their relation to the blanking signals is known, and they can be reconstructed.

BOARD DESCRIPTION

Reference to sheet one of the schematic shows that the demo board consists of four subsections:

- ECL translation and power regulation
- D1 to 422 demultiplexing
- Digital YUV to analog composite encoding
- Digital YUV to analog YUV and analog RGB conversion.

ECL Translation

Sheet two shows the D1 signal input at connector P1 as eight pairs of data and one pair of clock lines. These lines are terminated through 470 Ω resistors to –5 VDC and are converted from differential ECL data into ground referenced TTL data (U32–U34).

Standard three terminal regulators are used to convert unregulated positive and negative 9 volt inputs to regulated positive 5 VDC (Vcc), negative 5 VDC and positive 8 VDC. Bypass caps are shown and are distributed throughout the board.

U51 is a programmable microcontroller that will initialize the appropriate devices upon power up by use of the Philips I^{2}C interface. I^{2}C programming can also be performed over the I^{2}C bus via external connectors (JP4 and JP5 shown on sheet 5).

D1 to 422 Demux

The 8 data lines enter buffer U31 on sheet 3 and are clocked sequentially through U12, U13, and U14 at a 27 MHz clock rate. If a byte value of FF is detected at U26 at the output of U14, and if data byte values of 00 are detected by U5A and U5B at the outputs of U13 and U12, the coincidence of these signals latches the contents of bits TL6, TL5, and TL4 into U15. These signals are reclocked at a 13.5 MHz rate and are output by U17 and U6B as HREF (horizontal blanking), vertical blanking, and field ID.

The 27 MHz clock is divided in half by U27A and buffered by U7. Counters U8 and U9 are loaded to a preset by HREF and clocked by the 27 MHz clock to produce a horizontal sync reset pulse at the output of U22A.

The 8 bits of multiplexed YUV data are duplicated into two identical buses. One bus (to be demuxed as Y) is connected to the A1-D1 inputs of U20 and U18, the other bus (to be demuxed as UV) is connected to the A2-D2 inputs of U19 and U21. The outputs of all four of the demux devices are returned to the alternate inputs of the same device, QA-QD of U20 and U18 are returned to the corresponding A2-D2 inputs, and QA-QD of U19 and U21 are returned to the corresponding A1-D1 inputs. All four devices are clocked at the same 27 MHz rate, and the WS (write strobe) is supplied with a common 13 MHz clock. Due to the reversal of the input arrangement, the write strobe in one case will latch the Y data, and in the other case will latch the UV data. The data output from U18-U21 actually changes at a 13.5 MHz rate due to the feedback of the data and the 13.5 MHz write strobe. This data is latched and buffered by U24 for Y and U23 for UV. These two devices can also be tristated in the case it is desired to input alternative data from connector JP1. This tristate is controlled by jumper JP3.

Digital YUV to Analog Composite Encoding

The 16 bits of demuxed Y and UV are input to the data ports of the SAA7199 digital encoder. The device is supplied with a 13.5 MHz pixel clock, HREF for blanking, HS for horizontal reset, and Field ID for vertical reset. The TSG422 generator does not output interlaced vertical blanking, the generator produces vertical blanking at the beginning of line 263, as opposed to starting midway between lines 262 and 263, as is the case in analog video. The SAA7199B needs only to be reset vertically once to place it in the proper field sequence; the device will then create the proper vertical synchronization. That being the case, field ID is used to reset the device vertically for the first field, and the SAA7199 calculates and correctly produces the interlaced vertical interval between field 1 and 2.

The signal CLK_13 is used both to latch the data (via the LDV pin) and, after a delay period produced by U47A and U47B, is applied to the CLKIN and LLC pins. The delay is to ensure that latching the data and clocking it do not occur simultaneously.

The SAA7199B simultaneously outputs composite video and S-video (separate luminance and chrominance). Output filters are applied to these outputs to low pass any residual clock energy and to provide sin(X)/X correction. The output of the composite filter is buffered; this allows for driving long cable lengths without effecting the output filter characteristics.

Digital video evaluation board

U54, Q4, and Q5 strip and buffer sync from the luminance portion of the S-video output. This composite sync is used for the analog YUV and RGB that is produced by the SAA7165 and TDA4686 devices (described in the next section). The position of this sync relative to the active YUV (RGB) signals is programmable via the SAA7199B.

The SAA7199B is programmed to run in slave mode with YUV as the input format. The following chart lists the complete register settings for initializing the encoder:

SUB ADDR	DATA
SAA7199B	
00	AE
01	00
02	00
03	00
04	44
05	30
06	52
07	30
08	10
09	00
0A	00
0B	00
0C	A6
0D	00
0E	0D

These registers are programmed via the I^2C bus, either by the microcontroller or the I^2C interface connectors JP4 or JP5.

Note that the encoder has both digital (Vcc) and analog (AVcc) power connections. AVcc is produced from Vcc by the filter network comprised of L4, C64, C65, and C67.

Digital YUV to Analog YUV and RGB conversion

Sheet five indicates the data buses Y[0..7] and UV[0..7] input to U53 in parallel with the outputs of U38 and U38 tristate buffers. These buffers, in conjunction with U23 and U24 (sheet 3) and the signal D1SEL set by jumper JP3, select the input to the SAA7165 (and the SAA7199B) to be either the demuxed D1 data (JP3 shorted) or the data input from connector JP1 (JP3 open). An example of data that could be input to the demo board at JP1 is the data stream from the Philips digital decoder (SAA7151B, SAA7191B, or SAA7194(6)). The sync and clock signals from the decoder are input at connector JP2.

Connectors JP2 and JP1 are oriented such that the D1 demo board may be connected directly above the Philips DTV7199 demo board. JP2 connects to JP10 of the DTV7199 and JP1 connects to JP14 of the DTV7199. The same mechanical relation exists between the pair of connectors.

The SAA7165 also receives the 13.5 MHz clock and HREF signals to clock and blank the conversion process.

The video DAC outputs analog Y, U, and V on separate outputs. The polarity of the U and V signals is controllable in software for flexibility with all systems. The SAA7165 also provides controllable color transient improvement. The analog YUV signals are buffered by U42-U44 to provide .7 Vpp signals (full scale video) into a 75 Ω terminated load.

As with the SAA7199B, the SAA7165 has both digital (Vcc) and analog (Vcc_ANA). This separation if effected by L2, C22, and C23.

The YUV outputs are also fed to the inputs of the TDA4686 via resistor networks to provide the proper voltage range to the TDA4686. This device requires a full scale Y input of .45 Vpp, U input is 1.33 Vpp full scale, and V is 1.05 Vpp full scale.

The TDA4686 has an analog YUV to RGB matrix with software control of contrast, brightness, and saturation via the I^2C bus.

The TDA4686 requires a two-level timing signal called 'sandcastle' to initiate certain internal processes. This signal is synthesized by U40A, U45A, U46A, and U45B from vertical sync and HREF. HREF is delayed in this circuit to compensate for the pipeline delay of the video through the SAA7165.

The output of the TDA4686 are fed to a modified emitter follower circuit that ensures the proper DC blanking levels and drives 75 Ω loads. The default register setting provided by the microcontroller set RGB levels to .7 Vpp (full scale).

The default register settings are:

SUB ADDR	DATA
SAA7165*	
01	04
02	85
03	3B
TDA4686	
00	09
01	30
02	27
03	19
04	1F
05	1F
06	1F
07	1F
08	1F
09	1F
0A	3F
0B	00
0C	80
0D	1A
*There is no sub address 00 for the SAA7165.	

JP4 and JP5 are connected in parallel to allow daisy chaining of the I^2C cables to facilitate a multiple board configuration. Because the state of the I^2C bus is not necessarily known upon reset, the I^2C interface should be disconnected when resetting the board via the microcontroller.

The subaddress settings given are suggested initial values; consult the individual data sheets to manipulate the user-adjustable controls such as contrast, brightness, aperture control, color transient improvement settings, etc.

Performance tests of the SAA7199B using the Tektronix VM700A Video Measurement Test Set were made using the D1 demo Board, and results published in a document titled "SAA7199 Performance Measurements." This document is published as a separate data sheet.

Digital video evaluation board

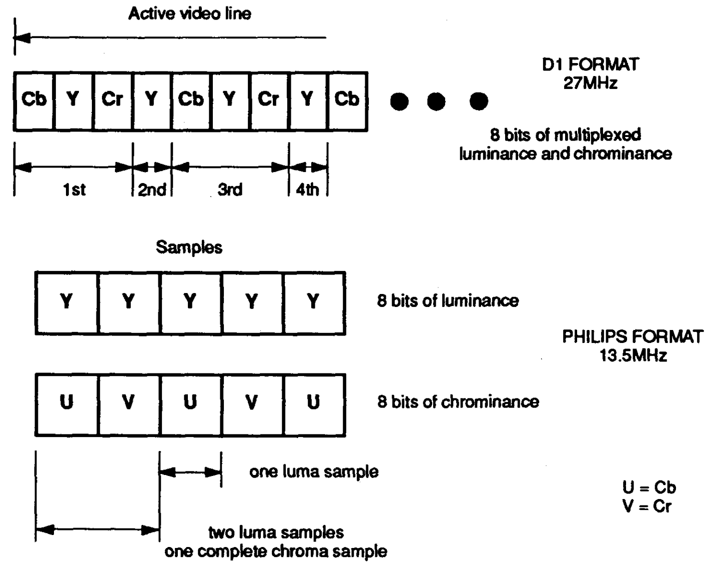


Figure 1. Data Format Comparison

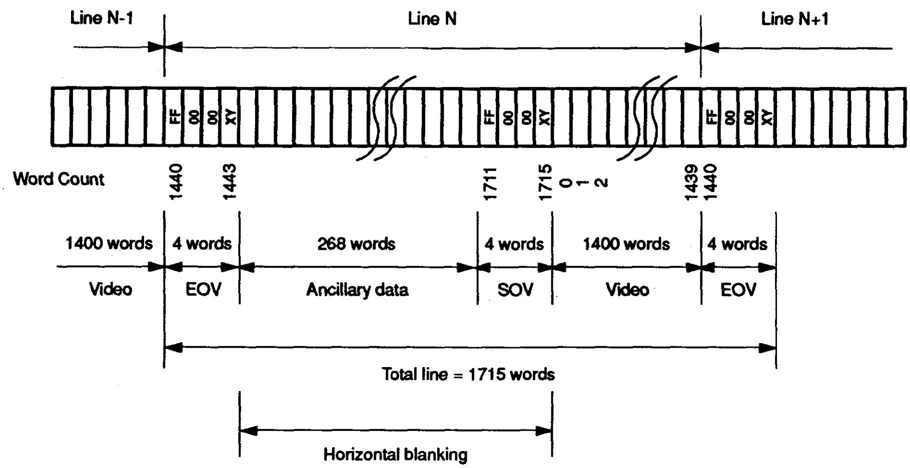
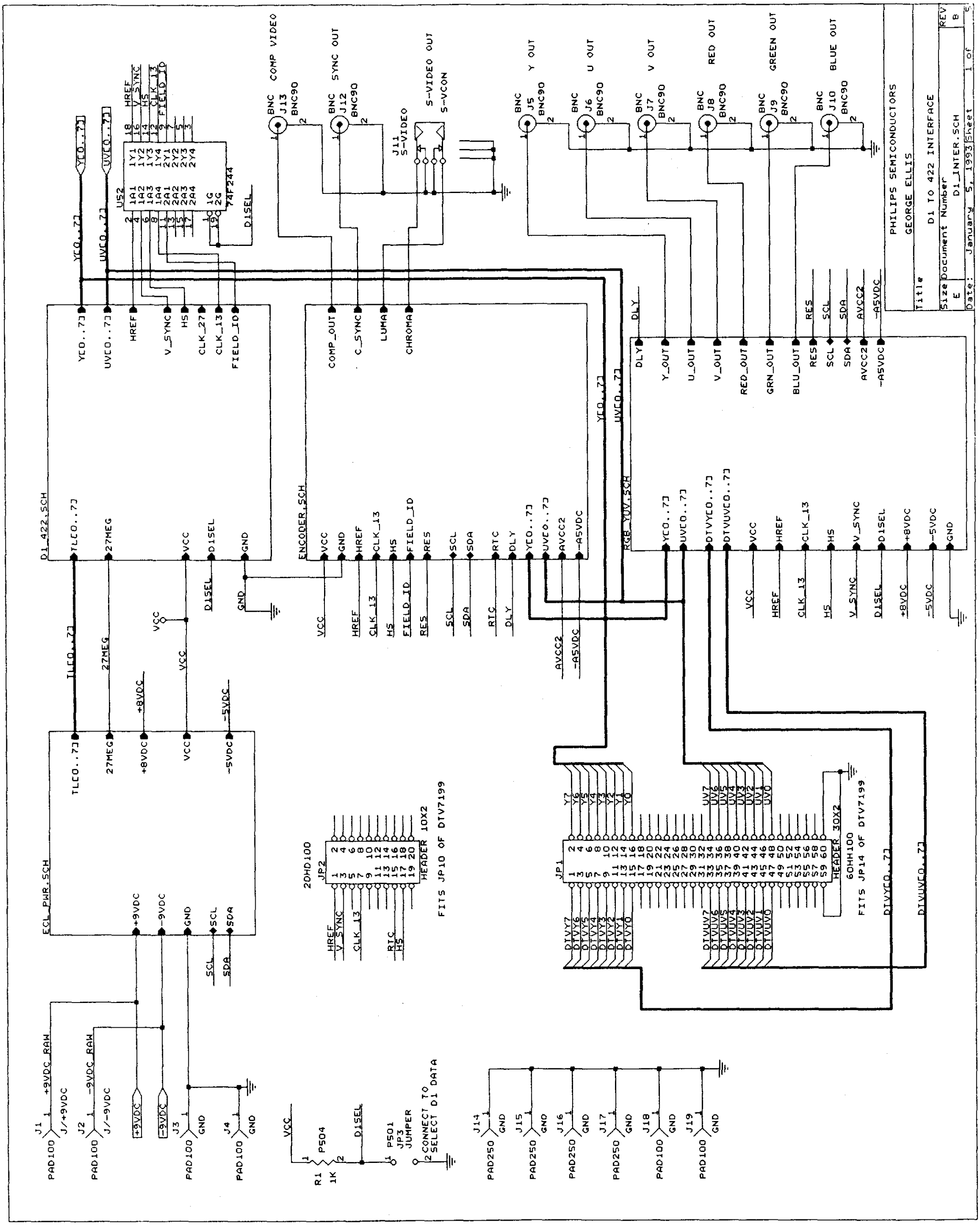
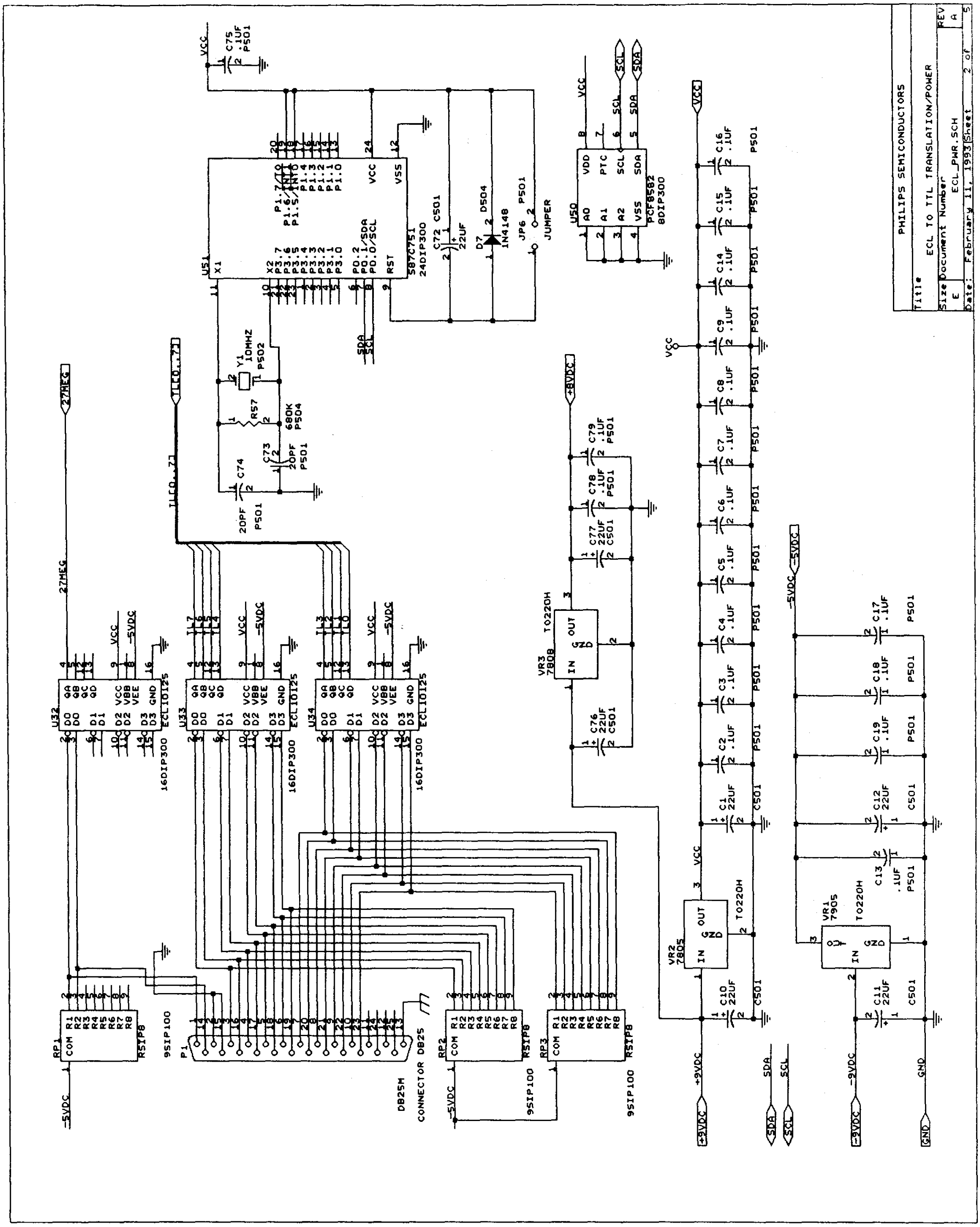


Figure 2. Active Video Markers for D1 Video

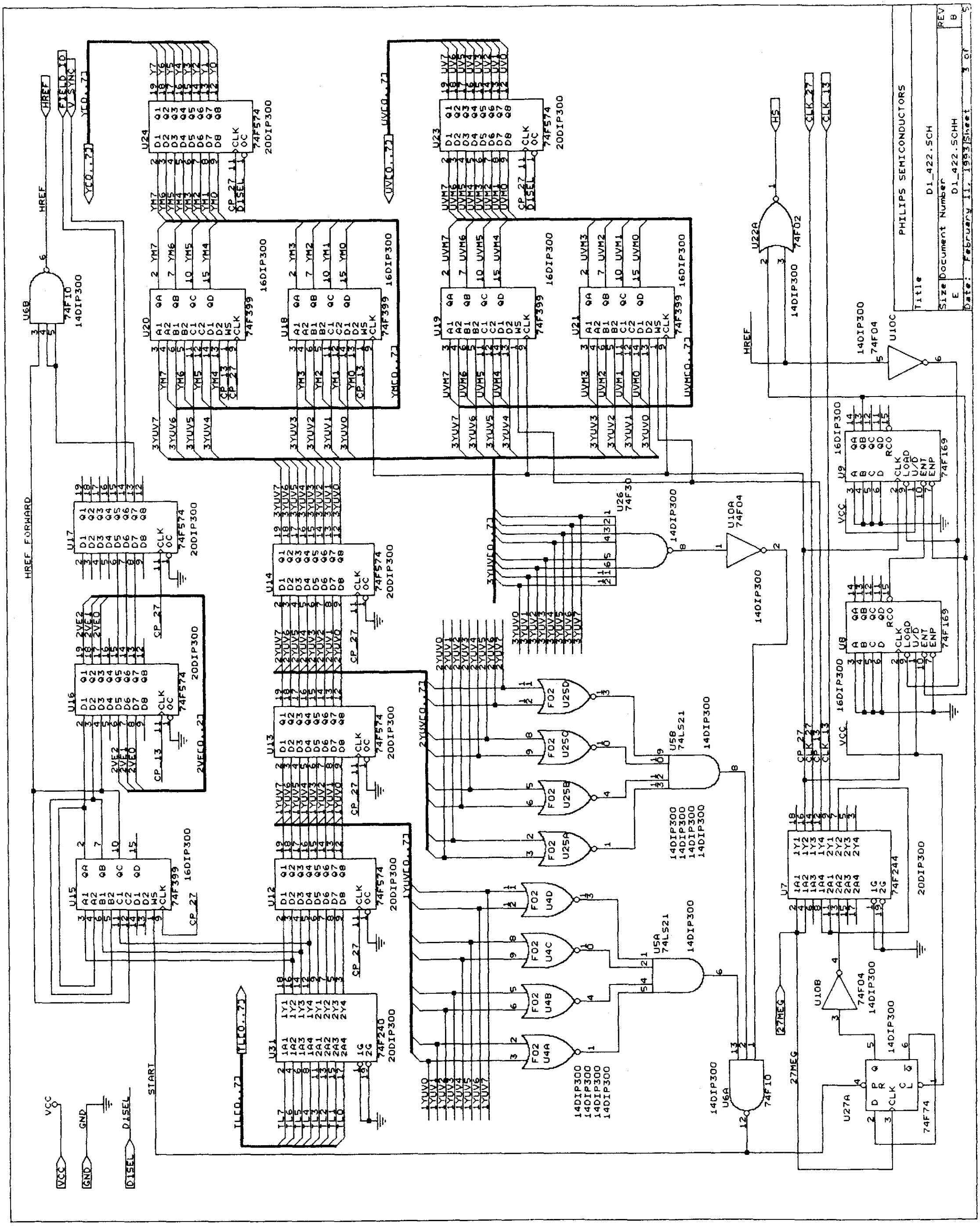
Digital video evaluation board



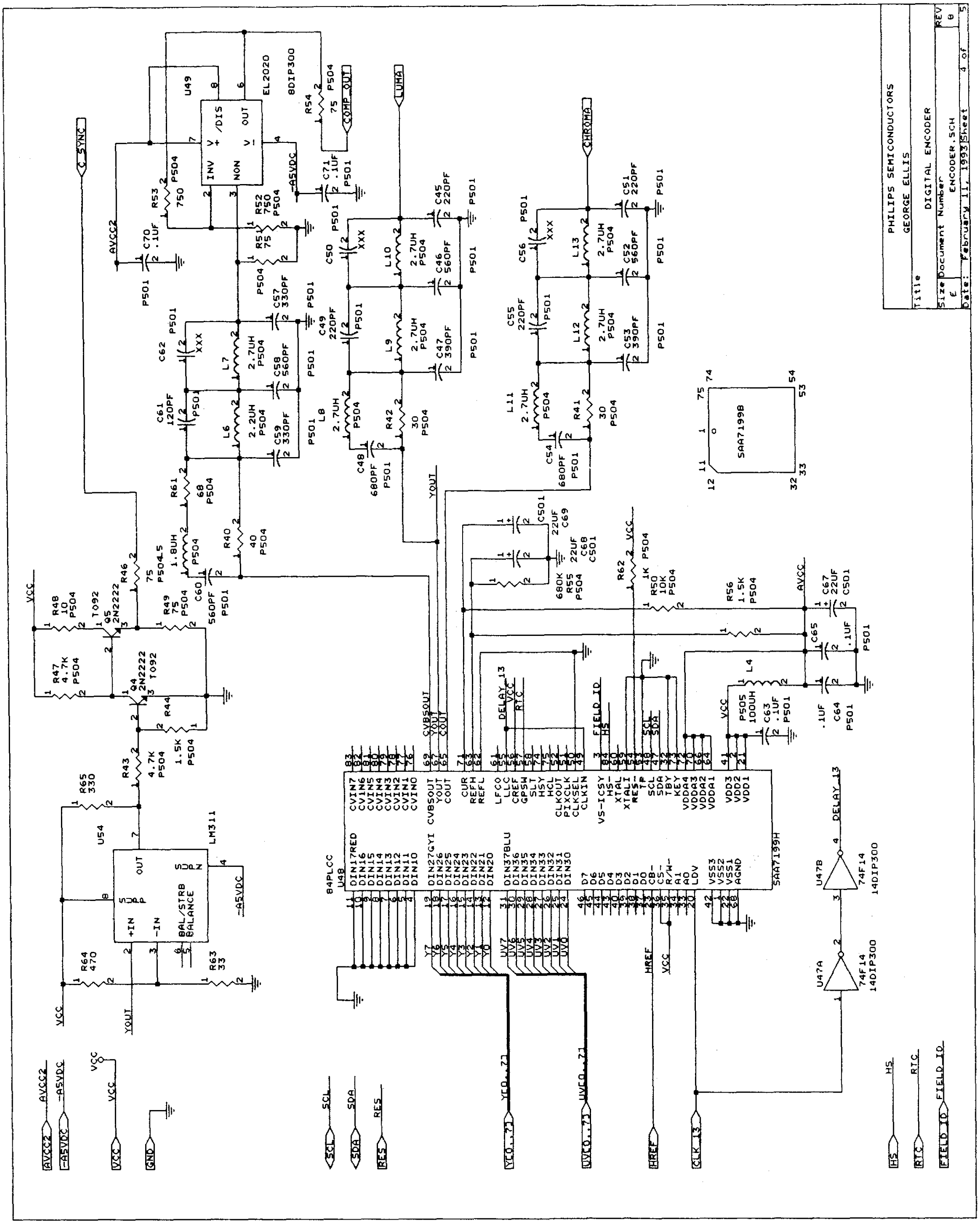
Digital video evaluation board



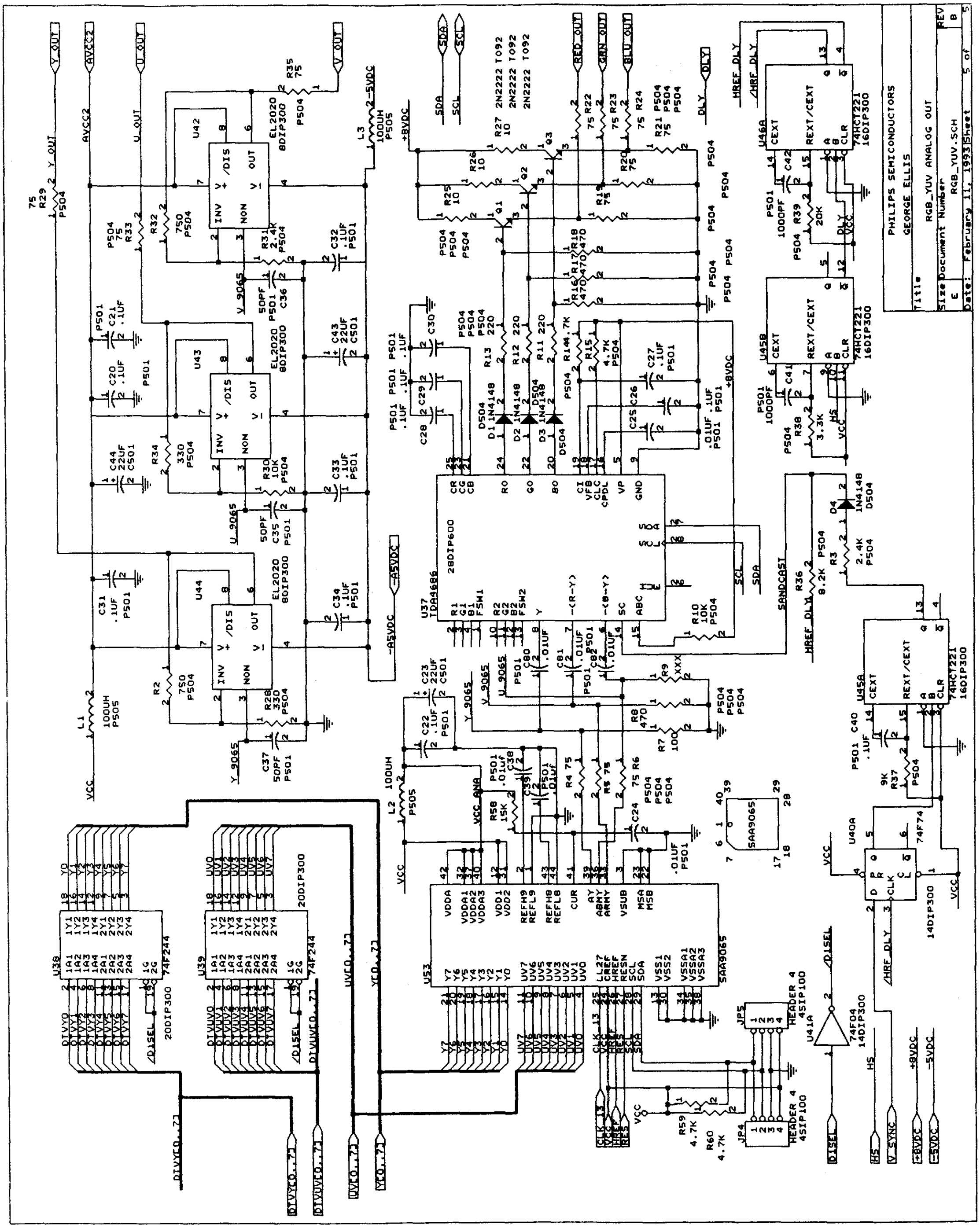
Digital video evaluation board



Digital video evaluation board



Digital video evaluation board



CVBS output filter for SAA7199B encoder

Author: George Ellis

OVERVIEW

Peak performance of the SAA7199B can be obtained by the use of an output filter connected between the CVBS output of the device and the output connector. This filter provides sin(x)/x equalization for the CVBS (composite video) signal.

THEORY

Sin(x)/x attenuation occurs with all DACs (digital-to-analog convertors) due to the sampling clock. This attenuation increases as the output frequency of the DAC increases and reaches total attenuation when the DAC output is equal to the sample frequency (see Figure 1.)

Another result of clocking the DAC is the creation of energy which is centered at multiples of the sample frequency f_s and has a bandwidth of $2(f_s–f_v)$, where f_v is the highest frequency of the output signal (see Figure 2). This non-baseband energy is referred to as 'aliasing', and if f_s is less than twice the frequency of f_v, this aliasing will extend into the baseband signal. This is not desirable because it produces visible corruption of the video signal.

The requirements of the filter, therefore, are that 1) it provides sufficient attenuation at frequencies above f_v and 2) it applies the appropriate inverse sin(x)/x boost at frequencies below f_v. Figure 3 shows an example of this filter requirement as a graph of gain versus frequency.

THE FILTER

The filter is illustrated in Figure 4. It is a modified low pass filter with components added to provide sin(x)/x equalization (C1, L1, and R2). Sin(x)/x attenuation is calculated by the formula

$$A(x) = \frac{sin(\pi f_x/f_s)}{\pi f_x/f_s}$$

where f_x is the frequency in question. The number $\pi f_x/f_s$ is in radians, before calculating the sin. This number should be converted to degrees (there are 57.29 degrees per one radian).

In this case, attenuation was calculated for 3.58 MHz and 4.43 MHz, the color subcarrier frequencies for NTSC and Pal, respectively.

A(3.58 MHz) = .881

A(4.43 MHz) = .834

The attenuation in decibels can be calculated from the formula:

dB = 20log(A(x))

This gives a value of –1.04 dB down for 3.58 MHz and a value of –1.57 dB down for 4.433 MHz. The filter, therefore, must provide a boost of 1.04 dB at 3.58 MHz, and of 1.57 dB at 4.433 MHz.

Figure 5 is a plot of the filter ranging from 1 MHz to 100 MHz and from 0 dB to –50 dB down, and Figure 6 shows the same frequency spread and a gain range from 0 dB to –20 dB to better illustrate the sin(x)/x correction.

Starting with a gain value of –6 dB (as would be expected for the 50% DC signal drop across the termination resistor), it can be seen that at a frequency of 3.58 MHz the gain is –5 dB, and at 4.43 MHz the gain is –4.5 dB, a boost of 1 dB and 1.5 dB, respectively, as required (see Figure 6). Figure 5 shows an attenuation of –22 dB at 8 MHz, –40 dB at 9 MHz, and a value of –43 dB at 13 MHz (the clock frequency).

Many different filters can be made to meet the sin(x)/x requirement. This filter was chosen to provide augmentation up through the Pal subcarrier region. A filter with a cutoff at lower frequencies could be designed for use with NTSC only. This filter was also chosen for economic reasons, and more expensive filters could certainly be designed with improved performance. This filter was found to have a good performance to cost ratio and can be made from standard component values and 5% tolerance parts.

If large capacitive loads are expected to be encountered, it may be desirable to buffer the output filter with a high speed op amp. If this is the case, the filter should be terminated with a 75 Ω load at the input of the op amp. The op amp should be operated in non-inverting mode with a gain of two.

CVBS output filter for SAA7199B encoder

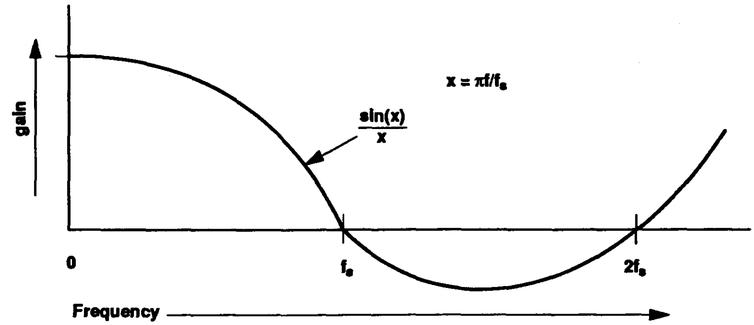


Figure 1. Attenuation

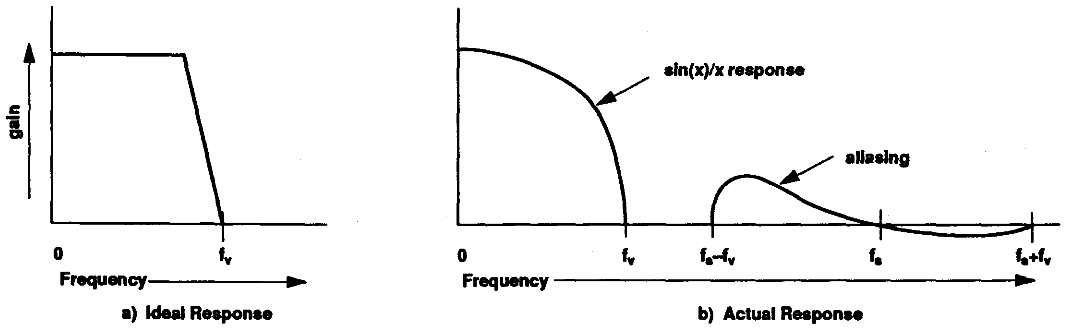


Figure 2. Response

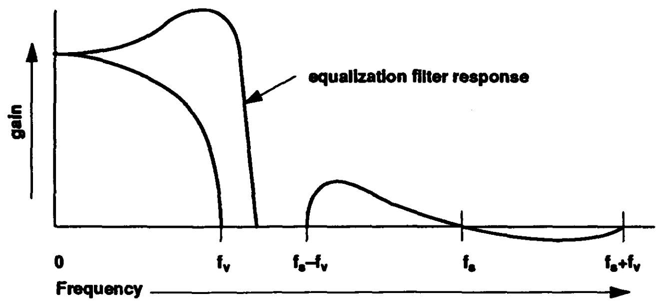


Figure 3. Example of Filter Requirement

CVBS output filter for SAA7199B encoder

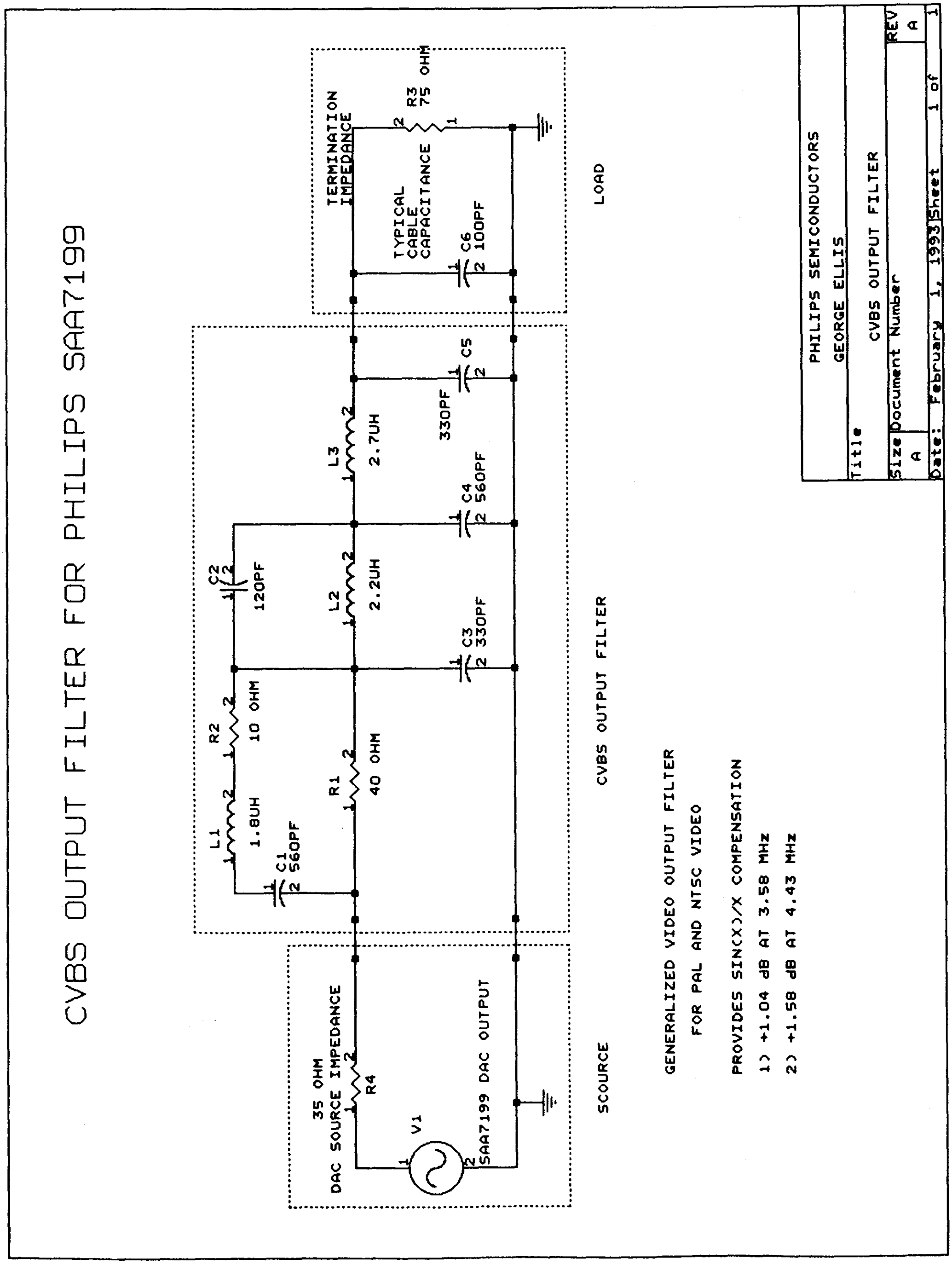


Figure 4. CVBS Output Filter

CVBS output filter for SAA7199B encoder

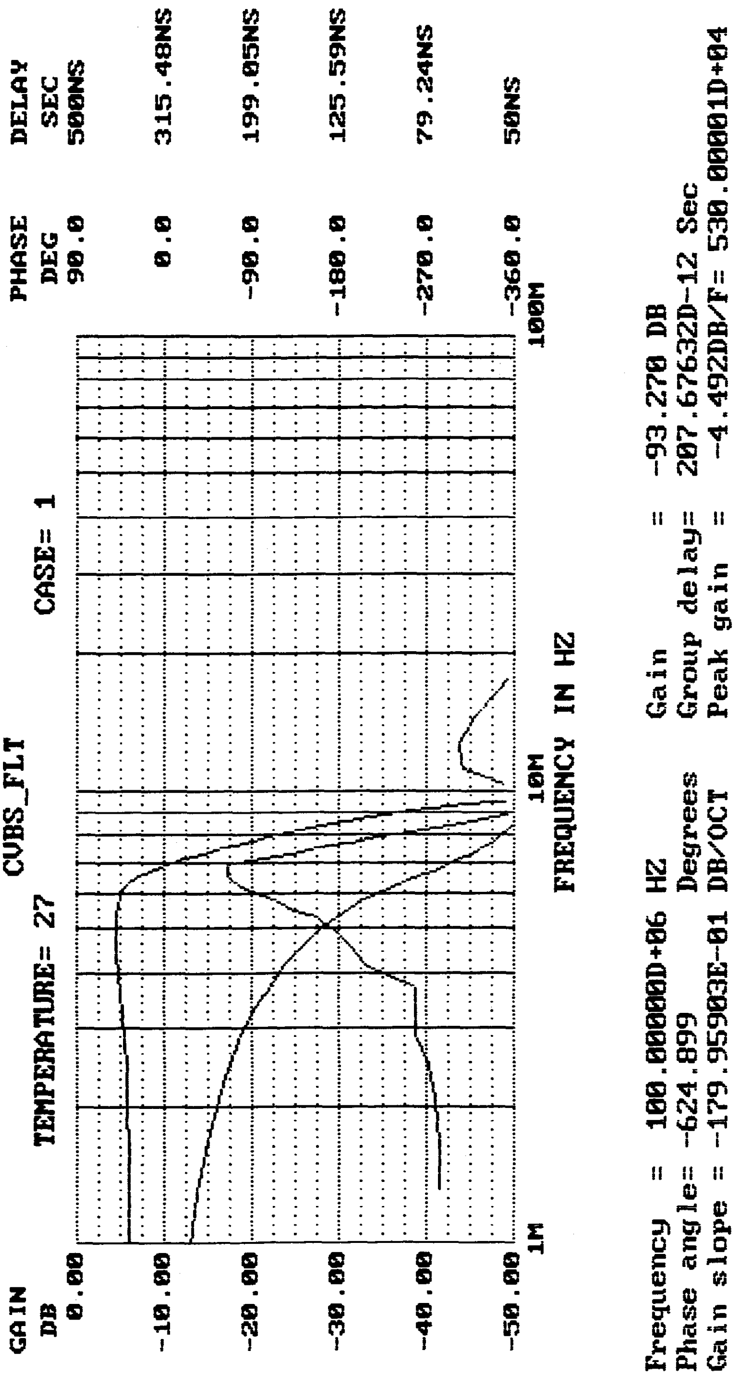


Figure 5. Plot of the Filter Ranging from 1MHz to 100MHz and from 0 dB to –50 dB

CVBS output filter for SAA7199B encoder

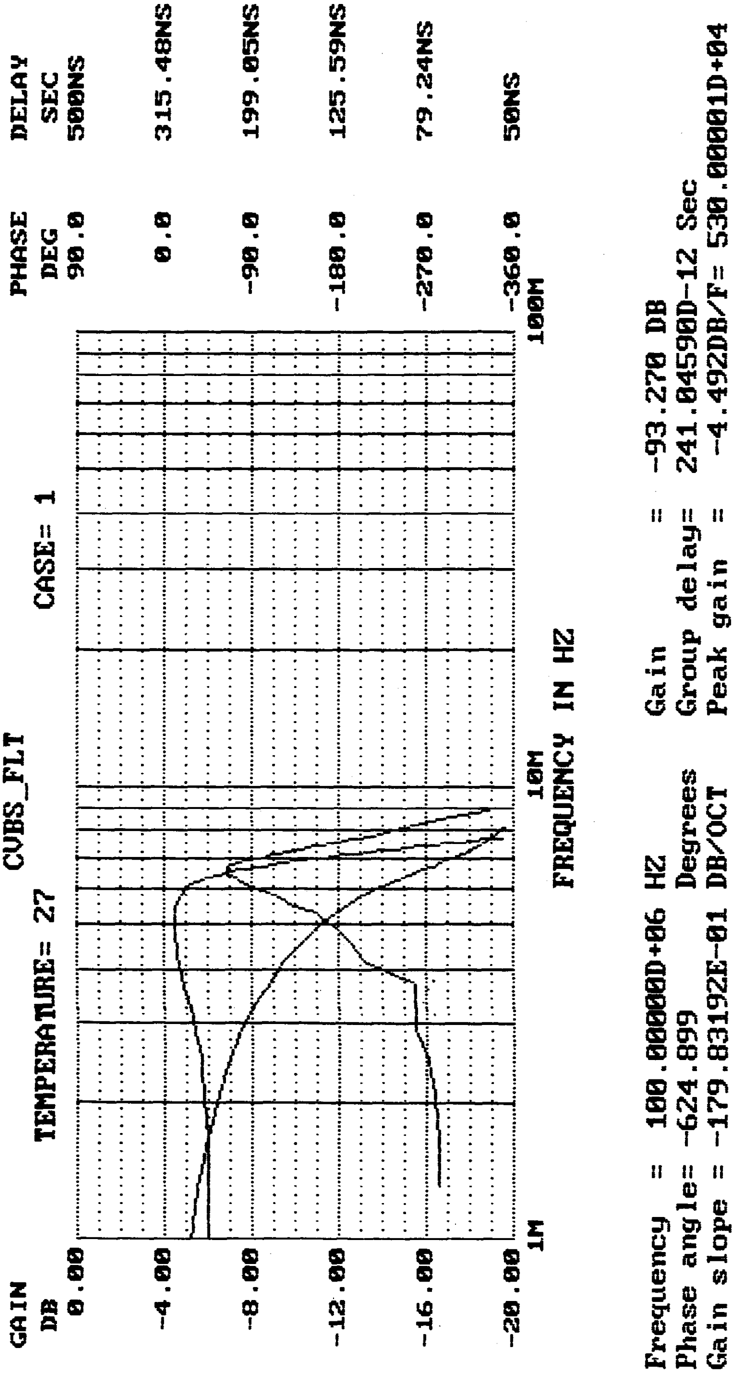


Figure 6. Plot of the Filter Ranging from 1MHz to 100MHz and from 0 dB to –20 dB

SAA1101 sync generator application

LOCK TO SUBCARRIER

The SAA1101 can be configured to run in a mode in which the output pulses are locked to a subcarrier signal that is either internally generated (as shown here), or can be applied as an AC coupled, low level input to pin 1.

The internal clock oscillator is used here with the frequency selected to be 2.517482MHz (CS0 and CS1 = 0). Remember that for different choices of oscillator frequency, the LC values of the tank circuit (L1 and C11) will change accordingly.

The NTSCI system is selected in this example; all outputs are active HIGH (see waveforms shown in data sheets).

LOCK TO EXTERNAL COMPOSITE SYNC

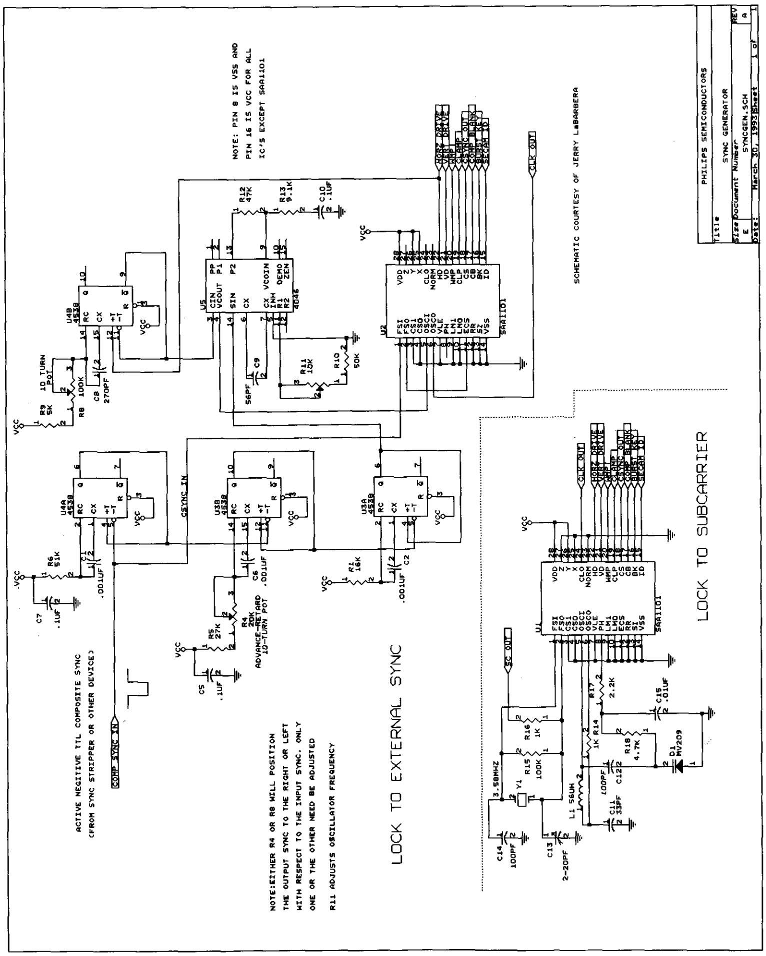
This schematic illustrates a lock to external sync application that uses an external PLL to generate a clock that is optimized for stability. Monostables are added to the reference and variable phase detector inputs to allow offsetting the sync outputs with respect to the composite sync input signal.

As above, the NTSC1 standard and 2.517482MHz clock are selected. The use of an external PLL (the HC4046) along with optimized loop filters and stable discrete components, produces a very stable clock (5 percent, or better, resistors and COG capacitors are recommended).

The lock mode selection is not critical in this application because the internal oscillator is not used; LM0 and LM1 are grounded for convenience. The subcarrier input at pin 1 is used as an inverter for the output of the sync stripper before it is fed to the ESC input (pin 11), which requires an active HIGH signal.

Either pot R4 or pot R8 will move the generated sync output relative to sync in, therefore, only one need be adjustable. Pot R11 is used to adjust the oscillator free-run frequency. R10, pot R11, and C9 must be temperature stable parts for oscillator frequency stability over temperature.

The outputs of the SAA1101 are active HIGH signals which can directly drive inverting buffers for use as conventional active LOW drivers.



I^2C-bus specification (including fast-mode)

PREFACE

This specification is an updated version including the following latest modifications:

- Programming of a slave address by software has been omitted. The realization of this feature is rather complicated and has not been used.
- The 'low-speed mode' has been omitted. This mode is, in fact, a subset of the total I^2C-bus specification and need not be specified explicitly.
- The 'fast-mode' is added. This allows a fourfold increase of bit rate up to 400 kbit/s. Fast-mode devices are downwards compatible i.e. they can be used in a 0 to 100 kbit/s I^2C-bus system.
- 10-bit addressing is added. This allows 1024 additional slave addresses.
- Slope control and input filtering for fast-mode devices is specified to improve the EMC behaviour.

NOTE

Neither the 100 kbit/s I^2C-bus system nor the 100 kbit/s devices have been changed.

I^2C-bus specification (including fast-mode)

1.0 INTRODUCTION

For 8-bit applications, such as those requiring single-chip microcontrollers, certain design criteria can be established:

- A complete system usually consists of at least one microcontroller and other peripheral devices such as memories and I/O expanders.
- The cost of connecting the various devices within the system must be minimized.
- Such a system usually performs a control function and doesn't require high-speed data transfer.
- Overall efficiency depends on the devices chosen and the interconnecting bus structure.

In order to produce a system to satisfy these criteria, a serial bus structure is needed. Although serial buses don't have the throughput capability of parallel buses, they do require less wiring and fewer connecting pins. However, a bus is not merely an interconnecting wire, it embodies all the formats and procedures for communication within the system.

Devices communicating with each other on a serial bus must have some form of protocol which avoids all possibilities of confusion, data loss and blockage of information. Fast devices must be able to communicate with slow devices. The system must not be dependent on the devices connected to it, otherwise modifications or improvements would be impossible. A procedure has also to be devised to decide which device will be in control of the bus and when. And, if different devices with different clock speeds are connected to the bus, the bus clock source must be defined. All these criteria are involved in the specification of the I^2C-bus.

2.0 THE I^2C-BUS CONCEPT

Any IC fabrication process (NMOS, CMOS, bipolar) can be supported by the I^2C-bus. Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognised by a unique address - whether it's a microcontroller, LCD driver, memory or keyboard interface - and can operate as either a transmitter or receiver, depending on the function of the device. Obviously an LCD driver is only a receiver, whereas a memory can both receive and transmit data. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers (see Table 1). A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The I^2C-bus is a multi-master bus. This means that more than one device capable of controlling the bus can be connected to it. As masters are usually micro-controllers, let's consider the case of a data transfer between two microcontrollers connected to the I^2C-bus (Fig.1). This highlights the master-slave and receiver-transmitter relationships to be found on the I^2C-bus. It should be noted that these relationships are

Table 1 Definition of I^2C-bus terminology

Term	Description
Transmitter	The device which sends the data to the bus
Receiver	The device which receives the data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
Synchronization	Procedure to synchronize the clock signals of two or more devices

I²C-bus specification (including fast-mode)

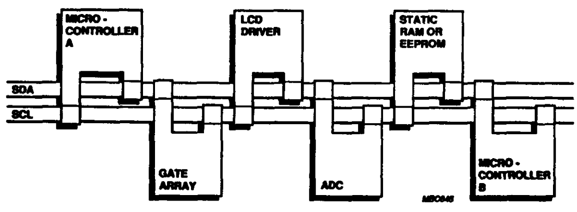


Fig.1 Example of an I²C-bus configuration

not permanent, but only depend on the direction of data transfer at that time. The transfer of data would proceed as follows:

1) Suppose microcontroller A wants to send information to microcontroller B:

- microcontroller A (master), addresses microcontroller B (slave)
- microcontroller A (master-transmitter), sends data to microcontroller B (slave-receiver)
- microcontroller A terminates the transfer.

2) If microcontroller A wants to receive information from microcontroller B:

- microcontroller A (master) addresses microcontroller B (slave)
- microcontroller A (master-receiver) receives data from microcontroller B (slave-transmitter)
- microcontroller A terminates the transfer.

Even in this case, the master (microcontroller A) generates the timing and terminates the transfer.

The possibility of connecting more than one microcontroller to the I²C-bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event - an arbitration procedure has been developed. This procedure relies on the wired-AND connection of all I²C interfaces to the I²C-bus.

If two or more masters try to put information onto the bus, the first to produce a 'one' when the other produces a 'zero' will lose the arbitration. The clock signals during arbitration are a synchronised combination of the clocks generated by the masters using the wired-AND connection to the SCL line (for more detailed information concerning arbitration see section 6.0).

Generation of clock signals on the I²C-bus is always the responsibility of master devices; each master generates its own clock signals when transferring data on the bus. Bus clock signals from a master can only be altered when they are stretched by a slow-slave device holding-down the clock line, or by another master when arbitration occurs.

3.0 GENERAL CHARACTERISTICS

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Fig.2). When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. Data on the I²C-bus can be transferred at a rate up to 100 kbit/s in the standard-mode, or up to 400 kbit/s in the fast-mode. The number of interfaces connected to the bus is solely dependent on the limiting bus capacitance of 400 pF.

4.0 BIT TRANSFER

Due to the variety of different technology devices (CMOS, NMOS, bipolar) which can be connected to the I²C-bus, the levels of the logical '0' (LOW) and '1' (HIGH) are not fixed and depend on the associated level of V_{DD} (see Section 15.0 for

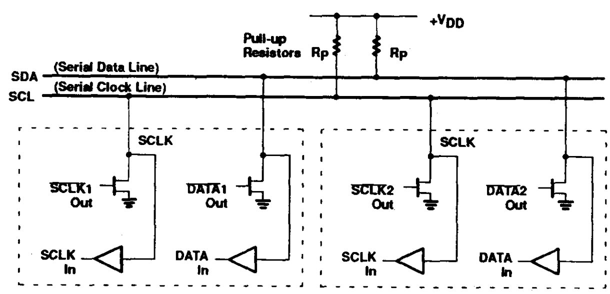


Fig.2 Connection of I²C-bus devices to the I²C-bus

I²C-bus specification (including fast-mode)

Electrical specifications). One clock pulse is generated for each data bit transferred.

4.1 Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Fig.3).

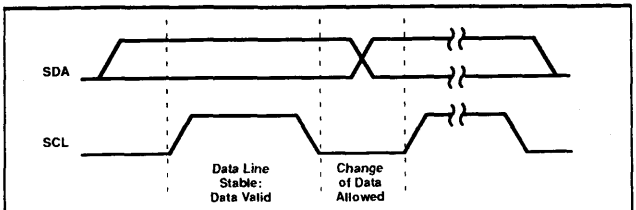


Fig.3 Bit transfer on the I²C-bus

4.2 START and STOP conditions

Within the procedure of the I²C-bus, unique situations arise which are defined as START and STOP conditions (see Fig.4).

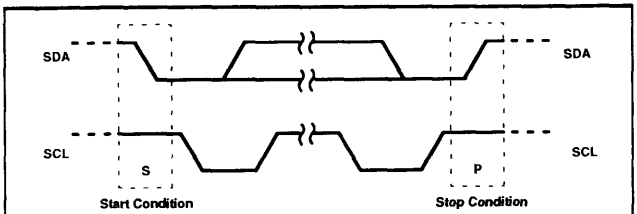


Fig.4 START and STOP conditions

A HIGH to LOW transition of the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition of the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. This bus free situation will be specified later (in Section 15.0).

Detection of START and STOP conditions by devices connected to the bus is easy if they incorporate the necessary interfacing hardware. However, microcontrollers with no such interface have to sample the SDA line at least twice per clock period in order to sense the transition.

5.0 TRANSFERRING DATA

5.1 Byte format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (Fig.5). If a receiver can't receive another complete byte of data until it has performed some other function, for example, servicing an internal interrupt, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer then continues when the receiver is ready for another byte of data and releases clock line SCL.

In some cases, it's permitted to use a different format from the I²C-bus format (for CBUS compatible devices for example). A message which starts with such an address can be terminated by generation of a STOP condition, even during the transmission of a byte. In this case, no acknowledge is generated (see section 8.1.3).

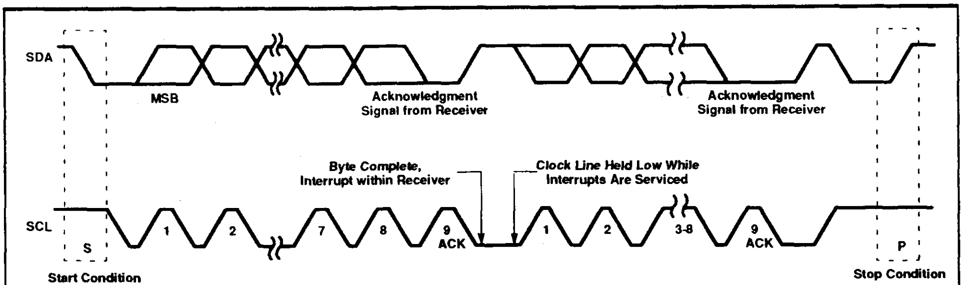


Fig.5 Data transfer on the I²C-bus

determined by the one with the shortest clock HIGH period.

6.2 Arbitration

A master may start a transfer only if the bus is free. Two or more masters may generate a START condition within the minimum hold time ($t_{HD;STA}$) of the START condition which results in a defined START condition to the bus.

Arbitration takes place on the SDA line, while the SCL line is at the HIGH level, in such a way that the master which transmits a HIGH level, while another master is transmitting a LOW level will switch off its DATA output stage because the level on the bus doesn't correspond to its own level.

Arbitration can continue for many bits. Its first stage is comparison of the address bits (addressing information is in Sections 8.0 and 12.0). If the masters are each trying to address the same device, arbitration continues with comparison of the data. Because address and data information on the I²C-bus is used for arbitration, no information is lost during this process.

A master which loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration.

If a master also incorporates a slave function and it loses arbitration during the addressing stage, it's possible that the winning master is trying to address it. The losing master must therefore switch over immediately to its slave-receiver mode.

Figure 8 shows the arbitration procedure for two masters. Of course, more may be involved (depending on how many masters are connected to the bus). The moment there is a difference between the internal data level of the master generating DATA 1 and the actual level on the SDA line, its data output is switched off, which means that a HIGH output level is then connected to the bus. This will not affect the data transfer initiated by the winning master. Since control of the I²C-bus is decided solely on the address and data sent by competing masters, there is no central master, nor any order of priority on the bus.

Special attention must be paid if, during a serial transfer, the arbitration procedure is still in progress at the moment when a repeated START condition or a STOP condition is transmitted to the I²C-bus. If it's possible for such a situation to occur, the masters involved must send this repeated START condition or STOP condition at the same position in the format frame. In other words, arbitration isn't allowed between:

- A repeated START condition and a data bit
- A STOP condition and a data bit
- A repeated START condition and a STOP condition.

6.3 Use of the clock synchronising mechanism as a handshake

In addition to being used during the arbitration procedure, the clock synchronization mechanism can be used to enable receivers to cope with fast data transfers, on either a byte level or a bit level.

On the byte level, a device may be able to receive bytes of data at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slaves can then hold the SCL line LOW after reception and acknowledgement of a byte to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure.

On the bit level, a device such as a microcontroller without, or with only a limited hardware I²C interface on-chip can slow down the bus clock by extending each clock LOW period. In this way, the speed of any master is adapted to the internal operating rate of this device.

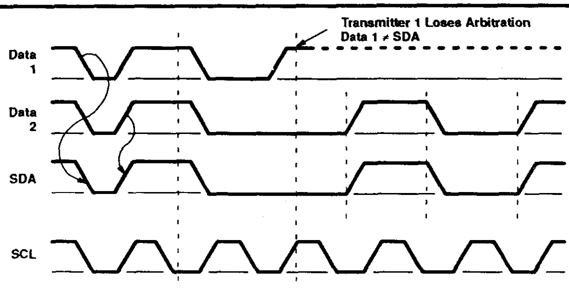


Fig.8 Arbitration procedure of two masters

I²C-bus specification (including fast-mode)

7.0 FORMATS WITH 7-BIT ADDRESSES

Data transfers follow the format shown in Fig.9. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/$\overline{W}$) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

Possible data transfer formats are:

- Master-transmitter transmits to slave-receiver. The transfer direction is not changed (Fig.10).

- Master reads slave immediately after first byte (Fig.11). At the moment of the first acknowledge, the master-transmitter becomes a master-receiver and the slave-receiver becomes a slave-transmitter. This acknowledge is still generated by the slave. The STOP condition is generated by the master.

- Combined format (Fig.12). During a change of direction within a transfer, the START condition and the slave address are both repeated, but with the R/$\overline{W}$ bit reversed.

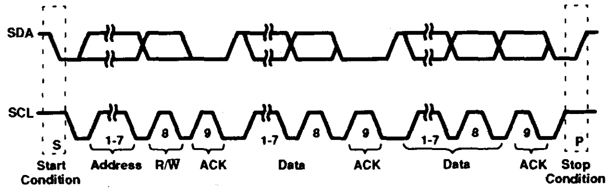


Fig.9 A complete data transfer

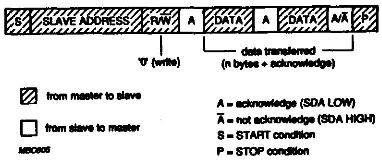


Fig.10 A master-transmitter addresses a slave-receiver with a 7-bit address. The transfer direction is not changed

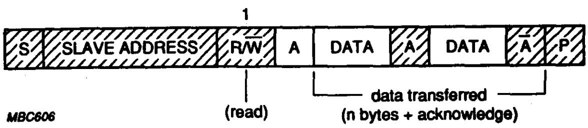


Fig.11 A master reads a slave immediately after the first byte

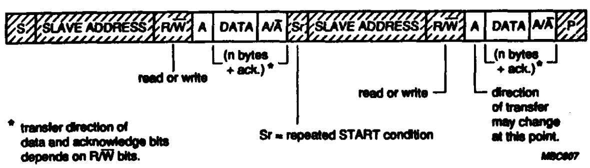


Fig.12 Combined format

NOTES:

1) Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the START condition and slave address is repeated, data can be transferred.
2) All decisions on auto-increment or decrement of previously accessed memory locations etc. are taken by the designer of the device.
3) Each byte is followed by an acknowledgement bit as indicated by the A or $\overline{A}$ blocks in the sequence.
4) I²C-bus compatible devices must reset their bus logic on receipt of a START or repeated START condition such that they all anticipate the sending of a slave address.

I²C-bus specification (including fast-mode)

8.0 7-BIT ADDRESSING (see section 13 for 10-bit addressing)

The addressing procedure for the I²C-bus is such that the first byte after the START condition usually determines which slave will be selected by the master. The exception is the 'general call' address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge. However, devices can be made to ignore this address. The second byte of the general call address then defines the action to be taken. This procedure is explained in more detail in Section 8.1.1.

8.1 Definition of bits in the first byte

The first seven bits of the first byte make up the slave address (Fig.13). The eighth bit is the LSB (least significant bit). It determines the direction of the message. A 'zero' in the least significant position of the first byte means that the master will write information to a selected slave. A 'one' in this position means that the master will read information from the slave.

When an address is sent, each device in a system compares the first 7 bits after the START condition with its address. If they match, the device considers itself addressed by the master as a slave-receiver or slave-transmitter, depending on the R/$\overline{W}$ bit.

A slave address can be made-up of a fixed and a programmable part. Since it's likely that there will be several identical devices in a system, the programmable part of the slave address enables the maximum possible number of such devices to be connected to the I²C-bus. The number of programmable address bits of a device depends on the number of pins available. For example, if a device has 4 fixed and 3 programmable address bits, a total of 8 identical devices can be connected to the same bus.

The I²C-bus committee coordinates allocation of I²C addresses. Further information can be obtained fom the Philips representatives listed on the back cover. Two groups of eight addresses (0000XXX and 1111XXX) are reserved for the purposes shown in Table 2. The bit combination 11110XX of the slave address is reserved for 10-bit addressing (see Section 13.0).

Table 2 Definition of bits in the first byte

Slave address	R/$\overline{W}$ bit	Description
0000 000	0	General call address
0000 000	1	START byte
0000 001	X	CBUS address
0000 010	X	Address reserved for different bus format
0000 011	X	
0000 1XX	X	Reserved for future purposes
1111 1XX	X	
1111 0XX	X	10-bit slave addressing

NOTES:

1) No device is allowed to acknowledge at the reception of the START byte.
2) The CBUS address has been reserved to enable the inter-mixing of CBUS compatible and I²C-bus compatible devices in the same system. I²C-bus compatible devices are not allowed to respond on reception of this address.
3) The address reserved for a different bus format is included to enable I²C and other protocols to be mixed. Only I²C-bus compatible devices that can work with such formats and protocols are allowed to respond to this address.

Fig.13 The first byte after the START procedure

I^2C-bus specification (including fast-mode)

8.1.1 General call address

The general call address should be used to address every device connected to the I^2C-bus. However, if a device doesn't need any of the data supplied within the general call structure, it can ignore this address by not acknowledging. If a device does require data from a general call address, it will acknowledge this address and behave as a slave-receiver. The second and following bytes will be acknowledged by every slave-receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not acknowledging. The meaning of the general call address is always specified in the second byte (Fig.14).

There are two cases to consider:

- When the least significant bit B is a 'zero'.
- When the least significant bit B is a 'one'.

When B is a 'zero'; the second byte has the following definition:

- 00000110 (H'06'). Reset and write programmable part of slave address by hardware. On receiving this 2-byte sequence, all devices designed to respond to the general call address will reset and take in the programmable part of their address. Precautions have to be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus
- 00000100 (H'04'). Write programmable part of slave address by hardware. All devices which define the programmable part of their address by hardware (and which respond to the general call address) will latch this programmable part at the reception of this two byte sequence. The device will not reset.
- 00000000 (H'00'). This code is not allowed to be used as the second byte.

Sequences of programming procedure are published in the appropriate device data sheets.

The remaining codes have not been fixed and devices must ignore them.

When B is a 'one'; the 2-byte sequence is a 'hardware general call'. This means that the sequence is transmitted by a hardware master device, such as a keyboard scanner, which cannot be programmed to transmit a desired slave address. Since a hardware master doesn't know in advance to which device the message has to be transferred, it can only generate this hardware general call and its own address - identifying itself to the system (Fig.15).

The seven bits remaining in the second byte contain the address of the hardware master. This address is recognised by an intelligent device, such as a microcontroller, connected to the bus which will then direct the information from the hardware master. If the hardware master can also act as a slave, the slave address is identical to the master address.

In some systems, an alternative could be that the hardware master

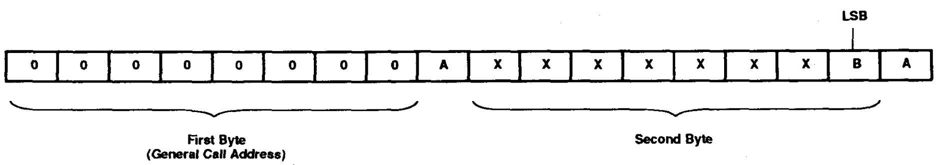


Fig.14 General call address format

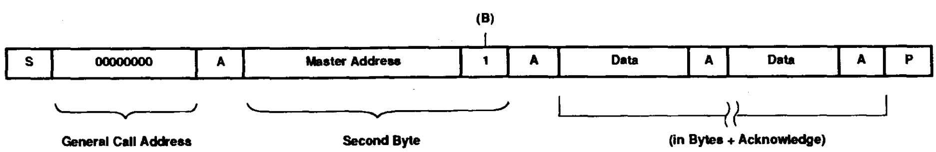


Fig.15 Data transfer from a hardware master-transmitter

I²C-bus specification (including fast-mode)

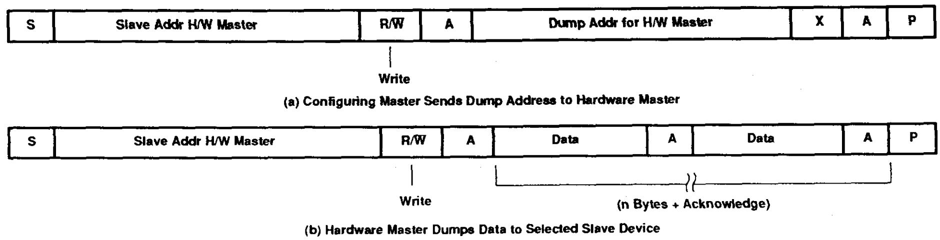


Fig.16 Data transfer by a hardware-transmitter capable of dumping data directly to slave devices (a) Configuring master sends dump address to hardware master (b) Hardware master dumps data to selected slave

transmitter is set in the slave-receiver mode after the system reset. In this way, a system configuring master can tell the hardware master-transmitter (which is now in slave-receiver mode) to which address data must be sent (Fig.16). After this programming procedure, the hardware master remains in the master-transmitter mode.

8.1.2 START byte

Microcontrollers can be connected to the I²C-bus in two ways. A microcontroller with an on-chip hardware I²C-bus interface can be programmed to be only interrupted by requests from the bus. When the device doesn't have such an interface, it must constantly monitor the bus via software. Obviously, the more times the microcontroller monitors, or polls, the bus the less time it can spend carrying out its intended function. There is therefore a speed difference between fast hardware devices and a relatively slow microcontroller which relies on software polling.

In this case, data transfer can be preceded by a start procedure which is much longer than normal (Fig.17). The start procedure consists of:

- A START condition (S)
- A START byte (00000001)
- An acknowledge clock pulse (ACK)
- A repeated START condition (Sr).

After the START condition S has been transmitted by a master which requires bus access, the START byte (00000001) is transmitted. Another microcontroller can therefore sample the SDA line at a low sampling rate until one of the seven zeros in the START byte is detected. After detection of this LOW level on the SDA line, the microcontroller can switch to a higher sampling rate to find the repeated START condition Sr which is then used for synchronization.

A hardware receiver will reset on receipt of the repeated START condition Sr and will therefore ignore the START byte.

An acknowledge-related clock pulse is generated after the START byte. This is present only to conform with the byte handling format used on the bus. No device is allowed to acknowledge the START byte.

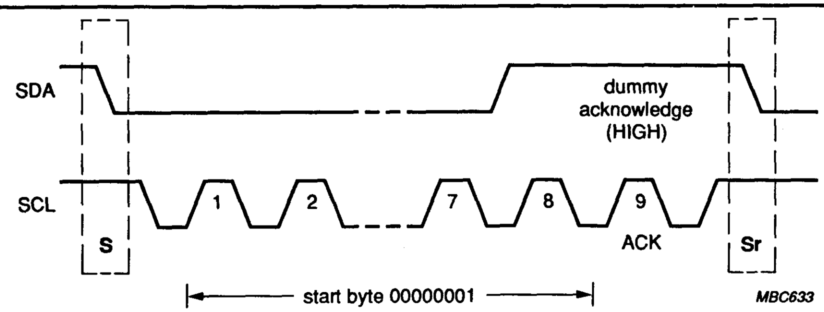


Fig.17 START byte procedure

I²C-bus specification (including fast-mode)

8.1.3 CBUS compatibility

CBUS receivers can be connected to the I²C-bus. However, a third line called DLEN must then be connected and the acknowledge bit omitted. Normally, I²C transmissions are sequences of 8-bit bytes; CBUS compatible devices have different formats.

In a mixed bus structure, I²C-bus devices must not respond to the CBUS message. For this reason, a special CBUS address (0000001X) to which no I²C-bus compatible device will respond, has been reserved. After transmission of the CBUS address, the DLEN line can be made active and a CBUS-format transmission (Fig.18) sent. After the STOP condition, all devices are again ready to accept data.

Master-transmitters can send CBUS formats after sending the CBUS address. The transmission is ended by a STOP condition, recognised by all devices.

NOTE: If the CBUS configuration is known, and expansion with CBUS compatible devices isn't foreseen, the designer is allowed to adapt the hold time to the specific requirements of the device(s) used.

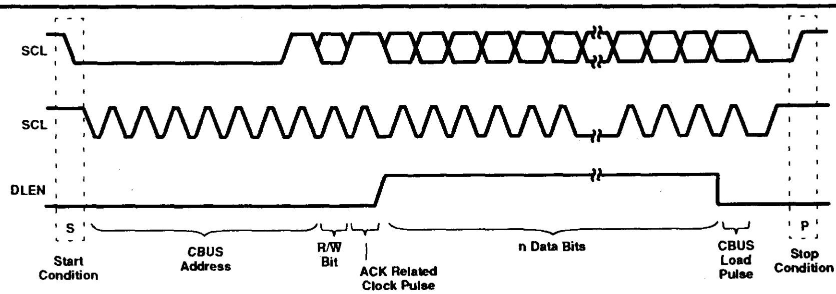


Fig.18 Data format of transmissions with CBUS transmitter/receiver

I²C-bus specification (including fast-mode)

9.0 ELECTRICAL CHARACTERISTICS FOR I²C-BUS DEVICES

The electrical specifications for the I/Os of I²C-bus devices and the characteristics of the bus lines connected to them are given in Tables 3 and 4 in Section 15.

I²C-bus devices with fixed input levels of 1.5 V and 3 V can each have their own appropriate supply voltage. Pull-up resistors must be connected to a 5 V ± 10% supply (Fig.19). I²C-bus devices with input levels related to V_{DD} must have one common supply line to which the pull-up resistor is also connected (Fig.20).

When devices with fixed input levels are mixed with devices with input levels related to V_{DD}, the latter devices must be connected to one common supply line of 5 V ± 10% and must have pull-up resistors connected to their SDA and SCL pins as shown in Fig.21.

Input levels are defined in such a way that:

- The noise margin on the LOW level is 0.1 V_{DD}
- The noise margin on the HIGH level is 0.2 V_{DD}
- Series resistors (R_S) of e.g. 300 Ω can be used for protection against high voltage spikes on the SDA and SCL line due to flash-over of a TV picture tube, for example (Fig.22).

9.1 Maximum and minimum values of resistors R_p and R_s

In a standard-mode I²C-bus system the values of resistors R_p and R_s in Fig.22 depend on the following parameters:

1) Supply voltage
2) Bus capacitance
3) Number of connected devices (input current + leakage current)

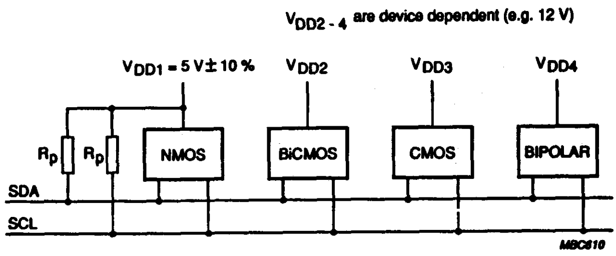


Fig.19 Fixed input level devices connected to the I²C-bus

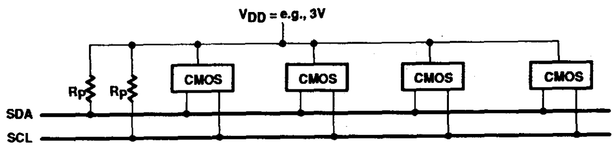


Fig.20 Devices with wide supply voltage range connected to the I²C-bus

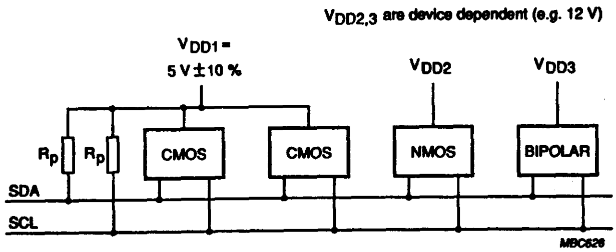


Fig.21 Devices with input levels related to V_{DD} (supply V_{DD1}) mixed with fixed input level devices (supply $V_{DD2, 3}$) on the I²C-bus

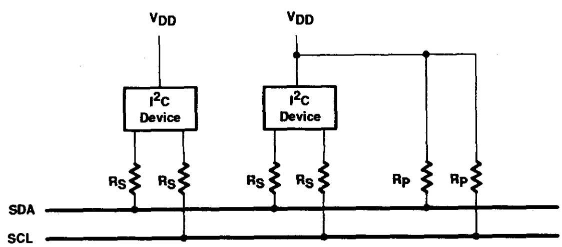


Fig.22 Series resistors (R_s) for protection against high-voltage spikes

I^2C-bus specification (including fast-mode)

The supply voltage limits the minimum value of resistor R_p due to the specified minimum sink current of 3 mA at V_{OLmax} = 0.4 V for the output stages. V_{DD} as a function of $R_{p\ min}$ is shown in Fig.23. The desired noise margin of $0.1V_{DD}$ for the LOW level limits the maximum value of R_S. $R_{S\ max}$ as a function of R_p is shown in Fig.24.

The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_p due to the specified rise time. Fig.25 shows $R_{p\ max}$ as a function of bus capacitance.

The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 µA. Due to the desired noise margin of $0.2V_{DD}$ for the HIGH level, this input current limits the maximum value of R_p. This limit depends on V_{DD}. The total HIGH level input current is shown as a function of R_p max in Fig.26.

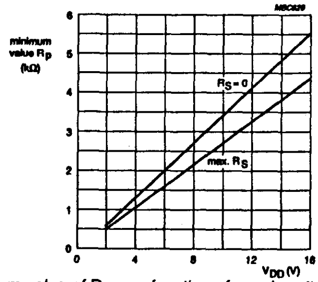


Fig.23 Minimum value of R_p as a function of supply voltage with the value of R_s as a parameter

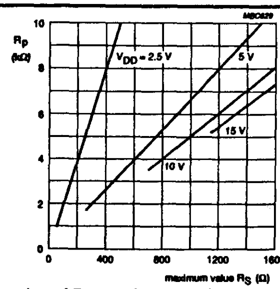


Fig.24 Maximum value of R_s as a function of the value of R_p with supply voltage as a parameter

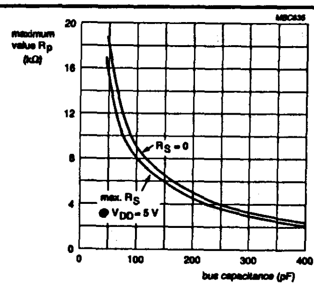


Fig.25 Maximum value of R_p as a function of bus capacitance for a standard-mode I^2C-bus

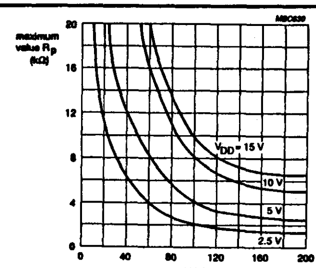


Fig.26 Total HIGH level input current as a function of the maximum value of R_p with supply voltage as a parameter

I²C-bus specification (including fast-mode)

10.0 EXTENSIONS TO THE I²C-BUS SPECIFICATION

The I²C-bus with a data transfer rate of up to 100 kbit/s and 7-bit addressing has now been in existence for more than ten years with an unchanged specification. The concept is accepted world-wide as a de facto standard and hundreds of different types of I²C-bus compatible ICs are available from Philips and other suppliers. The I²C-bus specification is now extended with the following two features:

- A **fast-mode** which allows a fourfold increase of the bit rate to 0 to 400 kbit/s
- **10-bit addressing** which allows the use of up to 1024 additional addresses.

There are two reasons for these extensions to the I²C-bus specification:

- New applications will need to transfer a larger amount of serial data and will therefore demand a higher bit rate than 100 kbit/s. Improved IC manufacturing technology now allows a fourfold speed increase without increasing the manufacturing cost of the interface circuitry
- Most of the 112 addresses available with the 7-bit addressing scheme have been issued more than once. To prevent problems with the allocation of slave addresses for new devices, it is desirable to have more address combinations. About a tenfold increase of the number of available addresses is obtained with the new 10-bit addressing.

All new devices with an I²C-bus interface are provided with the fast-mode. Preferably, they should be able to receive and/or transmit at 400 kbit/s. The minimum requirement is that they can synchronize with a 400 kbit/s transfer; they can then prolong the LOW period of the SCL signal to slow down the transfer. Fast-mode devices must be downward-compatible which means that they must still be able to communicate with 0 to 100 kbit/s devices in a 0 to 100 kbit/s I²C-bus system.

Obviously, devices with 0 to 100 kbit/s I²C-bus interface cannot be incorporated in a fast-mode I²C-bus system because, since they cannot follow the higher transfer rate. Unpredictable states of these devices would occur.

Slave devices with a fast-mode I²C-bus interface can have a 7-bit or 10-bit slave address. However, a 7-bit address is preferred because it is the cheapest solution in hardware and it results in the shortest message length. Devices with 7-bit and 10-bit addresses can be mixed in the same I²C-bus system regardless of whether it is a 0 to 100 kbit/s standard-mode system or a 0 to 400 kbit/s fast-mode system. Existing and future masters can generate 7-bit or 10-bit addresses.

11.0 FAST-MODE

In the fast-mode of the I²C-bus, the protocol, format, logic levels and maximum capacitive load for the SDA and SCL lines given in the previous I²C-bus specification remain unchanged. Changes to the previous I²C-bus specification are:

- The maximum bit rate is increased to 400 kbit/s
- Timing of the serial data (SDA) and serial clock (SCL) signals has been adapted. There is no need for compatibility with other bus systems such as CBUS because they cannot operate at the increased bit rate
- The inputs of fast-mode devices must incorporate spike suppression and a Schmitt trigger at the SDA and SCL inputs
- The output buffers of fast-mode devices must incorporate slope control of the falling edges of the SDA and SCL signals
- If the power supply to a fast-mode device is switched off, the SDA and SCL I/O pins must be floating so that they don't obstruct the bus lines
- The external pull-up devices connected to the bus lines must be adapted to accommodate the shorter maximum permissible rise time for the fast-mode I²C-bus. For bus loads up to 200 pF, the pull-up device for each bus line can be a resistor; for bus loads between 200 pF and 400 pF, the pull-up device can be a current source (3 mA max.) or a switched resistor circuit as shown in Fig.34.

12.0 10-BIT ADDRESSING

The 10-bit addressing does not change the format in the I²C-bus specification. Using 10 bits for addressing exploits the reserved combination 1111XXX for the first 7 bits of the first byte following a START (S) or repeated START (Sr) condition as explained in Section 8.1. The 10-bit addressing does not affect the existing 7-bit addressing. Devices with 7-bit and 10-bit addresses can be connected to the same I²C-bus, and both 7-bit and 10-bit addressing can be used in a standard-mode system (up to 100 kbit/s) or a fast-mode system (up to 400 kbit/s) system.

Although there are eight possible combinations of the reserved address bits 1111XXX, only the four combinations 11110XX are used for 10-bit addressing. The remaining four combinations 11111XX are reserved for future I²C-bus enhancements.

I²C-bus specification (including fast-mode)

12.1 Definition of bits in the first two bytes

The 10-bit slave address is formed from the first two bytes following a START condition (S) or a repeated START condition (Sr).

The first 7 bits of the first byte are the combination 11110XX of which the last two bits (XX) are the two most-significant bits (MSBs) of the 10-bit address; the eighth bit of the first byte is the $R/\overline{W}$ bit that determines the direction of the message. A 'zero' in the least significant position of the first byte means that the master will write information to a selected slave. A 'one' in this position means that the master will read information from the slave.

If $R/\overline{W}$ is 'zero', then the second byte contains the remaining 8 bits (XXXXXXXX) of the 10-bit address. If $R/\overline{W}$ is 'one', then the next byte contains data transmitted from slave to master.

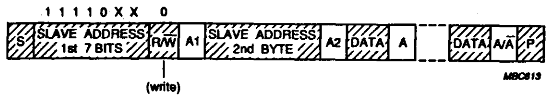


Fig.27 A master-transmitter addresses a slave-receiver with a 10-bit address

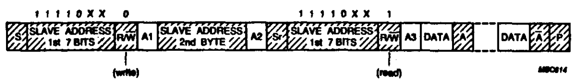


Fig.28 A master-receiver addresses a slave-transmitter with a 10-bit address

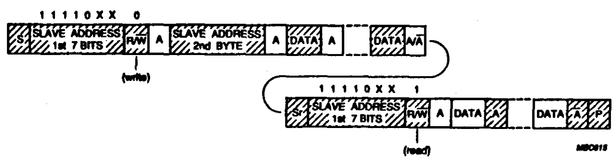


Fig.29 Combined format. A master addresses a slave with a 10-bit address, then transmits data to this slave and reads data from this slave

12.2 Formats with 10-bit addresses

Various combinations of read/write formats are possible within a transfer that includes 10-bit addressing. Possible data transfer formats are:

- **Master-transmitter transmits to slave-receiver with a 10-bit slave address. The transfer direction is not changed (Fig.27).** When a 10-bit address follows a START condition, each slave compares the first 7 bits of the first byte of the slave address (11110XX) with its own address and tests if the eighth bit ($R/\overline{W}$ direction bit) is 0. It is possible that more than one device will find a match and generate an acknowledge (A1). All slaves that found a match will compare the 8 bits of the second byte of the slave address (XXXXXXXX) with their own addresses, but only one slave will find a match and generate an acknowledge (A2). The matching slave will remain addressed by the master until it receives a STOP condition (P) or a repeated START condition (Sr) followed by a different slave address.
- **Master-receiver reads slave-transmitter with a 10-bit slave address. The transfer direction is changed after the second $R/\overline{W}$ bit (Fig.28).** Up to and including acknowledge bit A2, the procedure is the same as that described above for a master-transmitter

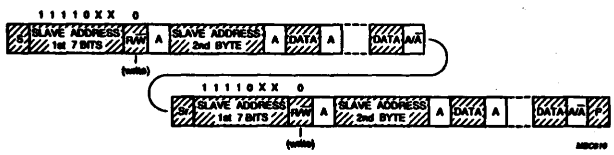


Fig.30 Combined format. A master transmits data to two slaves, both with 10-bit addresses

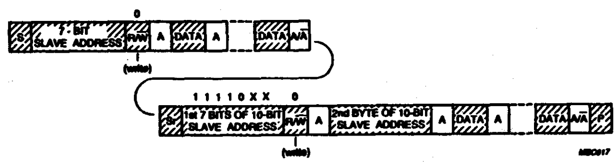


Fig.31 Combined format. A master transmits data to two slaves, one with a 7-bit address, and one with a 10-bit address

addressing a slave-receiver. After the repeated START condition (Sr), a matching slave remembers that it was addressed before. This slave then checks if the first 7 bits of the first byte of the slave address following Sr are the same as before after the START condition (S), and tests if the eighth (R/$\overline{W}$) bit is 1. If there is a match, the slave considers that it has been addressed as a transmitter and generates acknowledge A3. The slave-transmitter remains addressed until it receives a STOP condition (P) or until it receives another repeated START condition (Sr) followed by a different slave address. After Sr, all the other slave devices will also compare the first 7 bits of the first byte of the slave address (11110XX) with their own addresses and test the eighth (R/$\overline{W}$) bit. However, none of them will be addressed because R/$\overline{W}$ = 1 (for 10-bit devices), or the 11110XX slave address (for 7-bit devices) does not match)

- **Combined format. A master transmits data to a slave and then reads data from the same slave (Fig.29).** The same master occupies the bus all the time. The transfer direction is changed after the second R/$\overline{W}$ bit
- **Combined format. A master transmits data to one slave and then transmits data to another slave (Fig.30).** The master occupies the bus all the time
- **Combined format. 10-bit and 7-bit addressing combined in one serial transfer (Fig.31).** After each START condition (S), or each repeated START condition (Sr), a 10-bit or 7-bit slave address can be transmitted. Figure 30 shows how a master-transmits data to a slave with a 7-bit address and then transmits data to a slave with a 10-bit address. The same master occupies the bus all the time.

NOTES:

1) Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the START condition and slave address is repeated, data can be transferred.
2) All decisions on auto-increment or decrement of previously accessed memory locations etc. are taken by the designer of the device.
3) Each byte is followed by an acknowledgement bit as indicated by the A or $\overline{A}$ blocks in the sequence.
4) I²C-bus compatible devices must reset their bus logic on receipt of a START or repeated START condition such that they all anticipate the sending of a slave address.

13.0 GENERAL CALL ADDRESS AND START BYTE

The 10-bit addressing procedure for the I²C-bus is such that the first two bytes after the START condition (S) usually determine which slave will be selected by the master. The exception is the 'general call' address 00000000 (H'00'). Slave devices with 10-bit addressing will react to a 'general call' in the same way as slave devices with 7-bit addressing (see Section 8.1.1).

Hardware masters can transmit their 10-bit address after a 'general call'. In this case, the 'general call' address byte is followed by two successive bytes containing the 10-bit address of the master-transmitter. The format is as shown in Fig. 15 where the first DATA byte contains the eight least-significant bits of the master address.

The START byte 00000001 (H'01') can precede the 10-bit addressing in the same way as for 7-bit addressing (see Section 8.1.2).

14.0 APPLICATION INFORMATION FOR FAST-MODE I²C-BUS DEVICES

14.1 Output stage with slope control

The electrical specifications for the I/Os of I²C-bus devices and the characteristics of the bus lines connected to them are given in Tables 3 and 4 in Section 15.

Figures 32 and 33 show examples of output stages with slope control in CMOS and bipolar technology. The slope of the falling edge is defined by a Miller capacitor (C1) and a resistor (R1). The typical values for C1 and R1 are indicated on the diagrams. The wide tolerance for output fall time t_{OF} given in Table 3 means that the design is not critical. The fall time is only slightly influenced by the external bus load (C_b) and external pull-up resistor (R_p). However, the rise time (t_R) specified in Table 4 is mainly determined by the bus load capacitance and the value of the pull-up resistor.

14.2 Switched pull-up circuit

The supply voltage (V_{DD}) and the maximum output LOW level determine the minimum value of pull-up resistor R_p (see Section 9.1). For example, with a supply voltage of V_{DD} = 5 V ± 10% and $V_{OL\ max.}$ = 0.4 V at 3 mA, $R_{p\ min.}$ = (5.5 − 0.4)/0.003 = 1.7 kΩ. As shown in Fig.35, this value of R_p limits the maximum bus capacitance to about 200 pF to meet the maximum t_R requirement of 300 ns. If the bus has a higher capacitance than this, a switched pull-up circuit as shown in Fig.34 can be used.

The switched pull-up circuit in Fig.34 is for a supply voltage of V_{DD} = 5 V ± 10 % and a maximum capacitive load of 400 pF. Since it is controlled by the bus levels, it needs no additional control signals. During the rising/falling edges, the bilateral switch in the HCT4066 switches pull-up resistor R_p2 on/off at bus levels between 0.8 V and 2.0 V. Combined resistors R_p1 and R_p2 can pull-up the bus line within the maximum specified rise time (t_R) of 300 ns. The maximum sink current for the driving I²C-bus device will not exceed 6 mA at V_{OL2} = 0.6 V, and 3 mA at V_{OL1} = 0.4 V.

Series resistors R_s are optional. They protect the I/O stages of the I²C-bus devices from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus line signals. The maximum value of R_s is determined by the maximum permitted voltage drop across this resistor when the bus line is switched to the LOW level in order to switch off R_p2.

14.3 Wiring pattern of the bus lines

In general, the wiring must be so chosen that crosstalk and interference to/from the bus lines is minimized. The bus lines are most susceptible to crosstalk and interference at the HIGH level because of the relatively high impedance of the pull-up devices.

If the length of the bus lines on a PCB or ribbon cable exceeds 10 cm and includes the V_{DD} and V_{SS} lines, the wiring pattern must be:

SDA
V_{DD}
V_{SS}
SCL

If only the V_{SS} line is included, the wiring pattern must be:

SDA
V_{SS}
SCL

I²C-bus specification (including fast-mode)

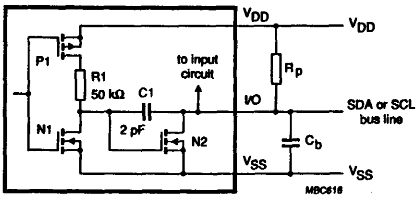


Fig.32 Slope-controlled output stage in CMOS technology

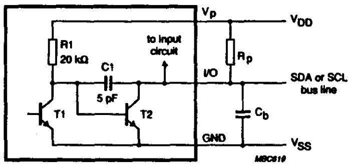


Fig.33 Slope-controlled output stage in bipolar technology

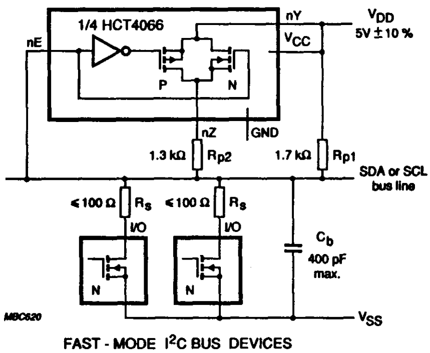


Fig.34 Switched pull-up circuit

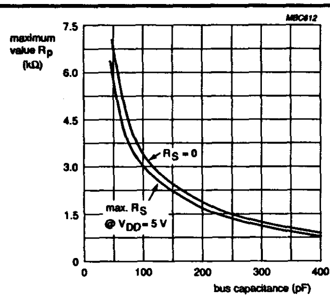


Fig.35 Maximum value of R_p as a function of bus capacitance for meeting the $t_{R\,max}$ requirement for a fast-mode I²C-bus

These wiring patterns also result in identical capacitive loads for the SDA and SCL lines. The V_{SS} and V_{DD} lines can be omitted if a PCB with a V_{SS} and/or V_{DD} layer is used.

If the bus lines are twisted-pairs, each bus line must be twisted with a V_{SS} return. Alternatively, the SCL line can be twisted with a V_{SS} return, and the SDA line twisted with a V_{DD} return. In the latter case, capacitors must be used to decouple the V_{DD} line to the V_{SS} line at both ends of the twisted pairs.

If the bus lines are shielded (shield connected to V_{SS}), interference will be minimized. The shielded cable must have low capacitive coupling between the SDA and SCL lines to minimize crosstalk.

14.4 Maximum and minimum values of resistors R_p and R_s

The maximum and minimum values for resistors R_p and R_s connected to a fast-mode I²C-bus can be determined from Fig.23, 24 and 26 in Section 9.1. Because a fast-mode I²C-bus has faster rise times (t_R) the maximum value of R_p as a function of bus capacitance is less than that shown in Fig.25 The replacement graph for Fig.25 showing the maximum value of R_p as a function of bus capacitance (C_b) for a fast mode I²C-bus is given in Fig.35.

I^2C-bus specification (including fast-mode)

15.0 ELECTRICAL SPECIFICATIONS AND TIMING FOR I/O STAGES AND BUS LINES

The I/O levels, I/O current, spike suppression, output slope control and pin capacitance for I^2C-bus devices are given in Table 3. The I^2C-bus timing is given in Table 4. Figure 36 shows the timing definitions for the I^2C-bus.

The noise margin for levels on the bus lines for fast-mode devices are the same as those specified in Section 9.0 for standard-mode I^2C-bus devices.

The minimum HIGH and LOW periods of the SCL clock specified in Table 4 determine the maximum bit transfer rates of 100 kbit/s for standard-mode devices and 400 kbit/s for fast mode devices. Standard-mode and fast-mode I^2C-bus devices must be able to follow transfers at their own maximum bit rates, either by being able to transmit or receive at that speed or by applying the clock synchronization procedure described in Section 6 which will force the master into a wait state and stretch the LOW period of the SCL signal. Of course, in the latter case the bit transfer rate is reduced.

Table 3 Characteristics of the SDA and SCL I/O stages for I^2C-bus devices

Parameter	Symbol	standard-mode devices		fast-mode devices		Unit
		Min.	Max.	Min.	Max.	
LOW level input voltage:	V_{IL}					V
fixed input levels		−0.5	1.5	−0.5	1.5	
V_{DD}-related input levels		−0.5	$0.3V_{DD}$	−0.5	$0.3V_{DD}$	
HIGH level input voltage:	V_{IH}					V
fixed input levels		3.0	*1)	3.0	*1)	
V_{DD}-related input levels		$0.7V_{DD}$	*1)	$0.7V_{DD}$	*1)	
Hysteresis of Schmitt trigger inputs:	V_{hys}					V
fixed input levels		n/a	n/a	0.2	-	
V_{DD}-related input levels		n/a	n/a	$0.05V_{DD}$	-	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	n/a	n/a	0	50	ns
LOW level output voltage (open drain or open collector):						V
at 3 mA sink current	V_{OL1}	0	0.4	0	0.4	
at 6 mA sink current	V_{OL2}	n/a	n/a	0	0.6	
Output fall time from $V_{IH\,min.}$ to $V_{IL\,max.}$ with a bus capacitance from 10 pF to 400 pF:	t_{OF}					ns
with up to 3 mA sink current at V_{OL1}		-	250[2)]	$20 + 0.1C_b$[2)]	250	
with up to 6 mA sink current at V_{OL2}		n/a	n/a	$20 + 0.1C_b$[2)]	250[3)]	
Input current each I/O pin with an input voltage between 0.4 V and $0.9V_{DD\,max.}$	I_i	−10	10	−10[3)]	10[3)]	µA
Capacitance for each I/O pin	C_i	-	10	-	10	pF

n/a = not applicable

1) maximum $V_{IH} = V_{DD\,max.} + 0.5$ V

2) C_b = capacitance of one bus line in pF. Note that the maximum t_F for the SDA and SCL bus lines quoted in Table 4 (300 ns) is longer than the specified maximum t_{OF} for the output stages (250 ns). This allows series protection resistors (R_s)to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Fig.34 without exceeding the maximum specified t_F.

3) I/O pins of fast-mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.

I^2C-bus specification (including fast-mode)

Table 4 Characteristics of the SDA and SCL bus lines for I^2C-bus devices

Parameter	Symbol	Standard-mode I^2C-bus		Fast-mode I^2C-bus		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data hold time:	$t_{HD;DAT}$					
for CBUS compatible masters (see NOTE, Section 8.1.3)		5.0	-	-	-	µs
for I^2C-bus devices		0[1]	-	0[1]	0.9[2]	µs
Data set-up time	$t_{SU;DAT}$	250	-	100[3]	-	ns
Rise time of both SDA and SCL signals	t_R	-	1000	20 + $0.1C_b$[4]	300	ns
Fall time of both SDA and SCL signals	t_F	-	300	20 + $0.1C_b$[4]	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	µs
Capacitive load for each bus line	C_b	-	400	-	400	pF

All values referred to $V_{IH\,min.}$ and $V_{IL\,max.}$ levels (see Table 3).

1) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH\,min.}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

2) The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

3) A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\,max.} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode I^2C-bus specification) before the SCL line is released.

4) C_b = total capacitance of one bus line in pF.

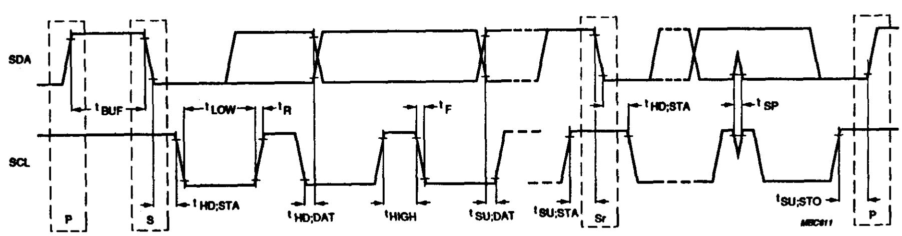


Fig.36 Definition of timing on the I^2C-bus

I²C bus addresses

ASSIGNED I²C BUS ADDRESSES

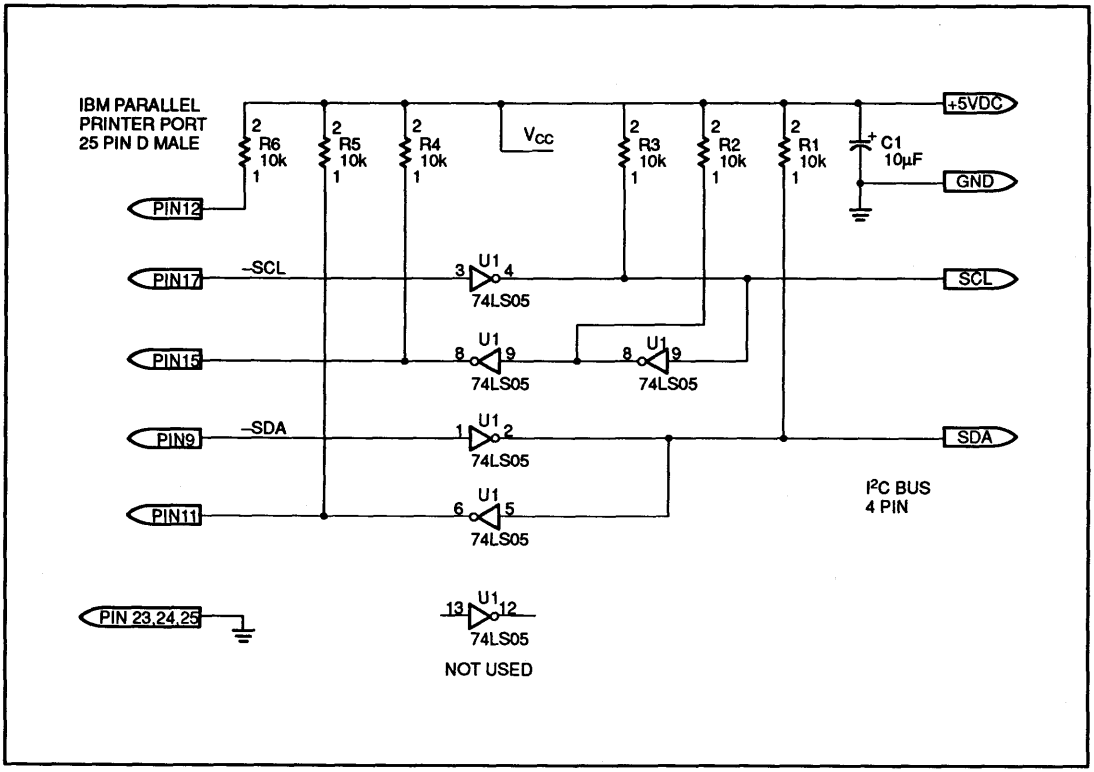
PART NUMBER	FUNCTION	I²C ADDRESS A6	A5	A4	A3	A2	A1	A0
—	General call address	0	0	0	0	0	0	0
—	Reserved addresses	0	0	0	0	X	X	X
PCF8574	I²C bus to 8-bit bus converter	0	1	0	0	A	A	A
PCF8574A	I²C bus to 8-bit bus converter	0	1	1	1	A	A	A
SAA5252	Closed caption decoder	0	0	1	0	1	0	0
SAA7151B	Digital multistandard colour decoder with SCART interface	1	0	0	0	1	A	1
SAA7152	Digital combination filter	1	0	1	1	0	0	1
SAA7194 (7196)	Digital video decoder and scaler circuit (DESC)	0	1	0	0	0	0	A
SAA7191B	S-VHS digital multistandard decoder "square pixel"	1	0	0	0	1	A	1
SAA7192A	Digital color space converter	1	1	1	0	0	0	A
SAA7199	Digital encoder	1	0	1	1	0	0	0
SAA9051	Digital multi-standard TV decoder	1	0	0	0	1	0	1
TDA4670	Picture signal improvement circuit	1	0	0	0	1	0	0
TDA4680/4686	Video processor	1	0	0	0	1	0	0
TDA8440	Switch for CTV receivers	1	0	0	1	A	A	A
TDA8442	Interface for color decoders	1	0	0	0	1	0	0
TDA8443	YUV/RGB interface circuit	1	1	0	1	A	A	A
TDA8444	Octuple 6-bit DAC	0	1	0	0	A	A	A
TDA9141	PAL/NTSC/SECAM decoder/sync processor	1	0	0	0	1	A	1

X = Don't care.
A = Can be connected high or low by the user.

I^2C parallel printer port adaptor

The schematic below shows how Philips I^2C software programs are able to communicate through any IBM-compatible PC parallel printer port using I^2C serial protocol. The software toggles the SDA and SCL lines in a manner compatible with all I^2C integrated circuits and I^2C evaluation boards such as DTV7191 and DTV9051. Some variations of the four-wire I^2C bus pinning have changed the order of the clock, data power and ground. Check the pinning required for each evaluation board connected using this type of interface. Power for the interface board must come from the application, not the PC printer port.

I^2C PARALLEL PRINTER PORT ADAPTOR



Interfacing the PCD8584 I²C-bus controller to 80C51 family microcontrollers

AN425

DESCRIPTION

This application note shows how to use the PCD8584 I²C-bus controller with 80C51 family microcontrollers. One typical way of connecting the PCD8584 to an 80C31 is shown. Some basic software routines are described showing how to transmit and receive bytes in a single master system. An example is given of how to use these routines in an application that makes use of the I²C circuits on an I²C demonstration board.

The PCD8584 is used to interface between parallel microprocessor or microcontroller buses and the serial I²C bus. For a description of the I²C bus protocol refer to the I²C bus specification which is printed in the microcontroller user guide.

The PCD8584 controls the transmission and reception of data on the I²C bus, arbitration, clock speeds and transmission and reception of data on the parallel bus. The parallel bus is compatible with 80C51, 68000, 8085 and Z80 buses. Communication with the I²C-bus can be done on an interrupt or polled basis. This application note focuses on interfacing with 8051 microcontrollers in single master systems.

PCD8584

In Figure 1, a block diagram is shown of the PCD8584. Basically it consists of an I²C-interface similar to the one used in 84Cxx family microcontrollers, and a control block for interfacing to the microcontroller.

The control block can automatically determine whether the control signals are from 80xx or 68xxx type of microcontrollers.

This is determined after the first write action from the microcontroller to the PCD-8584. The control block also contains a programmable divider which allows the selection of different PCD8584 and I²C clocks.

The I²C interface contains several registers which can be written and read by the microcontroller.

S1 is the control/status register. This register is accessed while the A0 input is 1. The meaning of the bits depends on whether the register is written to or read from. When used as a single master system the following bits are important:

PIN: Interrupt bit. This bit is made active when a byte is sent/received to/from the I²C-bus. When ENI is made active, PIN also controls the external INT line to interrupt the microcontroller.

ES0–ES2: These bits are used as pointer for addressing S0, S0', S2 and S3. Setting ES0 also enables the Serial I/O.

ENI: Enable Interrupt bit. Setting this bit enables the generation of interrupts on the INT line.

STA, STO: These bits allow the generation of START or STOP conditions.

ACK: With this bit set and the PCD8584 is in master/receiver mode, no acknowledge is generated by the PCD8584. The slave/transmitter now knows that no more data must be sent to the I²C-bus.

BER: This bit may be read to check if bus errors have occurred.

BB: This bit may be read to check whether the bus is free for I²C-bus transmission.

S2 is the clock register. It is addressed when A0 = 0 and ES0–ES2 = 010 in the previous write cycle to S1. With the bits S24–S20 it is possible to select 5 input clock frequencies and 4 I²C clock frequencies.

S3 is the interrupt vector register. It is addressed when A0 = 0 and ES0–ES2 = 001 in the previous write cycle to S1. This register is not used when an 80C51 family microcontroller is used. An 80C51 microcontroller has fixed interrupt vector addresses.

S0' is the own address register. It is addressed when A0 = 0 and ES0–ES2 = 000. This register contains the slave address of the PCD8584. In the single master system described here, this register has no functional use. However, by writing a value to S0', the PCD8584 determines whether an 80Cxx or 68xxx type microcontroller is the controlling microcontroller by looking at the $\overline{CS}$ and $\overline{WR}$ lines. So independent of whether the PCD8584 is used as master or slave, the microcontroller should always first write a value to S0' after reset.

S0 is the I²C data register. It is addressed when A0 = 0 and ES0–ES2 = 1x0. Transmission of a byte on the I²C bus is done by writing this byte to S0. When the transmission is finished, the PIN bit in S1 is reset and if ENI is set, an interrupt will be generated. Reception of a byte is signaled by resetting PIN and by generating an interrupt if ENI is set. The received byte can be read from S0.

The SDA and SCL lines have no protection diodes to V_{DD}. This is important for multi-master systems. A system with a PCD8584 can now be switched off without causing the I²C-bus to hang-up. Other masters still can use the bus.

For more information of the PCD8584 refer to the data sheet.

PCD8584/8031 Hardware Interface

Figure 2 shows a minimum system with an 8051 family controller and a PCD8584. In this example, an 80C31 is used. However any 80C51 family controller with external addressing capability can be used.

The software resides in EPROM U3. For addressing this device, latch U2 is necessary to demultiplex the lower address bits from the data bits. The PCD8584 is mapped in the external data memory area. It is selected when A1 = 0. Because in this example no external RAM or other mapped peripherals are used, no extra address decoding components are necessary. A0 is used by the PCD8584 for proper register selection in the PCD8584.

U5A is an inverter with Schmitt trigger input and is used to buffer the oscillator signal of the microcontroller. Without buffering, the rise and fall time specifications of the CLK signal are not met. It is also important that the CLK signal has a duty cycle of 50%. If this is not possible with certain resonators or microcontrollers, then an extra flip-flop may me necessary to obtain the correct duty cycle.

U5C and U5D are used to generate the proper reset signals for the microcontroller and the PCD8584.

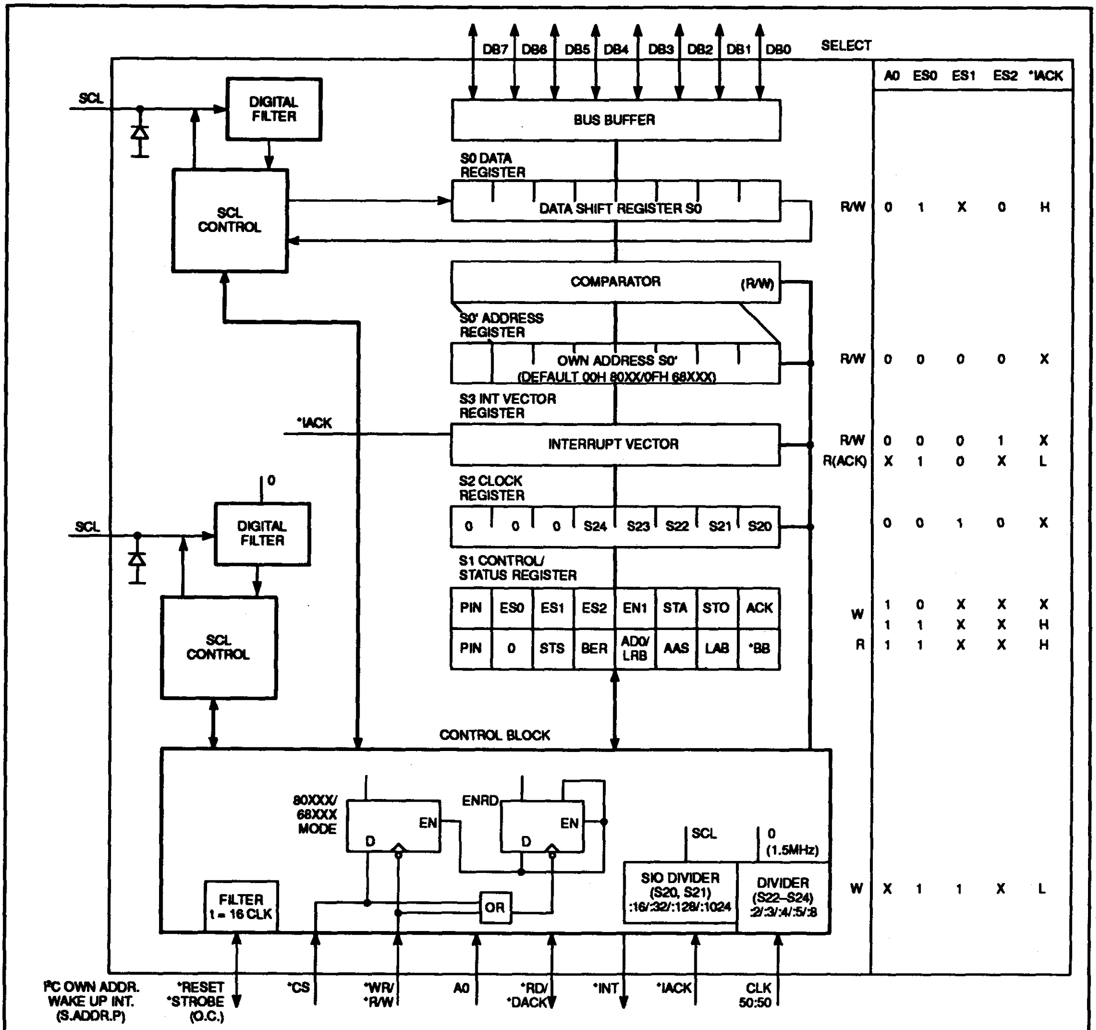


Figure 1. PCD8584 Block Diagram

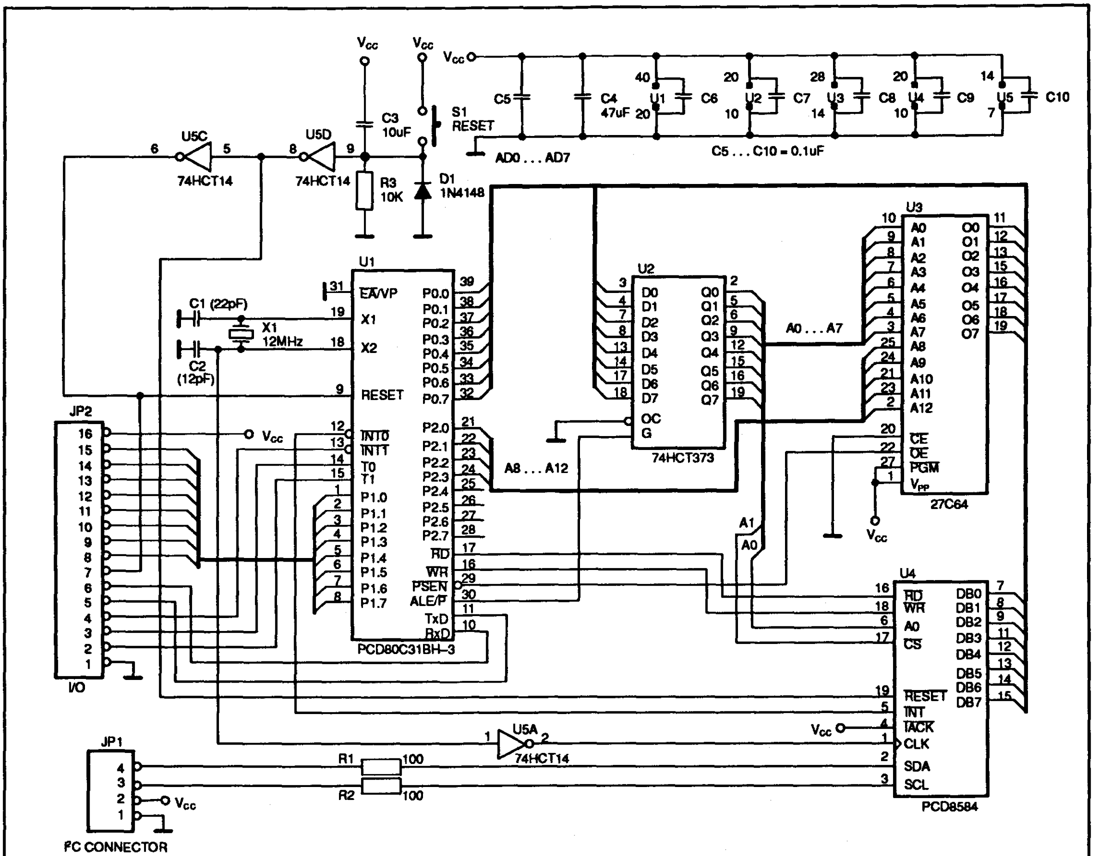


Figure 2. PCD8584 to 80C31 Interface

Basic PCD8584/8031 Driver Routines

In the listing section (page 2-210), some basic routines are shown. The routines are divided in two modules. The module ROUTINE contains the driver routines and initialization of the PCD8584. The module INTERR contains the interrupt handler. These modules may be linked to a module with the user program that uses the routines in INTERR and ROUTINE. In this application note, this module will be called USER. A description of ROUTINE and INTERR follows.

Module ROUTINE

Routine Sendbyte (Lines 17–20)—
This routine sends the contents of the accumulator to the PCD8584. The address is such that A0 = 0. Which register is accessed depends on the contents of ES0–ES2 of the control register. The address of the PCD8584 is in variable 'PCD8584'. This must have been previously defined in the user program. The DPTR is used as a pointer for addressing the peripheral. If the address is less than 255, then R0 or R1 may be used as the address pointer.

Routine Sendcontr (Lines 25, 26)—
This routine is similar to Sendbyte, except that now A0 = 1. This means that the contents of the accumulator are sent to the control register S1 in the PCD8584.

Routine Readbyte (Lines 30–33)—
This routine reads a register in the PCD8584 with A0 = 0. Which register depends on ESO –ES2 of the control register. The result of the read operation is returned in the accumulator.

Routine Readcontr (Lines 37–39)—
This routine is similar to Readbyte, except that now A0 = 1. This means that the accumulator will contain the value of status register S1 of the PCD8584.

Routine Start Lines (44–56)—
This routine generates a START–condition and the slave address with a R/W bit. In line 44, the variable IIC_CNT is reset. This variable is used as a byte counter to keep track of the number of bytes that are received or transmitted. IIC_CNT is defined in module INTERR.

Lines 45–46 increment the variable NR_BYTES if the PCD8584 must receive data. NR_BYTES is a variable that indicates how many bytes have to be received or transmitted. It must be given the correct value in the USER module. Receiving or transmitting is distinguished by the value of the DIR bit. This must also be given the correct value in the USER module.

Then the status register of PCD8584 must be read to check if the I²C bus is free. First the status register must be addressed by giving ES0– ES2 of the control register the correct value (lines 47–48). Then the Bus Busy bit is tested until the bus is free (lines 49–50). If this is the case, the slave address is sent to data register S0 and the I2C_END bit is cleared (lines 51–53). The slave address is set by the user program in variable USER. The LSB of the slave address is the R/W bit. I2C_END can be tested by the user program whether an I2C reception/transmission is in progress or not.

Next the START condition will be generated and interrupt generation enabled by setting the appropriate bits in control register S1. (lines 54–55).

Now the routine will return back to the user program and other tasks may be performed. When the START condition, slave address and R/W bit are sent, and the ACK is received, the PCD8584 will generate an interrupt. The interrupt routine will determine if more bytes have to be received or transmitted.

Routine Stop (Lines 59–62) —
Calling this routine, a STOP condition will be sent to the I²C bus. This is done by sending the correct value to control register S1 (lines 59– 61). After this the I2C_END bit is set, to indicate to the user program that a complete I²C sequence has been received or transmitted.

Routine I2C_Init (Lines 65–76)—
This routine initializes the PCD8584. This must be done directly after reset. Lines 67–70 write data to 'own address' register S0'. First the correct address of S0' is set in control register S1 (lines 67–68), then the correct value is written to it (lines 69–70). The value for S0' is in variable SLAVE_ADR and set by the user program. As noted previously, register S0' must always be the first register to be accessed after reset, because the PCD8584 now determines whether an 80Cxxx or 68xxx microcontroller is connected. Lines 72–76 set the clock register S2. The variable I2C_CLOCK is also set by the user program.

Module INTERR
This module contains the I²C interrupt routine. This routine is called every time a byte is received or transmitted on the I²C bus. In lines 12–15 RAM space for variables is reserved.

BASE is the start address in the internal 80C51 RAM where the data is stored that is received, or where the data is stored that has to be transmitted.

NR_BYTES, IIC_CNT and SLAVE were explained earlier. I2C_END and DIR are flags that are used in the program. I2C_END indicates whether an I²C transmission or reception is in progress. DIR indicates whether the PCD8584 has to receive or transmit bytes. The interrupt routine makes use of register bank 1.

The transmission part of the routine starts at line 42. In lines 42–43, a check is made whether IIC_CNT = NR_BYTES. If true, all bytes are sent and a STOP condition may be generated (lines 44–45).

Next the pointer for the internal RAM is restored (line 46) and the byte to be transmitted is fetched from the internal RAM (line 47). Then this byte is sent to the PCD8584 and the variables are updated (lines 47–49). The interrupt routine is left and the user program may proceed. The receive part starts from line 55. First a check is made if the next byte to be received is the last byte (lines 56–59). If true the ACK must be disabled when the last byte is received. This is accomplished by resetting the ACK bit in the control register S1 (lines 60–61).

Next the received byte may be read (line 62) from data register S0. The byte will be temporary stored in R4 (line 63). Then a check is made if this interrupt was the first after a START condition. If so, the byte read has no meaning and the interrupt routine will be left (lines 68–70). However by reading the data register S0 the next read cycle is started.

If valid data is received, it will be stored in the internal RAM addressed by the value of BASE (lines 71–73). Finally a check is made if all bytes are received. If true, a STOP condition will be sent (lines 75–78).

EXAMPLES
In the listing section (starting on page 8), some examples are shown that make use of the routines described before. The examples are transmission of a sequence, reception of I²C data and an example that combines both.

The first example sends bytes to the PCD 8577 LCD driver on the OM1016 demonstration board. Lines 7 to 10 define the interface with the other modules and should be included in every user program. Lines 14 to 16 define the segments in the user module. It is completely up to the user how to organize this.

Lines 24 and 28 are the reset and interrupt vectors. The actual user program starts at line 33. Here three variables are defined that are used in the I²C driver routines. Note that PCD8584 must be an even address, otherwise the wrong internal registers will be accessed! Lines 37–42 initialize the interrupt logic of the microcontroller. Next the PCD8584 will be initialized (line 45).

The PCD8584 is now ready to transmit data. A table is made in the routine at line 61. For the PCD8577, the data is a control byte and the segment data. Note that the table does not contain the slave address of the LCD driver. In lines 51–54, variables are made ready to start the transmission. This consists of defining the direction of the transmission (DIR), the address where the data table starts (BASE), the number of bytes to transmit (NR_BYTES, without slave address!) and the slave address (SLAVE) of the I²C peripheral that has to be accessed.

In line 55 the transmission is started. Once the I²C transmission is started, the user program can do other tasks because the transmission works on interrupts. In this example a loop is performed (line 58). The user can check the end of the transmission during the other tasks, by testing the I2C_END bit regularly.

The second example program receives 2 bytes from the PCF8574P I/O expander on the OM1016 demonstration board. Until line 45 the program is identical to the transmit routine because it consists of initialization and variable definition. From line 48, the variables are set for I²C reception. The received bytes are stored in RAM area from label TABLE. During reception, the user program can do other tasks. By testing the I2C_END bit the user can determine when to start processing the data in the TABLE.

The third example program displays time from the PCF8583P clock/calendar/RAM on the LCD display driven by the PCF8577. The LED display (driven by SAA1064) shows the value of the analog inputs of the A/D converter PCF8591. The four analog inputs are scanned consecutively.

In this example, both transmit and receive sequences are implemented as shown in the previous examples. The main clock part is from lines 62–128. This contains the calls to the I²C routines. From lines 135–160, routines are shown that prepare the data to be transmitted. Lines 171 to 232 are the main program for the AD converter and LED display. Lines 239 to 340 contain routines used by the main program. This demo program can also be used with the I²C peripherals on the OM1016 demonstration board.

```
ASM51  TSW  ASSEMBLER   Routines for PCD8584

LOC    OBJ        LINE  SOURCE

                        $TITLE (Routines for PCD8584)
                        $PAGELENGTH(40)
                        ;Program written for PCD8584 as master
                        ;
                                PUBLIC READBYTE,READCONTR,SENDBYTE
                                PUBLIC SENDCONTR,START,STOP
                                PUBLIC I2C_INIT
                                EXTRN  BIT(I2C_END,DIR)
                                EXTRN  DATA(SLAVE,IIC_CNT,NR_BYTES)
                                EXTRN  NUMBER(SLAVE_ADR,I2C_CLOCK,PCD8584)
                        ;
                        ;Define code segment
                        ROUTINE   SEGMENT CODE
----                              RSEG    ROUTINE
                        ;
                        ;SENDBYTE sends a byte to PCD8584 with A0=0
                        ;Byte to be send must be in accu
0000:            R      SENDBYTE:
0000: 900000     R              MOV DPTR,#PCD8584 ;Register address
0003: F0                SEND:   MOVX @DPTR,A     ;Send byte
0004: 22                        RET
                        ;
                        ;SENDCONTR sends a byte to PCD8584 with A0=1
                        ;Byte to be send must be in accu
0005:                   SENDCONTR:
0005: 900001     R              MOV DPTR,#PCD8584+01H ;Register address
0008: 80F9                      JMP SEND
                        ;
                        ;READBYTE reads a byte from PCD8584 with A0=0
                        ;Received byte is stored in accu
000A:                   READBYTE:
000A: 900000     R              MOV DPTR,#PCD8584 ;Register address
000D: E0                REC:    MOVX A,@DPTR     ;Receive byte
000E: 22                        RET
                        ;
                        ;READCONTR reads a byte from PCD8584 with A0=1
                        ;Received byte is stored in accu
000F:                   READCONTR:
000F: 900001     R              MOV DPTR,#PCD8584+01H ;Register address
0012: 80F9                      JMP REC
                        ;
                        ;START tests if the I2C bus is ready. If ready a
                        ;START-condition will be sent, interrupt generation
                        ;and acknowledge will be enabled.
0014: 750000     R      START:  MOV IIC_CNT,#00 ;Clear  I2C byte counter
0017: 200002     R              JB DIR,PROCEED  ;If DIR is 'receive' then
001A: 0500       R              INC NR_BYTES    ;increment NR_BYTES
001C: 7440              PROCEED:MOV A,#40H      ; Read STATUS register of
                                                ; 8584
001E: 120005     R              CALL SENDCONTR
0021: 12000F     R      TESTBB: CALL READCONTR
0024: 30E0FA                    JNB ACC.0,TESTBB; Test BB/ bit
0027: E500       R              MOV A,SLAVE
0029: C200       R              CLR I2C_END     ;Reset I2C ready bit
002B: 120000     R              CALL SENDBYTE   ;Send slave address
002E: 744D                      MOV A,#01001101B;Generate START, set ENI,
                                                ;set ACK
```

```
0030: 120005   R          CALL SENDCONTR
0033: 22                  RET
                  ;
                  ;STOP will generate a STOP condition and set the
                  ;I2C_END bit
0034: 74C3        STOP:   MOV A,#11000011B
0036: 120005   R          CALL SENDCONTR  ;Send STOP condition
0039: D200     R          SETB I2C_END    ;Set I2C_END bit
003B: 22                  RET
                  ;
                  ;I2C_init does the initialisation of the PCD8584
003C:             I2C_INIT:
                  ;Write own slave address
003C: E4                  CLR A
003D: 120005   R          CALL SENDCONTR  ;Write to control register
0040: 7400     R          MOV A,#SLAVE_ADR
0042: 120000   R          CALL SENDBYTE     ;Write to own slave
                                            ;register
                  ;Write clock register
0045: 7420                MOV A,#20H
0047: 120005   R          CALL SENDCONTR  ;Write to control register
004A: 7400     R          MOV A,#I2C_CLOCK
004C: 120000   R          CALL SENDBYTE   ;Write to clock register
004F: 22                  RET
                  ;
0050:                     END
```

```
ASM51  TSW  ASSEMBLER   I2C INTERRUPT ROUTINE

LOC    OBJ              SOURCE

                        $TITLE (I2C INTERRUPT ROUTINE)
                        $PAGELENGTH(40)
                        ;
                                PUBLIC INT0_SRV
                                PUBLIC DIR,I2C_END
                                PUBLIC BASE,NR_BYTES,IIC_CNT,SLAVE
                                EXTRN  CODE(SENDBYTE,SENDCONTR,STOP)
                                EXTRN  CODE(READBYTE,READCONTR)
                        ;
                        ;Define variables in RAM
                        IIC_VAR SEGMENT DATA
----                            RSEG IIC_VAR
0000:              R    BASE:   DS 1            ;Pointer to I2C table (till
                                                ;256)
0001:                   NR_BYTES: DS 1          ;Number of bytes to rcv/trm
0002:                   IIC_CNT:DS 1            ;I2C byte counter
0003:                   SLAVE:  DS 1            ;Slave address after START
                        ;
                        ;Define variable segment
                        BIT_VAR SEGMENT DATA BITADDRESSABLE
----                            RSEG BIT_VAR
0000:              R    STATUS: DS 1            ;Byte with flags
0000               R    I2C_END BIT STATUS.0    ;Defines if a I2C
                                                ;transmission is finished
                                                ;'1' is finished
                                                ;'0' is not ready
0000               R    DIR     BIT STATUS.3    ;Defines direction of I2C
                                                ;transmission
                                                ;'1':Transmit    '0':Receive
                        ;
                        ;Define code segment for routine
                        IIC_INT SEGMENT CODE PAGE
----                            RSEG IIC_INT
                        ;
                        ;Program uses registers in RB1
                                USING 1
                        ;
0000:              R    INT0_SRV:
0000: C0E0                      PUSH ACC        ;Save acc. en psw on stack
0002: C0D0                      PUSH PSW
0004: 75D008                    MOV PSW,#08H    ;Select register bank 1
0007: 300016       R            JNB DIR,RECEIVE ;Test direction bit
                                                ;8584 is MST/TRM

                        ;Program part to transmit bytes to IIC bus
000A: E502         R            MOV A,IIC_CNT   ;Compare IIC_CNT and
                                                ;NR_BYTES
000C: B50105       R            CJNE A,NR_BYTES,PROCEED
000F: 120000       R            CALL STOP       ;All bytes transmitted
0012: 8032                      JMP EXIT
0014: A800         R    PROCEED:MOV R0,BASE     ;RAM pointer
0016: E6                        MOV A,@R0       ;Source is internal RAM
0017: 0500         R            INC BASE        ;Update pointer of table
0019: 120000       R            CALL SENDBYTE   ;Send byte to IIC bus
001C: 0502         R            INC IIC_CNT     ;Update byte counter
001E: 8026                      JMP EXIT
```

```
                        ;
                        ;
                        ;Program to receive byte from IIC bus
0020:                   RECEIVE:
0020: E502        R             MOV A,IIC_CNT    ;Test if last byte is to be
                                                 ;received
0022: 04                        INC A
0023: 04                        INC A
0024: B50105      R             CJNE A,NR_BYTES,PROC_RD
0027: 7448                      MOV A,#01001000B;Last byte to be received.
                                                 ;Disable ACK
0029: 120000      R             CALL SENDCONTR   ;Write control word to
                                                 ;PCD8584
002C: 120000      R     PROC_RD:CALL READBYTE    ;Read I2C byte
002F: FC                        MOV R4,A         ;Save accu
                        ;If RECEIVE is entered after the transmission of
                        ;START+address then the result of READBYTE is not
                        ;relevant. READBYTE is used to start the generation
                        ;of the clock pulses for the next byte to read.
                        ;This situation occurs when IIC_CNT is 0
0030: E4                        CLR A            ;Test IIC_CNT
0031: B50202      R             CJNE A,IIC_CNT,SAVE
0034: 8006                      JMP END_TEST     ;START is send. No relevant
                                                 ;data in data reg. of 8584
0036: A800        R     SAVE:   MOV R0,BASE
0038: EC                        MOV A,R4         ;Destination is internal RAM
0039: F6                        MOV @R0,A
003A: 0500        R             INC BASE
003C: 0502        R     END_TEST:INC IIC_CNT    ;Test if all bytes are
                                                ;received
003E: E501        R             MOV A,NR_BYTES
0040: B50203      R             CJNE A,IIC_CNT,EXIT
0043: 120000      R             CALL STOP        ;All bytes received
                        ;
0046: D0D0              EXIT:   POP PSW          ;Restore PSW and accu
0048: D0E0                      POP ACC
004A: 32                        RETI
                        ;
004B:                           END
```

```
ASM51   TSW   ASSEMBLER    Send a string of bytes to the PCF8577 on OM1016

LOC     OBJ          LINE  SOURCE

                           $TITLE (Send a string of bytes to the PCF8577 on
                                   OM1016)
                           $PAGELENGTH(40)
                           ;
                           ;This program is an example to transmit bytes via
                           ;PCD8584
                           ;to the I2C-bus
                           ;
                                   PUBLIC   SLAVE_ADR,I2C_CLOCK,PCD8584
                                   EXTRN    CODE(I2C_INIT,INT0_SRV,START)
                                   EXTRN    BIT(I2C_END,DIR)
                                   EXTRN    DATA(BASE,NR_BYTES,IIC_CNT,SLAVE)
                           ;
                           ;
                           ;Define used segments
                           USER     SEGMENT CODE     ;Segment for user program
                           RAMTAB   SEGMENT DATA     ;Segment for table in
                                                     ;internal RAM
                           RAMVAR   SEGMENT DATA     ;Segment for RAM variables
                                                     ;in RAM
                           ;
                           ;
----                               RSEG     RAMVAR
0000:           R          STACK:  DS 20             ;Reserve stack area
                           ;
                           ;
----                               CSEG AT 00H
0000: 020000    R                  JMP MAIN          ;Reset vector
                           ;
                           ;
----                               CSEG AT 03H
0003: 020000    R                  JMP INT0_SRV      ;I2C interrupt vector
                                                     ;(INT0/)
                           ;
                           ;
----                               RSEG USER
                           ;Define I2C clock, own slave address and PCD8584
                           ;hardware address
0055                       SLAVE_ADR EQU 55H         ;Own slave address is 55H
001C                       I2C_CLOCK EQU 00011100B ;12.00MHz/90kHz
0000                       PCD8584   EQU 0000H       ;PCD8584 address with A0=0
                           ;0000: 7581FF    R    37  MAIN:    MOV SP,#STACK-1 ;Initialise stack pointer
                           ;Initialise 8031 interrupt registers for I2C
                           ;interrupt
0003: D2A8                         SETB EX0          ;Enable interrupt INT0/
0005: D2AF                         SETB EA           ;Set global enable
0007: D2B8                         SETB PX0          ;Priority level '1'
0009: D288                         SETB IT0          ;INT0/ on falling edge
                           ;
                           ;Initialise PCD8584
000B: 120000    R                  CALL I2C_INIT
                           ;
                           ;Make a table in RAM with data to be transmitted.
000E: 120021    R                  CALL MAKE_TAB
                           ;
                           ;Set variables to control PCD8584
```

```
0011: D200      R        SETB DIR          ;DIR='transmission'
0013: 750000    R        MOV BASE,#TABLE ;Start address of I2C-data
0016: 750005    R        MOV NR_BYTES,#05H ;5 bytes must be
                                           ;transferred
0019: 750074    R        MOV SLAVE,#01110100B ;Slave address PCF8577
                                           ; + WR/
001C: 120000    R        CALL START        ;Start I2C transmission
                  ;
                  ;
001F: 80FE        LOOP:  JMP LOOP          ;Endless loop when program
                                           ;is finished
                  ;
                  ;
0021:             MAKE_TAB:
0021: 7800      R        MOV R0,#TABLE     ;Make data ready for I2C
                                           ;transmission
0023: 7600               MOV @R0,#00       ;Controlword PCF8577
0025: 08                 INC R0
0026: 76FC               MOV @R0,#0FCH     ;'0'
0028: 08                 INC R0
0029: 7660               MOV @R0,#60H      ;'1'
002B: 08                 INC R0
002C: 76DA               MOV @R0,#0DAH     ;'2'
002E: 08                 INC R0
002F: 76F2               MOV @R0,#0F2H     ;'3'
0031: 22                 RET
                  ;
                  ;
----                     RSEG RAMTAB
0000:           R TABLE: DS 10             ;Reserve space in internal
                                           ;data RAM
                                           ;for I2C data to transmit
                  ;
                  ;
000A:                    END
```

```
ASM51   TSW   ASSEMBLER    Receive 2 bytes from the PCF8574P on OM1016

LOC    OBJ            LINE   SOURCE

                             $TITLE (Receive 2 bytes from the PCF8574P on OM1016)
                             $PAGELENGTH(40)
                             ;
                             ;This program is an example to receive bytes via
                             ;PCD8584
                             ;from the I2C-bus
                             ;
                                     PUBLIC  SLAVE_ADR,I2C_CLOCK,PCD8584
                                     EXTRN   CODE(I2C_INIT,INT0_SRV,START)
                                     EXTRN   BIT(I2C_END,DIR)
                                     EXTRN   DATA(BASE,NR_BYTES,IIC_CNT,SLAVE)
                             ;
                             ;
                             ;Define used segments
                             USER    SEGMENT CODE    ;Segment for user program
                             RAMTAB  SEGMENT DATA    ;Segment for table in
                                                     ;internal RAM
                             RAMVAR  SEGMENT DATA    ;Segment for RAM variables
                                                     ;in RAM
                             ;
                             ;
----                                 RSEG    RAMVAR
0000:             R          STACK:  DS 20           ;Reserve stack area
                             ;
                             ;
----                                 CSEG AT 00H
0000: 020000      R                  JMP MAIN        ;Reset vector
                             ;
                             ;
----                                 CSEG AT 03H
0003: 020000      R                  JMP INT0_SRV    ;I2C interrupt vector
                                                     ;(INT0/)
                             ;
                             ;
----                                 RSEG USER
                             ;Define I2C clock, own slave address and PCD8584
                             ;hardware address
0055                         SLAVE_ADR EQU 55H       ;Own slave address is 55H
001C                         I2C_CLOCK EQU 00011100B ;12.00MHz/90kHz
0000                         PCD8584   EQU 0000H     ;PCD8584 address with A0=0
                             ;0000: 7581FF   R    37  MAIN:   MOV SP,#STACK-1 ;Initialise stack pointer
                             ;Initialise 8031 interrupt registers for I2C
                             ;interrupt
0003: D2A8                           SETB EX0        ;Enable interrupt INT0/
0005: D2AF                           SETB EA         ;Set global enable
0007: D2B8                           SETB PX0        ;Priority level '1'
0009: D288                           SETB IT0        ;INT0/ on falling edge
                             ;
                             ;Initialise PCD8584
000B: 120000      R                  CALL I2C_INIT
                             ;
                             ;Set variables to control PCD8584
000E: C200        R                  CLR  DIR        ;DIR='receive'
0010: 750000      R                  MOV BASE,#TABLE ;Start address of I2C-data
0013: 750002      R                  MOV NR_BYTES,#02H ;2 bytes must be received
0016: 75004F      R                  MOV SLAVE,#01001111B ;Slave address PCF8574
                                                     ; + RD
```

```
0019: 120000   R          CALL START     ;Start I2C transmission
                  ;
                  ;
001C: 80FE        LOOP:   JMP LOOP       ;Endless loop when program
                                         ;is finished
                  ;
                  ;
----                      RSEG RAMTAB
0000:          R  TABLE:  DS 10          ;Reserve space in internal
                                         ;data RAM
                                         ;for received I2C data
                  ;
                  ;
000A:                     END
```

```
ASM51  TSW  ASSEMBLER   Demo program for PCD8584 I2C-routines

LOC    OBJ          LINE  SOURCE

                       1  $TITLE (Demo program for PCD8584 I2C-routines)
                       2  $PAGELENGTH(40)
                       3  ;Program displays on the LCD display  the time (with
                          ;PCF8583). Dots on LCD display blink every second.
                       5  ;On the LED display the values of the successive
                          ;analog input channels are shown.
                       7  ;Program reads analog channels of PCF8591P.
                       8  ;Channel number and channel value are displayed
                          ;successively.
                       9  ;Values are displayed on LCD and LED display on I2C
                          ;demo board.
                      10  ;
                      11          PUBLIC    SLAVE_ADR,I2C_CLOCK,PCD8584
                      12          EXTRN     CODE(I2C_INIT,INT0_SRV,START)
                      13          EXTRN     BIT(I2C_END,DIR)
                      14          EXTRN     DATA(BASE,NR_BYTES,IIC_CNT,SLAVE)
                      15  ;
                      16  ;
                      17  ;Define used segments
                      18  USER    SEGMENT  CODE    ;Segment for user program
                      19  RAMTAB  SEGMENT  DATA    ;Segment for table in
                                                   ;internal RAM
                      20  RAMVAR  SEGMENT  DATA    ;Segment for variables
                      21  ;
----                  22          RSEG RAMVAR
0000:          R      23  STACK:  DS 20            ;Stack area (20 bytes)
0014:                 24  PREVIOUS: DS 1           ;Store for previous seconds
0015:                 25  CHANNEL:DS 1             ;Channel number to be
                                                   ;sampled
0016:                 26  AN_VAL: DS 1             ;Analog value sampled
                                                   ;channel
0017:                 27  CONVAL: DS 3             ;Converted BCD value sampled
                                                   ;channel
                      28  ;
----                  29          CSEG AT 00H
0000: 020000   R      30          LJMP MAIN        ;Reset vector
                      31  ;
----                  32          CSEG AT 03H      ;INT0/
0003: 020000   R      33          LJMP INT0_SRV    ;Vector I2C-interrupt
                      34  ;
                      35  ;
----                  36          RSEG USER37  ;Define I2C clock, own slave address and address for
                          ;main processor
0055                  38  SLAVE_ADR EQU 55H       ;Own slaveaddress is 55h
001C                  39  I2C_CLOCK EQU 00011100B ;12.00MHz/90kHz
0000                  40  PCD8584   EQU 0000H     ;Address of PCD8584. This
                                                   ;must be an EVEN number!!
                      41  ;Define addresses of I2C peripherals
00A3                  42  PCF8583R  EQU 10100011B ;Address PCF8583 with Read
                                                   ;active
00A2                  43  PCF8583W  EQU 10100010B ;Address PCF8583 with Write
                                                   ;active
009F                  44  PCF8591R  EQU 10011111B ;Address PCF8591 with Read
                                                   ;active
009E                  45  PCF8591W  EQU 10011110B ;Address PCF8591 with Write
                                                   ;active
```

```
ASM51   TSW   ASSEMBLER   Demo program for PCD8584 I2C-routines

LOC   OBJ           SOURCE

0074                PCF8577W  EQU 01110100B ;Address PCF8577 with Write
                                            ;active
0076                SAA1064W  EQU 01110110B ;Address SAA1064 with Write
                                            ;active
                    ;
0000: 7581FF   R    MAIN:    MOV SP,#STACK-1 ;Define stack pointer
                    ;Initialise 80C31 interruptregisters for I2C
                    ;interrupt (INT0/)
0003: D2A8                   SETB EX0        ;Enable interrupt INT0/
0005: D2AF                   SETB EA         ;Set global enable
0007: D2B8                   SETB PX0        ;Priority level is '1'
0009: D288                   SETB IT0        ;INT0/ on falling edge
                    ;Initialise PCD8584
000B: 120000   R             CALL I2C_INIT
                    ;
000E: 751500   R             MOV CHANNEL,#00 ;Set AD-channel
                    ;
                    ;Time must be read from PCD8583.
                    ;First write word address and control register of
                    ;PCD8583.
0011: D200     R             SETB DIR        ;DIR='transmission'
0013: 750000   R             MOV BASE,#TABLE ;Start address I2C data
0016: 750002   R             MOV NR_BYTES,#02H ;Send 2 bytes
0019: 7500A2   R             MOV SLAVE,#PCF8583W
001C: E4                     CLR A
001D: F500     R             MOV TABLE,A     ;Data to be sent (word
                                             ;address).
001F: F501     R             MOV TABLE+1,A   ;      "         (control
                                             ;byte)
0021: 120000   R             CALL START      ;Start transmission.
0024: 3000FD   R    FIN_1:   JNB I2C_END,FIN_1 ;Wait till transmission
                                             ;finished
                    ;Send word address before reading time
0027: D200     R    REPEAT:  SETB DIR        ;'transmission
0029: 750000   R             MOV BASE,#TABLE ;I2C data
002C: 7500A2   R             MOV SLAVE,#PCF8583W
002F: 7401                   MOV A,#01
0031: F500     R             MOV NR_BYTES,A  ;Send 1 byte
0033: F500     R             MOV TABLE,A     ;Data to be sent is '1'
0035: 120000   R             CALL START      ;Start I2C transmission
0038: 3000FD   R    FIN_2:   JNB I2C_END,FIN_2 ;Wait till transmission
                                             ;finished
                    ;
                    ;Time can now be read from PCD8583. Data read is
                    ;hundredths of sec's, sec's, min's and hr's
003B: C200     R             CLR DIR         ;DIR='receive'
003D: 750000   R             MOV BASE,#TABLE ;I2C table
0040: 750004   R             MOV NR_BYTES,#04; 4 bytes to receive
0043: 7500A3   R             MOV SLAVE,#PCF8583R
0046: 120000   R             CALL START      ;Start I2C reception
0049: 3000FD   R    FIN_3:   JNB I2C_END,FIN_3 ;Wait till finished
                    ;
                    ;Transfer data to R2...R5
004C: 7800     R             MOV R0,#TABLE   ;Set pointers
004E: 7902                   MOV R1,#02H     ;Pointer R2
0050: E6            TRANSFER:MOV A,@R0
```

```
ASM51  TSW  ASSEMBLER   Demo program for PCD8584 I2C-routines

LOC    OBJ          LINE  SOURCE

0051: F7             94          MOV @R1,A
0052: 08             95          INC R0
0053: 09             96          INC R1
0054: D500F9    R    97          DJNZ NR_BYTES,TRANSFER
0057: ED             98          MOV A,R5        ;Mask of hour counter
0058: 543F           99          ANL A,#3FH
005A: FD            100          MOV R5,A
                    101  ;
                    102  ;Data must now be displayed on LCD display.
                    103  ;First minutes and hours (in R4 and R5) must be
                    104  ;converted from BCD to LCD segment data.The segment
                         ;data
                    105  ;will be transferred to TABLE. R0 is pointer to
                         ;table
005B: 7800      R   106          MOV R0,#TABLE
005D: 7600          107          MOV @R0,#00H    ;Control word for PCF8577
005F: 08            108          INC R0 0060: 120080    R    109          CALL CONV
                    110  ;
                    111  ;Switch on dp between hours and minutes
0063: 430301    R   112          ORL TABLE+3,#01H
                    113  ;If lsb of seconds is '0' then switch on dp.
0066: EB            114          MOV A,R3        ;Get seconds
0067: 13            115          RRC A           ;lsb in carry
0068: 4003          116          JC PROCEED
006A: 430101    R   117          ORL TABLE+1,#01H;switch on dp
                    118  ;
                    119  ;Now the time (hours,minutes) can be displayed on
                         ;the LCD
006D:               120  PROCEED:
006D: D200      R   121          SETB DIR        ;Direction 'transmit'
006F: 750000    R   122          MOV BASE,#TABLE
0072: 750005    R   123          MOV NR_BYTES,#05H
0075: 750074    R   124          MOV SLAVE,#PCF8577W
0078: 120000    R   125          CALL START      ;Start transmission
                    126  ;
007B: 3000FD    R   127  FIN_4:  JNB I2C_END,FIN_4
007E: 8026          128          JMP ADCON       ;Proceed with AD-conversion
                                                 ;part
                    129  ;
                    130 ;*****************************************************************
                    131  ;Routines used by clock part of demo
                    132  ;
                    133  ;CONV converts hour and minute data to LCD data and
                         ;stores
                    134  ;it in TABLE.
0080: 90009C    R   135  CONV:   MOV DPTR,#LCD_TAB ;Base for LCD segment
                                                 ;table
0083: ED            136          MOV A,R5        ;Hours to accu
0084: C4            137          SWAP A          ;Swap nibbles
0085: 120096    R   138          CALL LCD_DATA   ;Convert 10's hours to LCD
                                                 ;data in table
0088: ED            139          MOV A,R5        ;Get hours
0089: 120096    R   140          CALL LCD_DATA
008C: EC            141          MOV A,R4        ;Get minutes
008D: C4            142          SWAP A
008E: 120096    R   143          CALL LCD_DATA   ;Convert 10's minutes
```

```
ASM51  TSW  ASSEMBLER   Demo program for PCD8584 I2C-routines

LOC   OBJ           LINE  SOURCE

0091: EC             144          MOV A,R4
0092: 120096   R     145          CALL LCD_DATA   ;Convert minutes
0095: 22             146          RET
                     147  ;
                     148  ;LCD_DATA gets data from segment table and stores it
                          ;in TABLE
0096: 540F           149  LCD_DATA:ANL A,#0FH     ;Mask off LS-nibble
0098: 93             150          MOVC A,@A+DPTR  ;Get LCD segment data
0099: F6             151          MOV @R0,A       ;Save data in table
009A: 08             152          INC R0
009B: 22             153          RET
                     154  ;
                     155  ;LCD_TAB is conversion table for LCD
009C:                156  LCD_TAB:
009C: FC60DA         157          DB 0FCH,60H,0DAH; '0','1','2'
009F: F266B6         158          DB 0F2H,66H,0B6H; '3','4','5'
00A2: 3EE0FE         159          DB 3EH,0E0H,0FEH; '6','7','8'
00A5: E6             160          DB 0E6H         ; '9'
                     161  ;
                     162  ;***********************************************************************
                     163  ;
                     164  ;
                     165  ;These part of the program reads an analog
                          ;input-channel.
                     166  ;Displaying is done on the LED-display
                     167  ;On odd-seconds the channel number will be
                          ;displayed.
                     168  ;On even-seconds the analog value of this channel is
                          ;displayed
                     169  ;Then the next channel is displayed.
                     170  ;
00A6: EB             171  ADCON:  MOV A,R3        ;Get seconds
00A7: 13             172          RRC A           ;lsb to carry
00A8: 503C           173          JNC NEW_MEAS    ;Even seconds; do a
                                                  ;measurement on the current
                                                  ;channel
                     174  ;
                     175  ;Display and/or update channel
00AA: 33             176          RLC A           ;Restore accu
00AB: B51402   R     177          CJNE A,PREVIOUS,NEW_CH ;If new seconds,
                                                  ;update channel number
00AE: 800A           178          JMP DISP_CH
00B0: 0515     R     179  NEW_CH: INC CHANNEL
00B2: E515     R     180          MOV A,CHANNEL   ;If channel=4 then
                                                  ;channel:=0
00B4: B40403         181          CJNE A,#04,DISP_CH
00B7: 751500   R     182          MOV CHANNEL,#00
00BA: 8B14     R     183  DISP_CH:MOV PREVIOUS,R3 ;Update previous seconds
00BC: E515     R     184          MOV A,CHANNEL   ;Get segment value of
                                                  ;channel
00BE: 900193   R     185          MOV DPTR,#LED_TAB
00C1: 93             186          MOVC A,@A+DPTR
                     187  ;
00C2: 7800     R     188          MOV R0,#TABLE   ;Fill table with I2C data
```

```
ASM51   TSW   ASSEMBLER    Demo program for PCD8584 I2C-routines

LOC    OBJ           LINE   SOURCE

00C4: 7600                          MOV @R0,#00       ;SAA1064 instruction byte
00C6: 08                            INC R0
00C7: 7677                          MOV @R0,#77H      ;SAA1064 control byte
00C9: 08                            INC R0
00CA: F6                            MOV @R0,A         ;Channel number
00CB: E4                            CLR A
00CC: 08                            INC R0
00CD: F6                            MOV @R0,A         ;Second digit
00CE: 08                            INC R0
00CF: F6                            MOV @R0,A         ;Third digit
00D0: 08                            INC R0
00D1: F6                            MOV @R0,A         ;Fourth byte
                             ;
00D2: D200         R                SETB DIR          ;I2C transmission of channel
                                                      ;number
00D4: 750000       R                MOV BASE,#TABLE
00D7: 750006       R                MOV NR_BYTES,#06H
00DA: 750076       R                MOV SLAVE,#SAA1064W
00DD: 120000       R                CALL START
                             ;
00E0: 3000FD       R         FIN_5: JNB I2C_END,FIN_5
00E3: 020027       R                JMP REPEAT        ; Repeat clock and AD cycle
                                                      ; again
                             ;
                             ;
                             ;Measure and display the value of an AD-channel
00E6: 120108       R         NEW_MEAS: CALL AD_VAL    ;Do measurement
                             ;Wait till values are available
00E9: 3000FD       R         FIN_6: JNB I2C_END,FIN_6
                             ;Relevant byte in TABLE+1. Transfer to AN_VAL
00EC: 7801         R                MOV R0,#TABLE+1
00EE: 8616         R                MOV AN_VAL,@R0
00F0: E516         R                MOV A,AN_VAL      ;Channel value in accu for
                                                      ;conversion
                             ;AN_VAL is converted to BCD value of the measured
                             ;voltage.
                             ;Input value for CONVERT in accu
                             ;Address for MSByte in R1
00F2: 7917         R                MOV R1,#CONVAL
00F4: 120154       R                CALL CONVERT
                             ;Convert 3 bytes of CONVAL to LED-segments
00F7: 900193       R                MOV DPTR,#LED_TAB ;Base of segment table
00FA: 7817         R                MOV R0,#CONVAL
00FC: 12018A       R                CALL SEG_LOOP
                             ;Display value of channel to LED display
00FF: 12012C       R                CALL LED_DISP
0102: 3000FD       R         FIN_8: JNB I2C_END,FIN_8 ;Wait till I2C
                                                      ;transmission is ended
0105: 020027       R                JMP REPEAT        ;Repeat clock and AD cycle
                             ;
                            ;*****************************************************************
                             ;Routines used for AD converter.
                             ;
                             ;AIN reads an analog values from channel denoted by
                             ;CHANNEL.
```

```
ASM51  TSW  ASSEMBLER   Demo program for PCD8584 I2C-routines

LOC    OBJ                SOURCE

                          ;Send controlbyte:
0108: D200      R         AD_VAL: SETB DIR          ;I2C transmission
010A: 7800      R                 MOV R0,#TABLE     ;Define control word
010C: A615      R                 MOV @R0,CHANNEL
010E: 750000    R                 MOV BASE,#TABLE ;Set base at table
0111: 750001    R                 MOV NR_BYTES,#01H ;Number of bytes to be
                                                    ;send
0114: 75009E    R                 MOV SLAVE,#PCF8591W ;Slave address PCF8591
0117: 120000    R                 CALL START        ;Start transmission of
                                                    ;controlword
011A: 3000FD    R         FIN_7:  JNB I2C_END,FIN_7 ;Wait until tranmission is
                                                    ;finished
                          ;Read 2 data bytes from AD-converter
                          ;First data byte is from previous conversion and not
                          ;relevant
011D: C200      R                 CLR DIR           ;I2C reception
011F: 750000    R                 MOV BASE,#TABLE ;Bytes must be stored in
                                                    ;TABLE
0122: 750002    R                 MOV NR_BYTES,#02H; Receive 3 bytes
0125: 75009F    R                 MOV SLAVE,#PCF8591R ;Slave address PCF8591
0128: 120000    R                 CALL START
012B: 22                          RET
                          ;
                          ;LED_DISP displays the data of 3 bytes from address
                          ;CONVAL
012C:                     LED_DISP:
012C: 431780    R                 ORL CONVAL,#80H ;Set decimal point
012F: 7800      R                 MOV R0,#TABLE
0131: 7917      R                 MOV R1,#CONVAL
0133: 7600                        MOV @R0,#00       ;SAA1064 instruction byte
0135: 08                          INC R0
0136: 7677                        MOV @R0,#01110111B ;SAA1064 control byte
0138: 08                          INC R0
0139: 7600                        MOV @R0,#00       ;First LED digit
013B: 08                          INC R0
013C: 120185    R                 CALL GETBY        ;Second digit
013F: 120185    R                 CALL GETBY        ;Third digit
0142: 120185    R                 CALL GETBY        ;Fourth digit
0145: D200      R                 SETB DIR          ;I2C transmission
0147: 750000    R                 MOV BASE,#TABLE
014A: 750006    R                 MOV NR_BYTES,#06
014D: 750076    R                 MOV SLAVE,#01110110B
0150: 120000    R                 CALL START        ;Start I2C transmission
0153: 22                          RET
                          ;
                          ;CONVERT calculates the voltage of the analog value.
                          ;Analog value must be in accu
                          ;BCD result (3 bytes) is stored from address stored
                          ;in R1
                          ;Calculation: AN_VAL*(5/256)
0154: 75F005              CONVERT:MOV B,#05
0157: A4                          MUL AB
                          ;b2..b0 of reg. B : 2E+2..2E0
                          ;b7..b0 of accu   : 2E-1..2E-8
0158: A7F0                        MOV @R1,B         ;Store MSB (10E0-units)
015A: 09                          INC R1
```

```
ASM51  TSW  ASSEMBLER   Demo program for PCD8584 I2C-routines

LOC    OBJ           LINE  SOURCE

015B: 7700                          MOV @R1,#00      ;Calculate 10E-1 unit
                                                     ;(10E-1 is 19h)
015D: B41C02               TEN_CH:  CJNE A,#19H+03H,V1  ;Check if accu <= 0.11
0160: 8002                          JMP TENS         ;accu=0.11; update tens
0162: 4006                 V1:      JC NX_CON        ;accu<0.11; update hundreds
0164: C3                   TENS:    CLR C            ;Calculate new value
0165: 9419                          SUBB A,#19H
0167: 07                            INC @R1          ;Update BCD byte
0168: 80F3                          JMP TEN_CH
                           ;Correction may be neccessary. With 8 bits '0.1' is
                           ;in fact 0.0976.
                           ;A digit of '0A' may appear. Correct this by
                           ;decrementing the digit.
                           ;The intermediate result result must be corrected
                           ;with 10*(0.1-0.0976)
                           ;This is 06H
016A: B70A03               NX_CON:  CJNE @R1,#0AH,PROC_CON ; If digit is '0A'
                                                     ;then correct
016D: 17                            DEC @R1
016E: 2419                          ADD A,#19H
0170: 09                   PROC_CON:INC R1
0171: 7700                          MOV @R1,#00      ;Calculate 10E-2 units
0173: B40302               HUND:    CJNE A,#03H,V2   ;Check if accu <= 10E-2
0176: 8002                          JMP HUNS         ;accu=10E-2; update hundreds
0178: 4006                 V2:      JC FINISH        ;accu<10E-2; conversion
                                                     ;finished
017A: C3                   HUNS:    CLR C            ;Calculate new value
017B: 9403                          SUBB A,#03H
017D: 07                            INC @R1          ;Update BCD byte
017E: 80F3                          JMP HUND
0180: B70A01               FINISH:  CJNE @R1,#0AH,FIN ;Check if result is '0A'.
                                                     ;Then correct.
0183: 17                            DEC @R1
0184: 22                   FIN:     RET
                           ;
                           ;CALLBY tranfers byte from @R1 to @R0
0185: E7                   GETBY:   MOV A,@R1
0186: F6                            MOV @R0,A
0187: 08                            INC R0
0188: 09                            INC R1
0189: 22                            RET
                           ;
                           ;SEG_LOOP converts 3 values to segment values.
                           ;R0 contains address of source and destination
                           ;DPTR contains base of table
018A: 7903                 SEG_LOOP: MOV R1,#03     ;Loop counter
018C: E6                   INLOOP:  MOV A,@R0     ;Get value to be displayed
018D: 93                            MOVC A,@A+DPTR  ;Get segment value from
                                                    ;table
018E: F6                            MOV @R0,A       ;Store segment data
018F: 08                            INC R0
0190: D9FA                          DJNZ R1,INLOOP
0192: 22                            RET
                           ;
                           ;
```

```
ASM51  TSW  ASSEMBLER   Demo program for PCD8584 I2C-routines

LOC    OBJ            LINE  SOURCE

                      335  ;LED_TAB is conversion table for BCD to LED segments
0193:                 336  LED_TAB:
0193: 7D483E          337          DB 7DH,48H,3EH  ; '0','1','2'
0196: 6E4B67          338          DB 6EH,4BH,67H  ; '3','4','5'
0199: 734C7F          339          DB 73H,4CH,7FH  ; '6','7','8'
019C: 4F              340          DB 4FH          ; '9'
                      341  ;
                      342 ;****************************************************************
                      343  ;
----                  344          RSEG RAMTAB
0000:          R      345  TABLE:  DS 10
                      346  ;
000A:                 347          END
```

Section 3
Functional Index of Products

CONTENTS

Digital-to-analog conversion

Digital video processing

A to D converter selection guide

Part	Resolution	Power	Convert Rate	Clamp	AGC	No. of Inputs	Outputs	Comments	Applications
TDA8703	8 bits	290mW	40MHz	No	No	One	Binary and Twos comp.	TTL compatible	General Purpose
TDA8704	8 bits	365mW	50MHz	No	No	One	Binary and Twos comp.	–40, +85 temp range	Automotive/High temp. general purpose
TDA8706	6 bits (X3)	300mW	20MHz	Yes	No	Three multi-plexed inputs	Binary TTL	Internal Reference	YUV, PIP applications
TDA8708A/B	8 bits	365mW	32MHz	Yes	Yes	One of three	Binary and Twos comp.	Peak white is 248 for 8708A 255 for 8708B	Video decoding, frame grabbers
TDA8709A	8 bits	380mW	32MHz	Yes	No	One of three	Binary and Twos comp.	Ext. voltage gain control	Video signal and chroma proc.
TDA8714	8 bits	325mW	75MHz	No	No	One	Binary and Twos comp.	7.6 effective bits at 4.43MHz	High speed applications: radar, medical, physics, etc.
TDA8715	8 bits	325mW	50MHz	No	No	One	Binary ECL with overflow	Comp. ECL clock	High speed ECL applications
TDA8716	8 bits	780mW	100MHz	No	No	One	Binary ECL with overflow	Comp. ECL clock	Very high speed ECL applications
TDA8718	8 bits	1140mW	600MHz	No	No	One	Binary ECL with overflow	Comp. ECL clock	Ultra high speed ECL applications
TDA8755	8 bits	565mW	20MHz	Yes	No	Three multi-plexed inputs	Binary and Twos comp.	4:1:1 data encoder	YUV video conversion

D to A converter selection guide

Part	Resolution	Power	Convert Rate (Max.)	Number of DACs/Package	Comments	Applications
TDA8702	8 bits	250mW	30MHz	One	75 Ω load	General purpose
TDA8712	8 bits	250mW	50MHz	One	75 Ω load	High speed general purpose
TDA8771	8 bits	175mW	35MHz	Three	3 volts p/p out into 1K Ω	Triple output general purpose
TDA8772	8 bits	260mW 310mW	35MHz 85MHz	Three	75 Ω load, separate blanking and sync inputs	RGB or YUV video with sync on signal
TDA7169	9 bits		35MHz	Three	75 Ω load	RGB or YUV video
TDA7165	8 bits		30MHz	Three	Digital YUV to analog YUV converter with aperture and color improvement	Interfaces to RGB monitor drivers
TDA9065	8 bits		30MHz	Three	Digital YUV to analog YUV converter with aperture improvement	Interfaces to RGB monitor drivers

I^2C-bus controller PCD8584

GENERAL DESCRIPTION

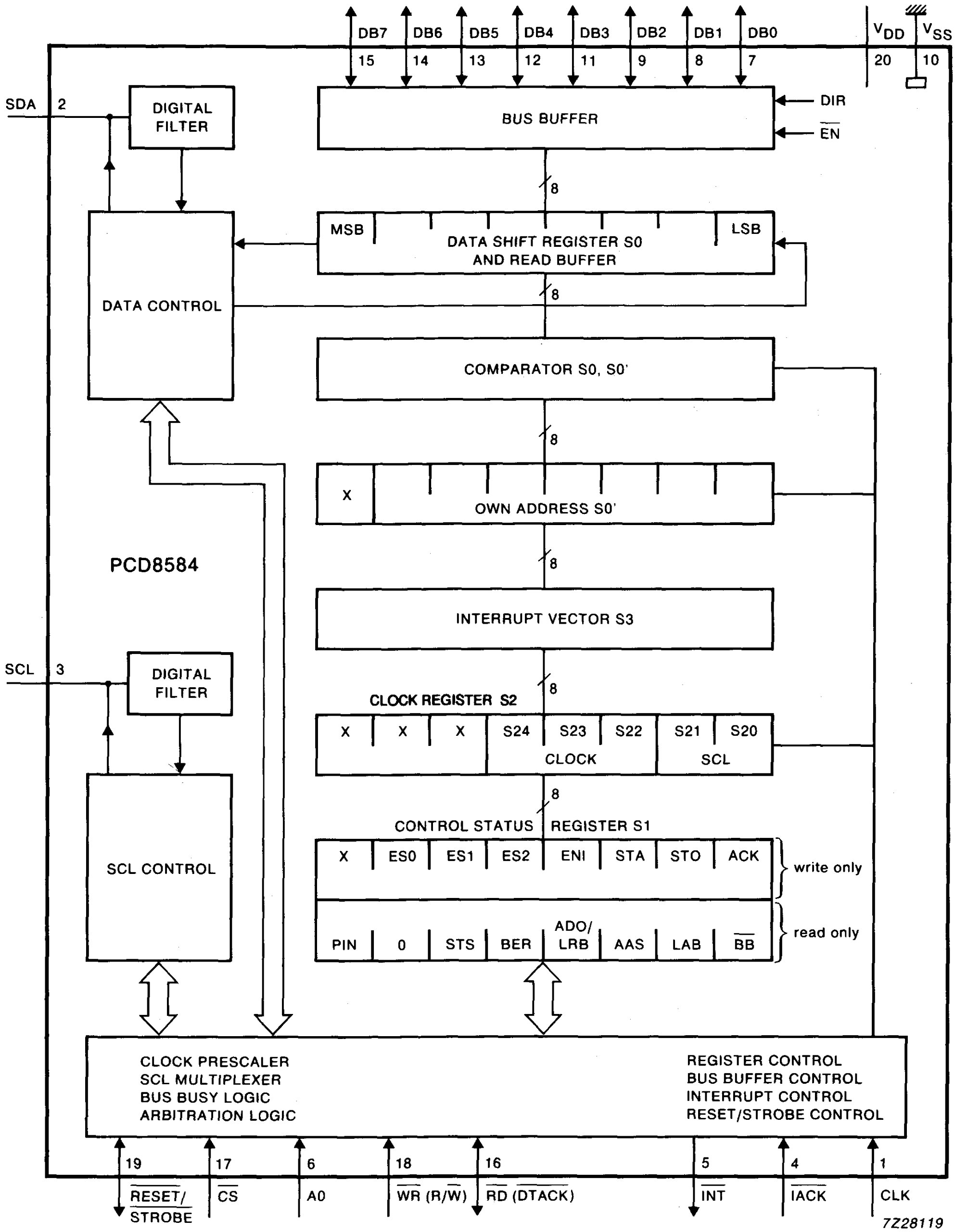
The PCD8584 is an integrated circuit designed in CMOS technology which serves as an interface between most standard parallel-bus microcontrollers/processors and the serial I^2C-bus. The PCD8584 provides both master and slave functions. Communication with the I^2C-bus is carried out on a byte-wise basis using interrupt or polled handshake. It controls all the I^2C-bus specific sequencing, protocol, arbitration and timing. The PCD8584 allows parallel-bus systems to communicate bidirectionally with the I^2C-bus.

Features

- Parallel-bus/I^2C-bus protocol converter
- Compatible with most parallel-bus processors including MAB8049, MAB8051, SCN68000 and Z80
- Automatic selection of bus interface
- Programmable interrupt vector
- Multi-master capability
- I^2C-bus monitor mode
- Long-distance mode
- Operating supply voltage 4.5 to 5.5 V
- Operating temperature range –20 to + 70 °C

PACKAGE OUTLINES

PCD8584P: 20-lead DIL; plastic (SOT146).
PCD8584T: 20-lead mini-pack; plastic (SO20; SOT163A).



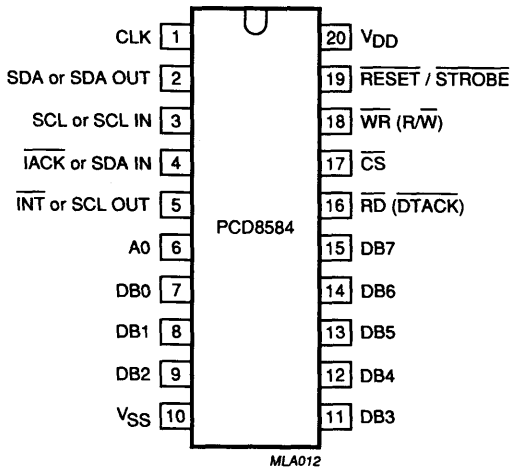
Where:

( ) indicate the SCN68000 pin name designations.

X = don't care.

Fig.1 Block diagram.

PINNING



Where:

( ) indicate the SCN68000 pin name designations.

Fig.2 Pinning diagram.

Pin functions

pin	mnemonic	function	description
1	CLK	I	Clock input from microprocessor clock generator (internal pull-up).
2	SDA or SDA OUT	I/O	I^2C-bus serial data input/output (open-drain). Serial data output in long-distance mode.
3	SCL or SCL IN	I/O	I^2C-bus serial clock input/output (open-drain). Serial clock input in long-distance mode.
4	$\overline{IACK}$ or SDA IN	I	Interrupt acknowledge input (internal pull-up); when this signal is asserted the interrupt vector in Register S2 will be available at the bus port if the ENI flag is set. Serial data input in long-distance mode.
5	$\overline{INT}$ or SCL OUT	O	Interrupt output (open-drain); this signal is enabled by the ENI flag in Register S1. It is asserted, when the PIN flag is reset. (PIN is reset after one byte is transmitted or received over the I^2C-bus). Serial clock output in long-distance mode.
6	A0	I	Register select input (internal pull-up); this input selects between the control/status register and the other registers. Logic 1 selects Register S1, logic 0 selects one of the other registers depending on bits loaded in ES0, ES1 and ES2 of Register S1.
7	DB0	I/O	
8	DB1	I/O	Bidirectional 8-bit bus port.
9	DB2	I/O	
10	V_{SS}		Negative supply voltage.

Pin functions (continued)

pin	mnemonic	function	description
11	DB3	I/O	
12	DB4	I/O	
13	DB5	I/O	Bidirectional 8-bit bus port.
14	DB6	I/O	
15	DB7	I/O	
16	$\overline{\text{RD}}$ ($\overline{\text{DTACK}}$)	I (O)	$\overline{\text{RD}}$ is the read control input for MAB8049, MAB8051 or Z80-type processors. $\overline{\text{DTACK}}$ is the data transfer control output for 68000-type processors (open-drain).
17	$\overline{\text{CS}}$	I	Chip select input (internal pull-up).
18	$\overline{\text{WR}}$ (R/$\overline{\text{W}}$)	I	$\overline{\text{WR}}$ is the write control input for MAB8048, MAB8051 or Z80-type processors (internal pull-up). R/$\overline{\text{W}}$ control input for 68000-type processors.
19	$\overline{\text{RESET}}$/ $\overline{\text{STROBE}}$	I/O	Reset input (open-drain); this input forces the I^{2}C-bus controller into a predefined state; all flags are reset, except PIN, which is set. Also functions as strobe output.
20	V_{DD}		Positive supply voltage.

FUNCTIONAL DESCRIPTION

General

The PCD8584 acts as an interface device between standard high-speed parallel buses and the serial I^{2}C-bus. On the I^{2}C-bus, it can act either as master or slave. Bidirectional data transfer between the I^{2}C-bus and the parallel-bus microprocessor is carried out on a byte-wise basis, using either an interrupt or polled handshake. Interface to either 80XX-type (e.g. MAB8048, MAB8051, Z80) or 68000-type buses is possible. Selection of bus type is automatically performed (see **Interface mode control**).

Table 1 Control signals utilized by the PCD8584 for processor interfacing

type	R/$\overline{\text{W}}$	$\overline{\text{WR}}$	$\overline{\text{RD}}$	$\overline{\text{DTACK}}$	$\overline{\text{IACK}}$
MAB8049/51	NO	YES	YES	NO	NO
SCC68000	YES	NO	NO	YES	YES
Z80	NO	YES	YES	NO	YES

The structure of the PCD8584 is similar to that of the I^{2}C-bus interface section of the MAB8400-series of microcontrollers, but with a modified control structure. The PCD8584 has five internal register locations. Three of these (Own Address register S0′, Clock register S2 and Interrupt Vector S3) are used for initialization of the PCD8584. Normally they are only written once directly after resetting of the PCD8584. The remaining two registers function as double registers (Data Buffer/Shift register S0, and Control/Status register S1) which are used during actual data transmission/reception. By using these double registers, which are separately write and read accessible, overhead for register access is reduced. S0 is a combination of a shift register and data buffer. S0 performs all serial-to-parallel interfacing with the I^{2}C-bus. S1 contains I^{2}C-bus status information required for bus access and/or monitoring.

FUNCTIONAL DESCRIPTION (continued)

Interface mode control (IMC)

Selection of either an 80XX-mode or 68000-mode interface is achieved by detection of the $\overline{WR}$ - $\overline{CS}$ signal sequence. The concept takes advantage of the fact that the write control input is common for both types of interfaces. The chip is non-initialized after reset until register S0′ is accessed. An 80XX-type interface is default. If a HIGH-to-LOW transition of $\overline{WR}$ (R/$\overline{W}$) is detected while $\overline{CS}$ is HIGH, the 68000-type interface mode is selected and the $\overline{DTACK}$ output is enabled.

Note:

The very first access to the PCD8584 after a reset must be a write access to register S0′ in order to set the appropriate interface mode.

Set-up Registers S0′, S2 and S3

Own Address Register S0′

When addressed as a slave, this register is loaded with the 7-bit I²C-bus address to which the PCD8584 is to respond. The "Addressed As Slave" (AAS) bit in Status register S1 is set when this address is received. Programming of this register is accomplished via the parallel-bus when A0 is LOW, with the appropriate bit combinations set in Control Status register S1 (S1 is written when A0 is HIGH). Bit combinations for accessing all registers are given in Tables 4 and 5. After reset S0′ has default address '00' Hex.

Clock Register S2

Register S2 provides control over chip clock frequency and SCL clock frequency. S20 and S21 provide a selection of 4 different I²C-bus SCL frequencies which are shown in Table 2.

Table 2 Register S2 selection of SCL frequency

bit		SCL approximate frequency (kHz)
S21	S20	
0	0	90
0	1	45
1	0	11
1	1	1.5

S22, S23 and S24 are used for control of the internal clock prescaler. Due to the possibility of varying microprocessor clock signals, the prescaler can be programmed to adapt to 5 different clock rates, thus providing a constant internal clock. This is required to provide a stable time base for the SCL generator and the digital filters associated with the I²C-bus signals SCL and SDA. Selection for adaption to external clock rates is shown in Table 3. After reset, a clock frequency of 12 MHz is the default value.

Table 3 Register S2 selection of clock frequency

bit S24	S23	S22	clock frequency (MHz)
0	X	X	3
1	0	0	4.43
1	0	1	6
1	1	0	8
1	1	1	12

Where: X = don't care.

Interrupt Vector S3

The interrupt vector register provides an 8-bit user-programmable vector for vectored-interrupt microprocessors. The vector is sent to the bus port when an interrupt acknowledge signal is asserted and the ENI (enable interrupt) flag is set. Default vector values are as follows:

- Vector is '00' Hex in 80XX-mode
- Vector is '0F' Hex in 68000-mode

On reset the PCD8584 is in the 80XX mode, thus the default interrupt vector becomes '00' Hex.

Interface Registers S0 and S1

Data Shift Register S0

S0 acts as serial shift register interfacing to the I²C-bus. S0 is a combination of a shift register and a data buffer; parallel data is always written to the shift register and read from the data buffer. Serial data is shifted in/out the shift register, and in receiver mode the data from the shift register is copied to the data buffer during the acknowledge phase (see also PIN bit). All read and write operations to the I²C-bus are done via this register.

Control/Status Register S1

Register S1 is accessed by a HIGH signal on register select input A0. To facilitate communication between the microcontroller/processor and the I²C-bus, register S1 has separate read and write functions for all bit positions.

The write-only section has been split into 2 parts:

- The ESO (Enable Serial Output) enables or disables the serial output. When ESO is LOW, register access for initialization is possible. When ESO is HIGH, serial communication is enabled; communication with serial shift register S0 is enabled and the S1 bus status bits are made available for reading. Select control bits ES1 and ES2 control selection of other registers for initialization and control of normal operation. After these bits are programmed for access to the desired register (see Tables 4 and 5), the register is selected by a logic LOW level on register select pin A0.

Note:

With ESO = 0, bits ENI, STA, STO and ACK of S1 can be read for test purposes.

FUNCTIONAL DESCRIPTION (continued)

Control/Status Register S1 (continued)

Table 4 Register access control; ESO = logic 0 (serial interface off)

A0	ES1	ES1	$\overline{IACK}$	operation
H	X	X	X	READ/WRITE CONTROL REGISTER (S1) STATUS (S1) not available
L	0	0	X	READ/WRITE OWN ADDRESS (S0')
L	0	1	X	READ/WRITE INTERRUPT VECTOR (S3)
L	1	0	X	READ/WRITE CLOCK REGISTER (S2)

Table 5 Register access control; ES0 = logic 1 (serial interface on)

A0	ES1	ES2	$\overline{IACK}$	operation
H	X	X	H	WRITE CONTROL REGISTER (S1)
H	X	X	H	READ STATUS REGISTER (S1)
L	X	0	H	READ/WRITE DATA (S0)
L	X	1	H	READ/WRITE INTERRUPT VECTOR (S3)
X	0	X	L	READ INTERRUPT VECTOR (acknowledge cycle)
X	1	X	L	long-distance mode

Instruction control bits ENI, STA, STO and ACK are used in normal operation to enable the interrupt output ($\overline{INT}$), generate I^2C-bus START and STOP conditions, and program the acknowledge response, respectively. These possibilities are shown in Table 6.

Table 6 Instruction table for serial bus control

STA	STO	present mode	function	operation
1	0	SLV/REC	START	transmit START + address remain MST/TRM if R/$\overline{W}$= logic 0; go to MST/REC if R/$\overline{W}$ = logic 1
1	0	MST/TRM	REPEAT START	same as for SLV/REC
0	1	MST/REC MST/TRM	STOP READ STOP WRITE	transmit stop go to SLV/REC mode (see note 1)
1	1	MST	DATA CHAINING	send STOP, START and address after last master frame without STOP sent (see note 2)
0	0	ANY	NOP	no operation (see note 3)

Notes to Table 6

1. In master-receiver mode, the last byte must be terminated with ACK bit HIGH ("negative-acknowledge"; see I²C-bus specification).
2. If both STA and STO are set HIGH simultaneously in master mode, a STOP condition followed by a START condition + address will be generated. This allows "chaining" of transmissions without relinquishing bus control.
3. All other STA, STO mode combinations not mentioned in Table 6 are NOPs.

The instruction bits are defined as follows:

- STA, STO: These bits control the generation of the I²C-bus START condition + transmission of slave address and R/$\overline{W}$ bit, generation of repeated START condition, and generation of the STOP condition.
- ENI: This bit enables the external interrupt output $\overline{INT}$, which is generated when the PIN bit is reset.
- ACK: This bit must be set normally to a '1'. This causes the I²C-bus controller to send an acknowledge automatically after each byte (this occurs during the ninth clock pulse). The bit must be reset when the I²C-bus controller is operating in master/receiver mode, and requires no further data to be sent from the slave transmitter. This causes a negative acknowledge on the I²C-bus, which halts further transmission from the slave device.

FUNCTIONAL DESCRIPTION (continued)

I²C-bus status information

The read-only section consists of I²C-bus status information. The functions are as follows:

- STS: When in slave-receiver mode, this flag is asserted when an externally generated STOP condition is detected (only used in slave-receiver mode).
- BER: Bus error. A misplaced START or STOP condition has been detected.
- LRB/AD0: Last Received Bit/Address 0 "General Call" Bit. This dual function status bit holds the value of the last received bit over the I²C-bus when AAS = 0. Normally this will be the value of the slave acknowledge; thus checking for slave acknowledgment is done via testing of the LRB bit. When AAS = 1 ("Address As Slave"), the I²C-bus controller has been addressed as a slave and this bit will be set if the slave address received was the "general call" address, or if it was the I²C-bus controller's slave address.
- AAS: "Addressed As Slave" bit. When acting as slave-receiver, this flag is set when an incoming address over the I²C-bus matches the value in Own Address register S0', or if the I²C-bus "general call" address ("00" Hex) has been received.
- LAB: "Lost Arbitration" bit. This bit is set when, in multmaster operation, arbitration is lost to another master on the I²C-bus.
- $\overline{BB}$: "Bus Busy" bit. This is read-only flag indicating when the I²C-bus is in use. A zero indicated that the bus is busy, and access is not possible. This bit is set/reset by STOP/START conditions.

PIN bit

The PIN bit "Pending Interrupt Not" is a read-only flag which is used to synchronize serial communication. Each time a serial data transmission is initiated (by setting the STA bit in the same register), the PIN will be set automatically. After successful transmission of one byte (9 clock pulses, including acknowledge), this bit will be automatically reset indicating a complete byte transmission. When the ENI bit is also set, the PIN flag triggers an external interrupt via the $\overline{INT}$ output when PIN is reset. When in receiver mode, the PIN bit is also reset on completion of each received byte. In polled applications, the PIN bit is tested to determine when a serial transmission has been completed. During register transfers the I²C-bus controller Data Register S0 and its internal shift register (not accessible directly), the I²C-bus controller will delay serial transmission by holding the SCL line LOW until the PIN bit becomes set. In receiver mode, the PIN bit is automatically set when the data register S0 is read. When the PIN bit becomes set all status bits will be reset, with exception of $\overline{BB}$.

Multi-master operations

To avoid conflict between data and repeated START and STOP operations, multi-master systems have some limitations:

- Transmissions requiring a repeated START condition must have identical format among all potential masters for both read and write operations
- For correct arbitration masters may only attempt to send data simultaneously to the same location, if they use the same formats (i.e. number of data bytes, location of the repeated START, etc.). If this condition is designed not to occur, differing formats may be used.

Reset A low-level pulse on the $\overline{RESET}$ input forces the I²C-bus controller into a well-defined state. All flags are reset (zero state), except the PIN flag, which is set. The $\overline{RESET}$ pin is also used for the $\overline{STROBE}$ output signal. Both functions are separated on-chip by a digital filter. The reset input signal has to be sufficiently long (minimum 30 clock cycles) to pass through the filter. The $\overline{STROBE}$ output signal is sufficiently short (8 clock cycles) to be blocked by the filter. For more detailed information on the Strobe function see **Special function modes.**

FUNCTIONAL DESCRIPTION (continued)

Comparison to the MAB8400 I²C-bus interface

The structure of the PCD8584 is similar to that of the MAB8400 series of microcontrollers, but with a modified control structure. Access to all I²C-bus control and status registers is done via the parallel-bus port in conjunction with register select input A0, and control bits ESO, ES1 and ES2. The main differences are highlighted below.

Deleted functions

The following functions are not available in the PCD8584:

- Always selected (ALS flag)
- Access to the bit counter (BC0 to BC2)
- Full SCL frequency selection (2 bits instead of 5 bits)
- The non-acknowledge mode (ACK flag)
- Asymmetrical clock (ASC flag)

Added functions

The following functions either replace the deleted functions or are completely new:

- Chip clock prescaler
- Assert acknowledge bit (ACK flag)
- Register selection bits (ES1 and ES2 flags)
- Additional status flags
- Automatic interface control between 80XX and 68000-type microprocessors
- Programmable interrupt vector
- Strobe generator
- Bus monitor function
- Long-distance mode (non-I²C-bus mode; only for communication between remote parallel-bus processors)

Special function modes

Strobe

When the I²C-bus controller receives its own address (or the "00" Hex general call address) followed immediately by a STOP condition (i.e. no further data transmitted after the address), a strobe output signal is generated at the $\overline{RESET}/\overline{STROBE}$ pin (pin 19). The $\overline{STROBE}$ signal consists of a monostable output pulse (active LOW), eight clock cycles long (see Fig.10). It is generated after the STOP condition is received, preceded by the correct slave address. This output can be used as a bus access controller for multi-master parallel-bus systems (see Fig.14).

Long-distance mode

The long-distance mode provides a serial communication link between parallel processors using two or more I²C-bus controllers. This mode is selected by setting ES1 to logic 1 while the serial interface is enabled (ESO = 1). In this mode the I²C-bus protocol is transmitted over 4 unidirectional lines, SDA, OUT, SCL IN, SDA IN and SCL OUT (pins 2, 3, 4 and 5). These communication lines should be connected to the line drivers/receivers for long distance applications. Specification for long distance transmission is then given by the chosen standard. Control of bus frequency, data transmission etc. is the same as in normal I²C-bus mode. After reading or writing data to shift register S0, long-distance mode must be initialized by setting ESO and ES1 to logic 1. Because the interrupt output $\overline{INT}$ is not available in this operating mode, data reception must be polled.

Monitor mode

When the 7-bit Own Address register S0' is loaded with all zeros, the I²C-bus controller acts as a passive I²C monitor. The main features of the monitor mode are as follows:

- The controller is always selected
- The controller is always in the slave-receiver mode
- The controller never generates an acknowledge
- The controller never generates an interrupt request
- A pending interrupt condition does not force SCL LOW
- Received data is automatically transferred to the read buffer
- Bus traffic is monitored by the PIN bit, which is reset after the acknowledge bit has been transmitted and is set as soon as the first bit of the next byte is detected

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 20)	V_{DD}	−0.3	+ 7.0	V
Voltage range on any input*	V_I	−0.8	V_{DD} + 0.5	V
DC input current (any input)	$\pm I_I$	−	10	mA
DC output current (any output)	$\pm I_O$	−	10	mA
Total power dissipation	P_{tot}	−	300	mW
Power dissipation per output	P_O	−	50	mW
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

Note to the Ratings

Stresses above those listed in accordance with Absolute Maximum System may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 5 ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4.5	5.0	5.5	V
Supply current						
standby	note 1	I_{DD1}	−	−	2.5	μA
operating	note 2	I_{DD2}	−	−	1.5	mA
Inputs						
SCL, SDA						
Input voltage LOW	note 3	V_{IL1}	0	−	0.8	V
Input voltage HIGH	note 3	V_{IH1}	2.0	−	V_{DD}	V
Input voltage LOW	note 4	V_{IL2}	0	−	$0.3V_{DD}$	V
Input voltage HIGH	note 4	V_{IH2}	$0.7V_{DD}$	−	V_{DD}	V
Resistance to V_{DD}	T_{amb} = 25 °C; note 5	R_i	25	−	100	kΩ
Outputs						
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3.0	−	−	mA
Output current HIGH	V_{OH} = 2.4 V; note 6	$-I_{OH}$	2.4	−	−	mA
Leakage current	note 7	$\pm I_{LO}$	−	−	1	μA

Notes to the characteristics

1. 22 kΩ pull-ups on D0 to D7; 10 kΩ pull-ups on SDA, SCL, $\overline{RD}$; $\overline{RESET}$ tied to V_{SS}; remaining pins open-circuit.
2. Same as note 1, but CLK waveform with 50% duty factor at 12 MHz.
3. CLK, $\overline{IACK}$, A0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{RESET}$, TTL level inputs.
4. SDA, SCL, D0 to D7, CMOS level inputs.
5. CLK, $\overline{IACK}$, A0, $\overline{CS}$, $\overline{WR}$.
6. D0 to D7.
7. D0 to D7 3-state, SDA, SCL, $\overline{INT}$, $\overline{RD}$, $\overline{RESET}$.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
I²C-bus timing					
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable bus spike width	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	µs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	µs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	µs
SCL LOW time	t_{LOW}	4.7	–	–	µs
SCL HIGH time	t_{HIGH}	4.0	–	–	µs
SCL and SDA rise time	t_r	–	–	1.0	µs
SCL and SDA fall time	t_f	–	–	0.3	µs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	µs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	µs

Parallel interface timing (see Figs 3 to 10)

All the timing limits are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
C_L = 100 pF, R_L = 1.5 kΩ (connected to V_{DD}) for open-drain and high-impedance outputs, where applicable (for measurement purposes only).

parameter	figure	symbol	min.	typ.	max.	unit
Clock rise time	3	t_r	–	–	6	ns
Clock fall time	3	t_f	–	–	6	ns
Input clock period (50% duty factor)	3	t_{CLK}	83	–	333	ns
$\overline{CS}$ set-up to $\overline{RD}$, $\overline{WR}$ LOW	4	t_{SU1}	30	–	–	ns
$\overline{CS}$ hold from $\overline{RD}$, $\overline{WR}$ HIGH	4	t_{HD1}	0	–	–	ns
A0 set-up to $\overline{RD}$, $\overline{WR}$ LOW	4	t_{SU2}	10	–	–	ns
A0 hold from $\overline{RD}$, $\overline{WR}$ HIGH	4	t_{HD2}	20	–	–	ns
$\overline{WR}$ pulse width	4	t_{W1}	230	–	–	ns
$\overline{RD}$ pulse width	4	t_{W2}	230	–	–	ns
Data set-up before $\overline{WR}$ HIGH	4	t_{SU3}	150	–	–	ns
Data valid after $\overline{RD}$ LOW	4	t_{VD}	–	110	180	ns
Data hold after $\overline{WR}$ HIGH	4	t_{HD3}	30	–	–	ns
Data bus floating after $\overline{RD}$ HIGH	4	t_{FL}	70	–	–	ns
A0 set-up to $\overline{CS}$ LOW	5 and 6	t_{SU4}	30	–	–	ns
R/$\overline{WR}$ set-up to $\overline{CS}$ LOW	5 and 6	t_{SU5}	30	–	–	ns
Data valid after $\overline{CS}$ LOW	5	t_{VD1}	–	110	180	ns
$\overline{DTACK}$ LOW after $\overline{CS}$ LOW	5 and 6	t_{d1}	–	$3t_{CLK}+75$	$3t_{CLK}+150$	ns
A0 hold from $\overline{CS}$ HIGH	5 and 6	t_{HD4}	0	–	–	ns
R/$\overline{WR}$ hold from $\overline{CS}$ HIGH	5 and 6	t_{HD5}	0	–	–	ns
Data hold after $\overline{CS}$ HIGH	5	t_{HD6}	160	–	–	ns
$\overline{DTACK}$ HIGH from $\overline{CS}$ HIGH	5 and 6	t_{d2}	–	100	120	ns
Data hold after $\overline{CS}$ HIGH	6	t_{HD7}	0	–	–	ns
Data set-up to $\overline{CS}$ LOW	6	t_{SU6}	0	–	–	ns
$\overline{INT}$ HIGH from $\overline{IACK}$ LOW	7 and 8	t_{d3}	–	130	180	ns
Data valid after $\overline{IACK}$ LOW	7 and 8	t_{VD2}	–	140	190	ns

Parallel interface timing (continued)

parameter	figure	symbol	min.	typ.	max.	unit
$\overline{IACK}$ pulse width	7 and 8	t_{W3}	230	–	–	ns
Data hold after $\overline{IACK}$ HIGH	7 and 8	t_{HD8}	100	–	–	ns
$\overline{DTACK}$ LOW from $\overline{IACK}$ LOW	8	t_{d4}	–	$3t_{CLK}+75$	$3t_{CLK}+150$	ns
$\overline{DTACK}$ HIGH from $\overline{IACK}$ HIGH	8	t_{d5}	–	120	140	ns
Reset pulse width	9	t_{W4}	$30t_{CLK}$	–	–	ns
Strobe pulse width	10	t_{W5}	$8t_{CLK}$	$8t_{CLK}+90$	–	ns

Notes to parallel interface timing

1. A minimum of 6 clock cycles must elapse between consecutive parallel-bus accesses when the I^2C-bus controller operates at 8 or 12 MHz. This may be reduced to 3 clock cycles for lower operating frequencies.
2. After reset the chip clock default is 12 MHz.

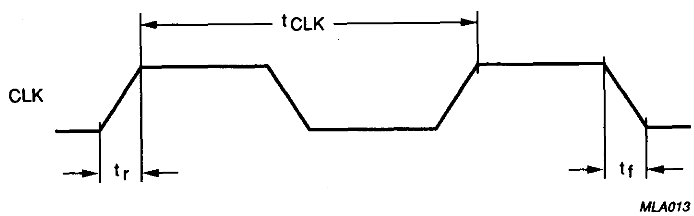
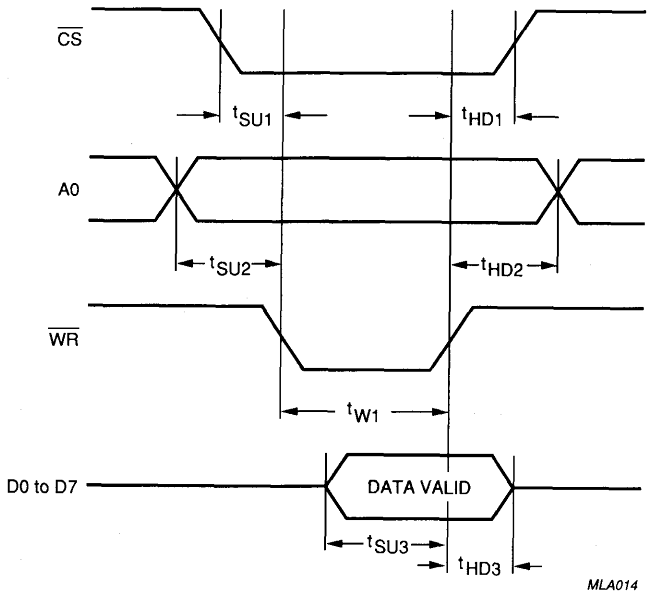
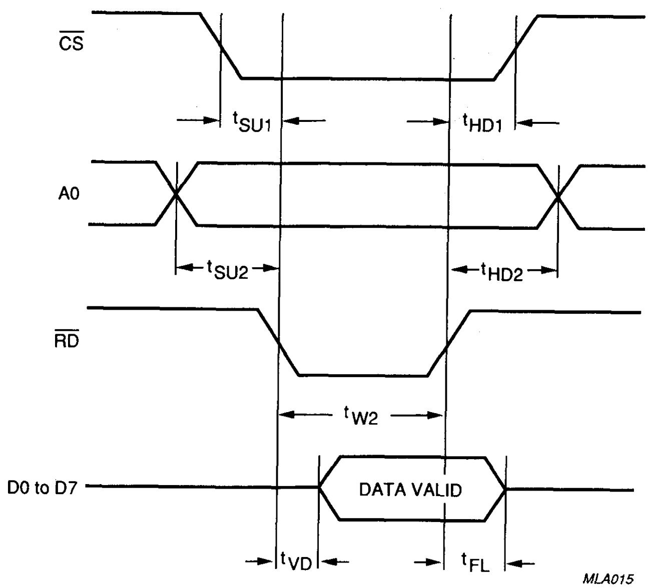


Fig.3 Clock input timing.

Timing diagrams



(a)



(b)

Fig. 4 Bus timing (80XX-mode); (a) write cycle, (b) read cycle.

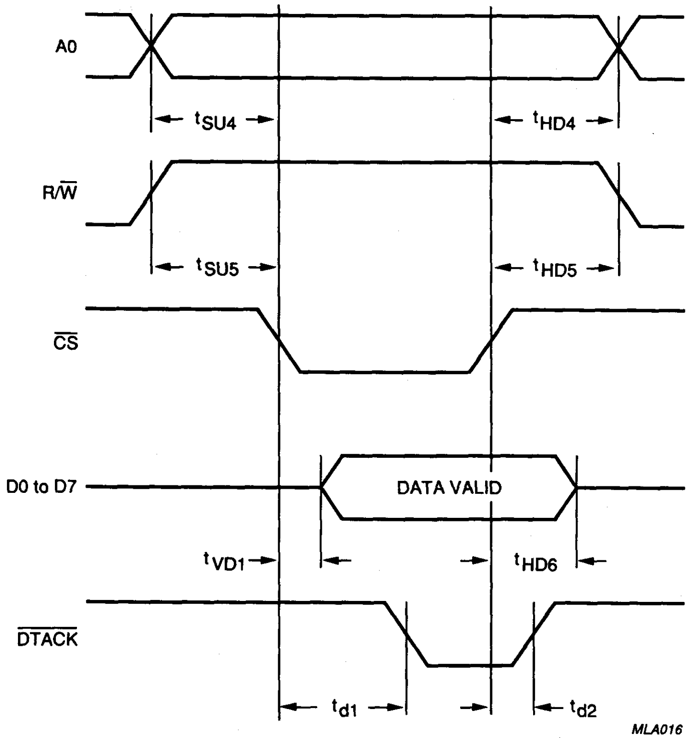


Fig.5 Bus timing; 68000-mode read cycle.

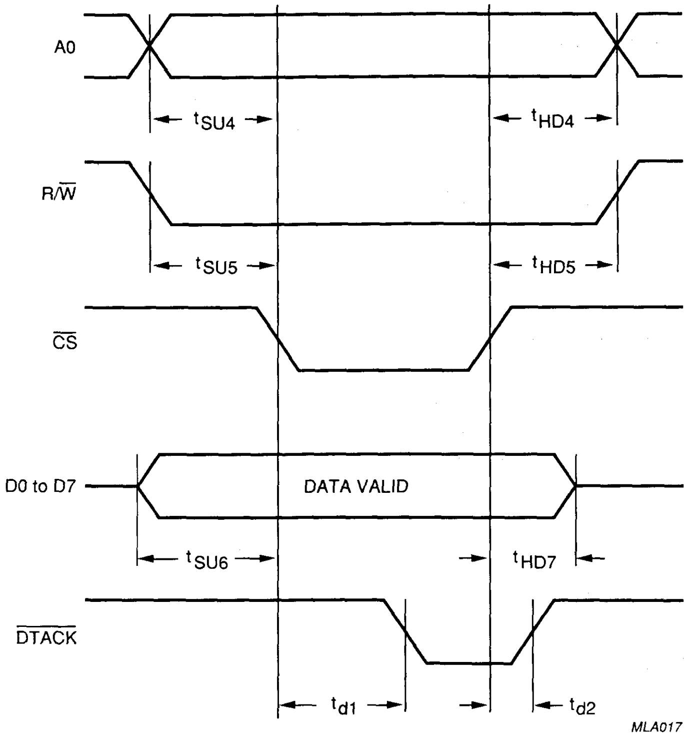


Fig.6 Bus timing; 68000-mode write cycle.

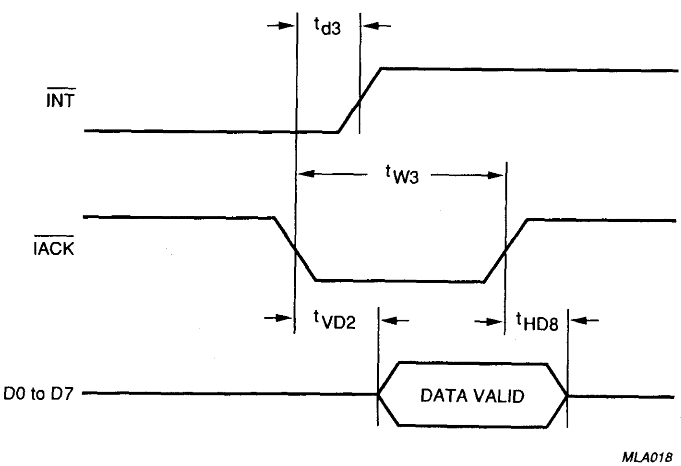


Fig.7 Interrupt timing; 80XX-mode.

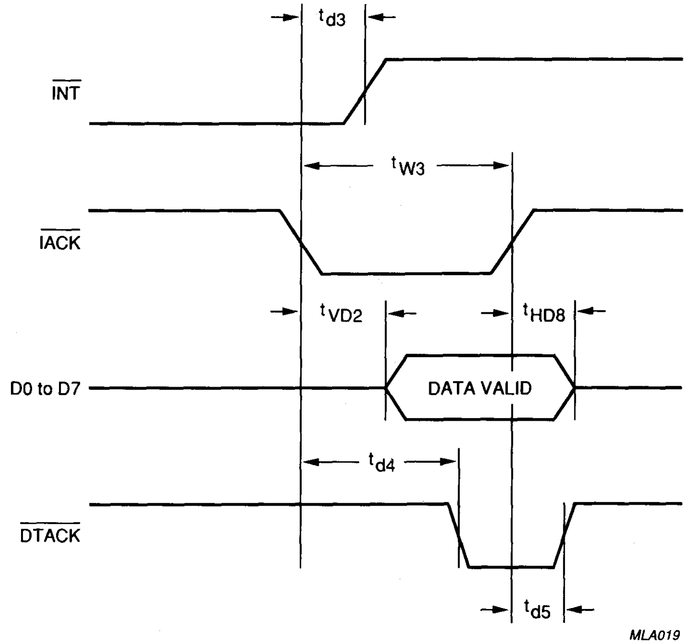


Fig.8 Interrupt timing; 68000-mode.

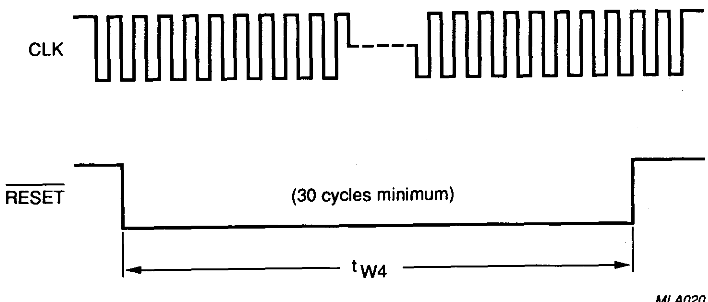


Fig.9 Reset timing.

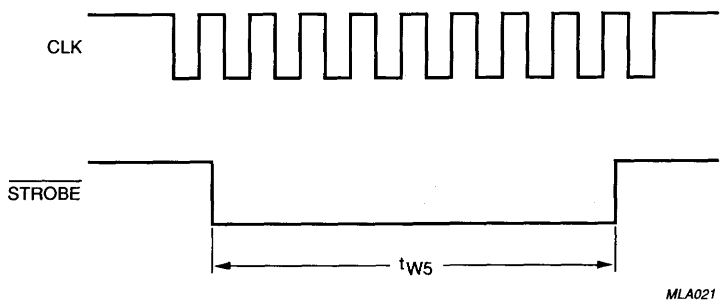


Fig.10 Strobe timing.

APPLICATION INFORMATION

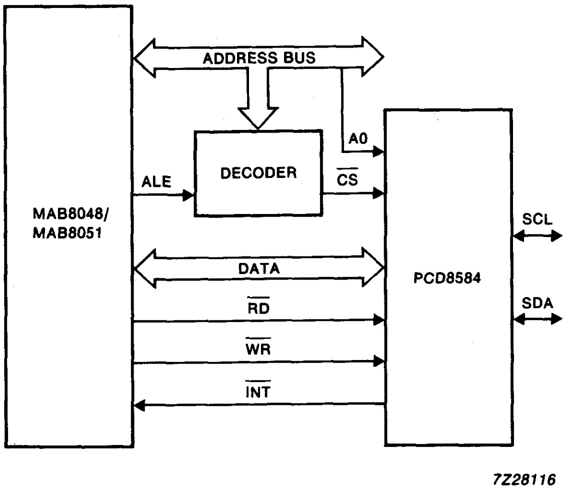


Fig.11 Application diagram using the MAB8048/MAB8051.

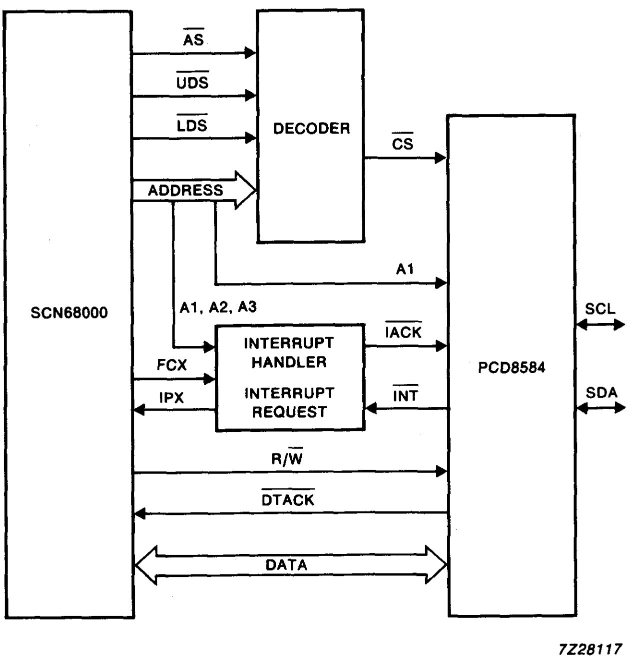


Fig.12 Application diagram using the SCN68000.

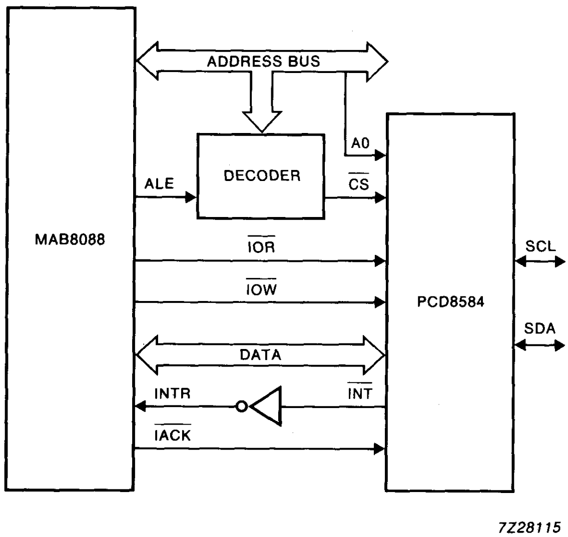


Fig.13 Application diagram using the 8088.

APPLICATION INFORMATION (continued)

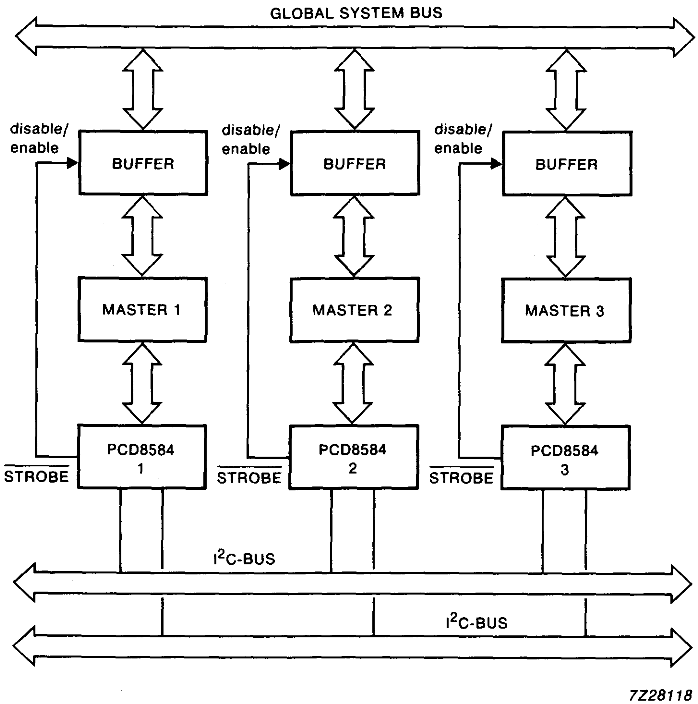


Fig.14 $\overline{\text{STROBE}}$ as bus access controller.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Remote 8-bit I/O expander for I²C-bus PCF8574/PCF8574A

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I²C).
It can also interface microcomputers without a serial interface to the I²C-bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I²C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I²C-bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig.9.

Features

- Operating supply voltage 2.5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I²C-bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

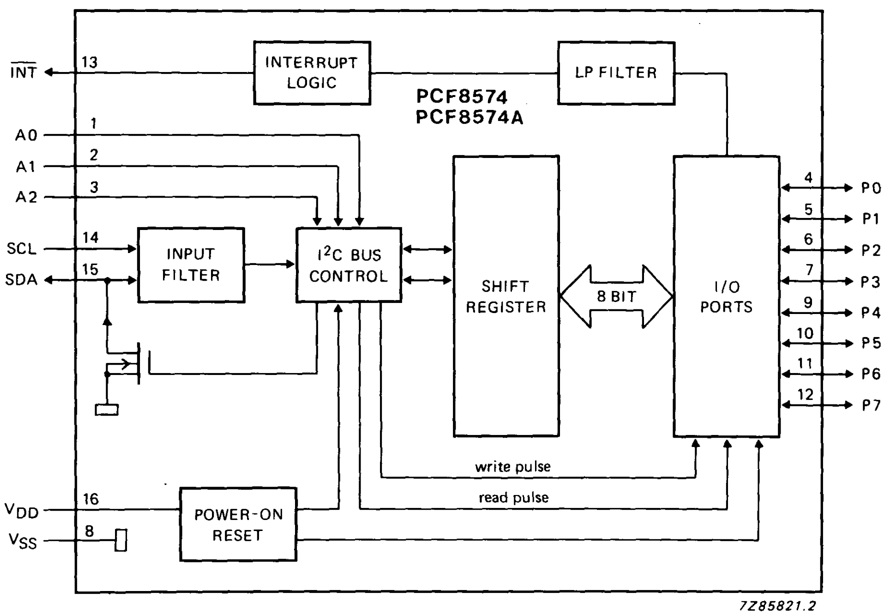


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

PINNING

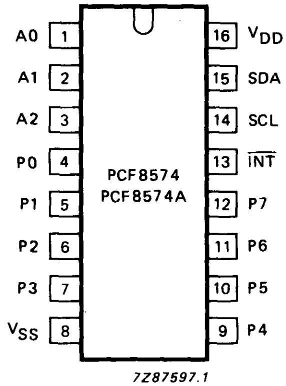


Fig.2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7	P0 to P3	8-bit quasi-bidirectional I/O port
9 to 12	P4 to P7	
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

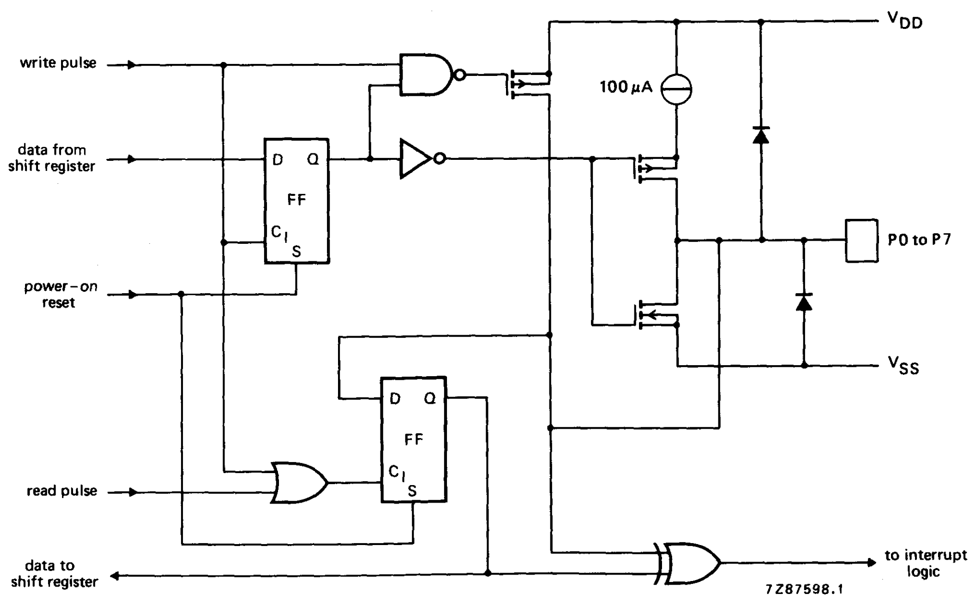


Fig.3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

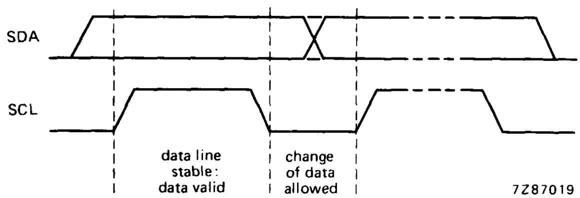


Fig.4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

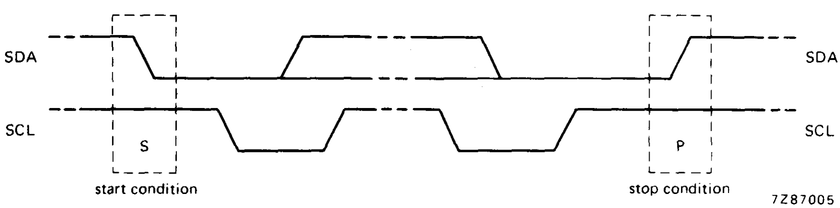


Fig.5 Definition of start and stop conditions.

CHARACTERISTICS OF THE I²C-BUS (continued)

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

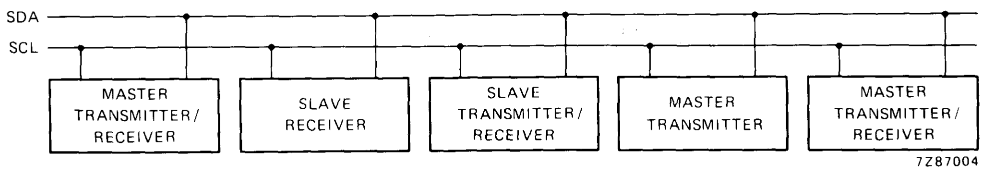


Fig.6 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

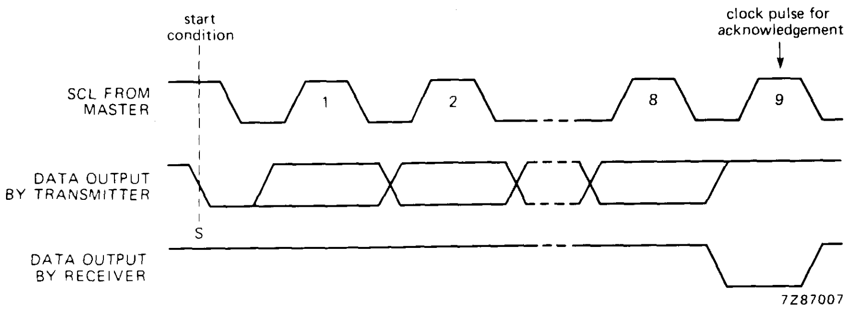


Fig.7 Acknowledgement on the I² C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

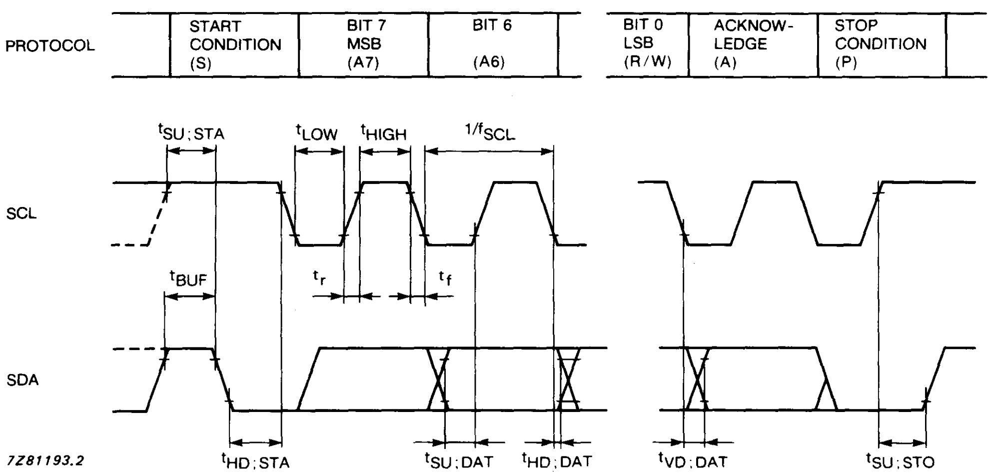


Fig.8 I²C-bus timing diagram.

FUNCTIONAL DESCRIPTION

Addressing (see Figs 9, 10 and 11)

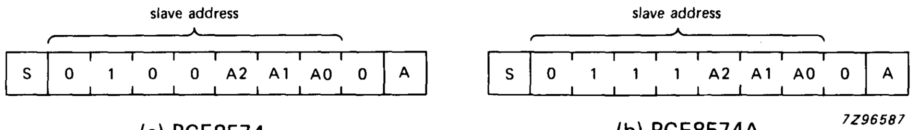


Fig.9 PCF8574 and PCF8574A slave addresses.

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

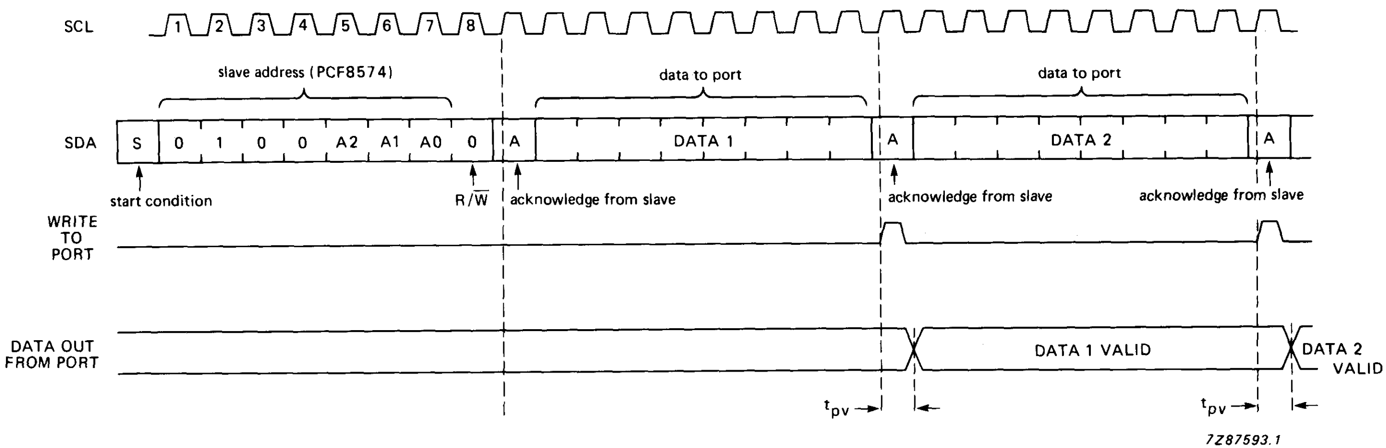


Fig.10 WRITE mode (output port).

Remote 8-bit I/O expander for I²C-bus

PCF8574/PCF8574A

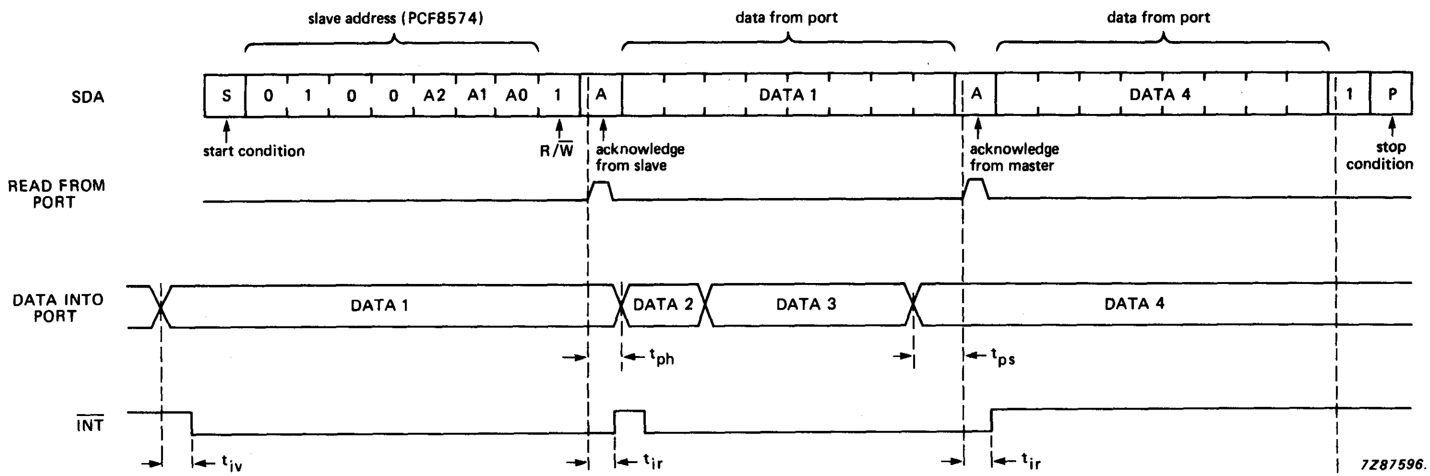


Fig.11 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 12 and 13)

The PCF8574/PCF8574A provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

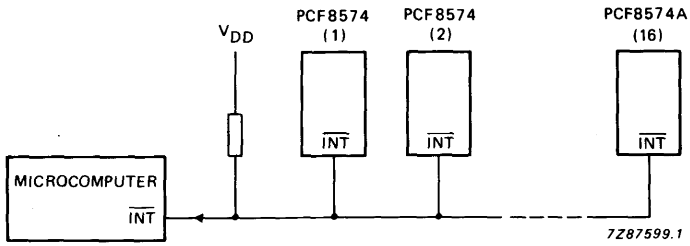


Fig.12 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.

Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.

Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit.

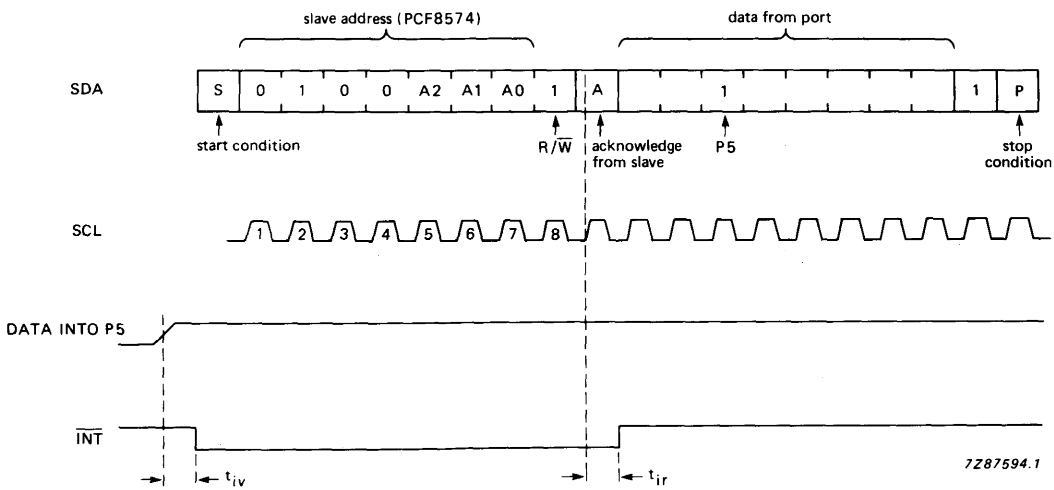


Fig.13 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig.14)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. At power-on the ports are HIGH. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The ports should be HIGH before being used as inputs.

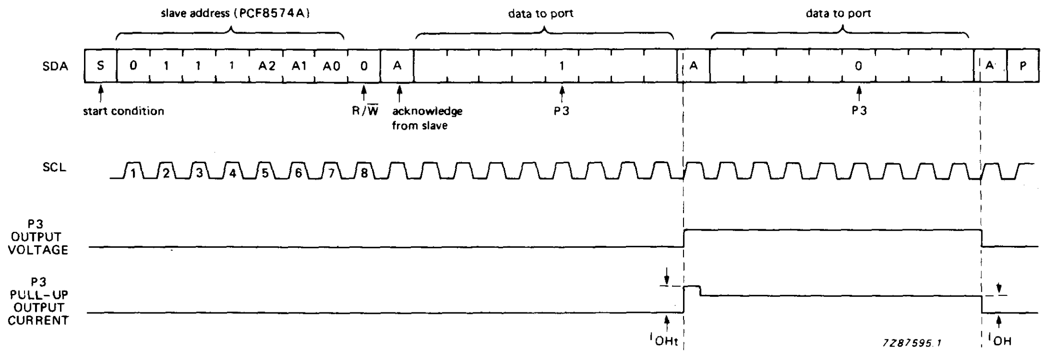


Fig.14 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+ 7.0	V
Input voltage range	V_I	V_{SS} −0.5	V_{DD} + 0.5	V
DC input current	$\pm I_I$	−	20	mA
DC output current	$\pm I_O$	−	25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; $\pm I_{SS}$	−	100	mA
Total power dissipation	P_{tot}	−	400	mW
Power dissipation per output	P_O	−	100	mW
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
Supply current	V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}					
operating	f_{SCL} = 100 kHz	I_{DD}	–	40	100	μA
standby		I_{DDO}	–	2.5	10	μA
Power-on reset level	note 1	V_{POR}	–	1.3	2.4	V
Input SCL; input/output SDA						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	$V_{DD} + 0.5$	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_{LI}\|$	–	–	1	μA
Input capacitance (SCL, SDA)	$V_I = V_{SS}$	C_I	–	–	7	pF
I/O ports						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	$V_{DD} + 0.5$	V
Maximum allowed input current through protection diode	$V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW	V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	25	–	mA
Output current HIGH	$V_{OH} = V_{SS}$	I_{OH}	30	–	300	μA
Transient pull-up current HIGH during acknowledge (see Fig.14)	$V_{OH} = V_{SS}$; V_{DD} = 2.5 V	$-I_{OHt}$	–	1	–	mA
Input/Output capacitance		$C_{I/O}$	–	–	10	pF
Port timing (see Figs 10 and 11)	$C_L = \leqslant 100$ pF					
Output data valid		t_{pv}	–	–	4	μs
Input data set-up		t_{ps}	0	–	–	μs
Input data hold		t_{ph}	4	–	–	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$						
Output current LOW	$V_{OL} = 0.4$ V	I_{OL}	1.6	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\lvert I_{LI} \rvert$	–	–	1	μA
$\overline{INT}$ timing (see Figs 11 and 13)	$C_L = \leqslant 100$ pF					
Input data valid		t_{iv}	–	–	4	μs
Reset delay		t_{ir}	–	–	4	μs
Select inputs A0, A1, A2						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	$V_{DD} + 0.5$	V
Input leakage current	pin at V_{DD} or V_{SS}	$\lvert I_{LI} \rvert$	–	–	250	nA

Note to the characteristics

1. The power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and sets all ports to logic 1 (with current source to V_{DD}).

Universal sync generator (USG) SAA1101

FEATURES

- Programmable to seven standards
- Additional outputs to simplify signal processing
- Can be synchronized to an external sync. signal
- Option to select the 524/624 line mode instead of the 525/625 line mode
- Lock from subcarrier to line frequency

GENERAL DESCRIPTION

The SAA1101 is a Universal Sync Generator (USG) and is designed for application in video sources such as cameras, film scanners, video generators and associated apparatus. The circuit can be considered as a successor to the SAA1043 sync generator and the SAA1044 subcarrier coupling IC.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range (pin 28)	4.5	5.5	V
I_{DD}	quiescent supply current	–	10	μA
f_{OSC}	clock oscillator frequency	–	24	MHz

ORDERING AND PACKAGE INFORMATION

EXTENDED	PACKAGE			
TYPE NUMBER	PINS	PIN POSITION	MATERIAL	CODE
SAA1101P	28	DIL	plastic	SOT117
SAA1101T	28	SO28	plastic	SOT136A

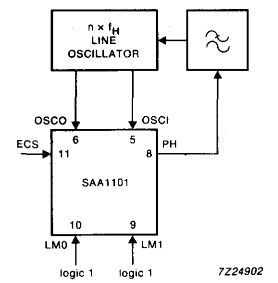


Fig.3(c) Fast sync lock, internal H_{ref}

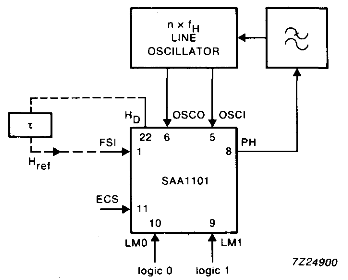


Fig.3(d) Slow sync lock, external H_{ref}

LOCK WITH HORIZONTAL AND VERTICAL SIGNALS

(slow lock modes only)

It is possible to use horizontal and vertical signals instead of composite sync signals. The connections in this situation are: the external horizontal signal is connected to the ECS input (pin 11) and the vertical signal to the RR input (pin 12). The HIGH time of the horizontal pulse must be less than 14.4 μs, otherwise it will be detected as being a vertical pulse and will corrupt the vertical slow lock system.

Selection of Clock Frequency

The clock frequency is selected using the CS0 and CS1 inputs as illustrated below.

CS0	CS1	FREQUENCY	625 LINES	525 LINES	UNITS
0	0	$160f_H$	2.5	2.517482	MHz
0	1	$320f_H$	5	5.034964	MHz
1	0	$960f_H$	15	15.104893	MHz
1	1	$1440f_H$	22.5	22.657340	MHz

Where the horizontal frequency, f_H = 15.625 kHz for 625 lines and 15.734264 kHz for 525 lines.

Lock modes

The USG offers four lock modes:

- Lock from the subcarrier
- Slow sync. lock, external H_{ref}
- Slow sync. lock, internal H_{ref}
- Fast sync. lock, internal H_{ref}

LOCK FROM SUBCARRIER

Lock from subcarrier to the line frequency for the above mentioned TV systems is given below; the horizontal frequency (f_H) = 15.625 kHz for 625 line systems and 15.734264 kHz for 525 line systems.

SECAM (1 and 2)	$282f_H$
PALN	$229.2516f_H$
NTSC (1 and 2)	$227.5f_H$
PALM	$227.25f_H$
PAL B/G	$283.7516f_H$

These relationships are obtained by the use of a phase locked loop and the internal programmed divider chain, see Fig. 3(a).

LOCK TO AN EXTERNAL SIGNAL SOURCE

The following methods can be used to lock to an external signal source:

1. Sync. lock slow; the line frequency is locked to an external signal. The line and frame information are extracted from the external sync. signal and used separately in the lock system. The line information is used in a phase-locked loop where external and internal line frequencies are compared by the same phase detector as is used for the subcarrier lock. The external frame information is compared with the internal frame in a slow lock system; mismatch of internal and external frames will result in the addition or suppression of one line depending on the direction of the fault. The maximum lock time for frame lock is 6.25 s, see Fig. 3(b).
2. Sync. lock fast. A fast lock of frames is possible with a frame reset which is extracted out of the incoming external sync. signal, see Fig. 3(c).
3. Sync. lock with external reference. Lock of an external sync. signal to the line frequency with an external line reference to make possible a shifted lock. The subcarrier input is, in this case, used as an external input for the horizontal reference, see Fig. 3(d).

SELECTION OF LOCK MODE

Lock mode is selected using the inputs LM0 and LM1 as illustrated in the Table below.

LM0	LM1	SELECTION
0	0	lock to subcarrier
0	1	slow sync. lock external H_{ref}
1	0	slow sync. lock internal H_{ref}
1	1	fast sync. lock internal H_{ref}

The different lock modes are illustrated by the following figures:

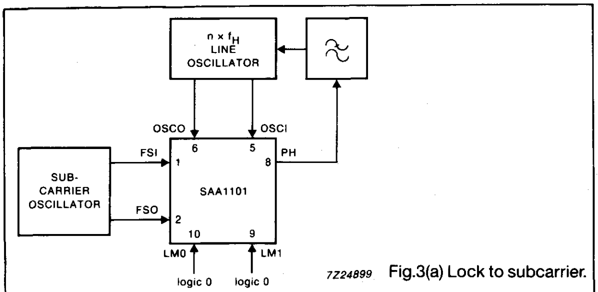


Fig.3(a) Lock to subcarrier.

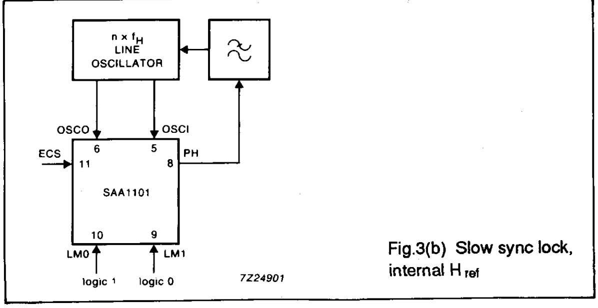


Fig.3(b) Slow sync lock, internal H_{ref}

Universal sync generator (USG)

SAA1101

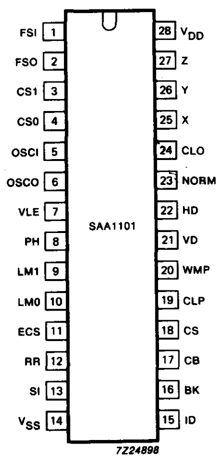


Fig.2 Pinning configuration; SOT117.

FUNCTIONAL DESCRIPTION

Generation of pulses

Generation of standard pulses such as sync, blanking and burst for TV systems: PAL B/G, PALN, PALM, SECAM and NTSC. In addition a number of non-standard pulses have been supplied to simplify signal processing. These signals include – horizontal drive, vertical drive, clamp pulse, identification etc. It is possible to select the 524/624 line mode instead of the 525/625 line mode for all the above TV systems for applications such as robotics, games and computers.

PINNING

SYMBOL	PIN	DESCRIPTION
FSI	1	subcarrier oscillator input, where f_{max} = 5 MHz
FSO	2	subcarrier oscillator output
CS1	3	clock frequency selection – CMOS input
CS0	4	clock frequency selection – CMOS input
OSCI	5	clock oscillator input, where f_{max} = 24 MHz
OSCO	6	clock oscillator output
VLE	7	vertical in-lock enable – CMOS input
PH	8	phase detector output – 3-state output
LM1	9	lock mode selection – CMOS input
LM0	10	lock mode selection – CMOS input
ECS	11	external composite sync. signal – CMOS Schmitt-trigger input
RR	12	frame reset – CMOS Schmitt-trigger input
SI	13	set identification, used to set the correct field sequence in PAL-mode. The correction (inversion of fH2) is done at the left-hand slope of the SI-pulse. Minimum pulse width is 800 ns. CMOS Schmitt-trigger input.
V_{SS}	14	ground
ID	15	identification – push-pull output
BK	16	burst key (PAL/NTSC), chroma-blanking (SECAM) – push-pull output
CB	17	composite blanking – push-pull output
CS	18	composite sync. – push-pull output
CLP	19	clamp pulse – push-pull output
WMP	20	white measurement pulse – 3-state output
VD	21	vertical drive pulse – push-pull output
HD	22	horizontal drive pulse – push-pull output
NORM	23	used with X, Y and Z to select TV system; NORM = 0, 625/525 line mode (standard); NORM = 1, 624/524 line mode – CMOS input
CLO	24	clock output – push-pull output
X	25	TV system selection input – CMOS input
Y	26	TV system selection input – CMOS input
Z	27	TV system selection input – CMOS input
V_{DD}	28	voltage supply

Universal sync generator (USG)

SAA1101

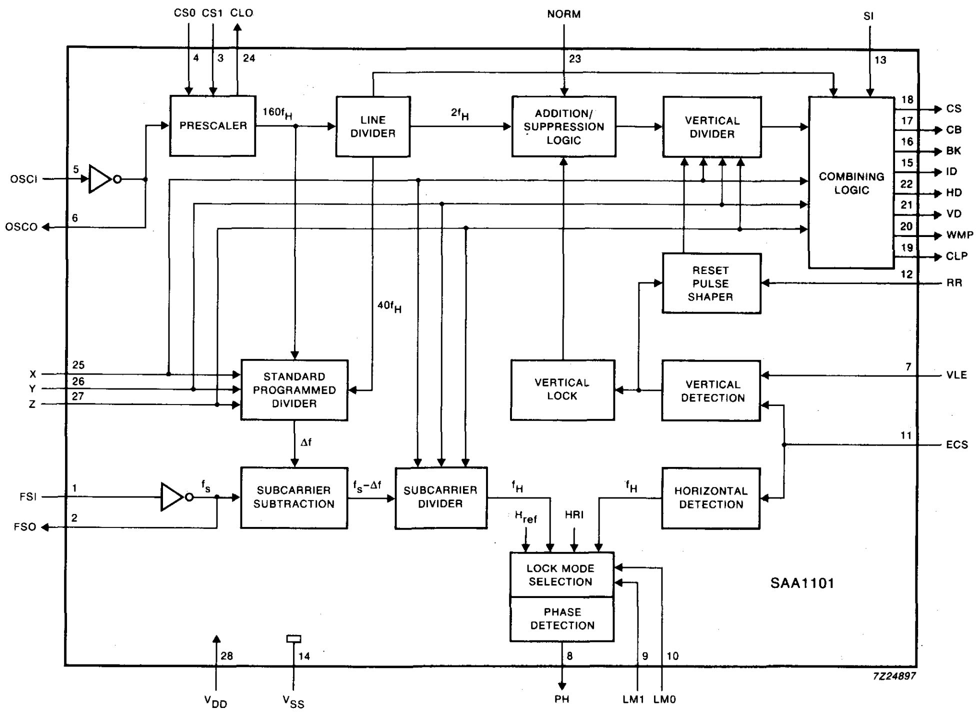


Fig.1 Block diagram.

Oscillators

The subcarrier oscillator has FSI as its input and FSO as its output. It is always used as a crystal oscillator with a series resonance crystal with parallel load capacitor. The maximum frequency, f_{max} = 5 MHz and the load capacitor, $C_L = 10 < C_L < 35$ pF.

The clock oscillator has OSCI as its input and OSCO as its output. It can be used with an LC oscillator or a series resonance crystal with parallel load capacitor (Fig.4). The maximum frequency, f_{max} = 24 MHz and the load capacitor, $C_L = 10 < C_L < 35$ pF.

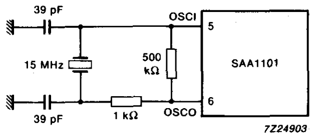


Fig.4 Crystal oscillator circuit.

Selection of TV System

Selection of the required TV system is achieved by the X, Y and Z inputs as illustrated by the following Table.

SYSTEM	X	Y	Z
SECAM1	0	0	0
PALN	0	0	1
NTSC1	0	1	0
PALM	0	1	1
SECAM2	1	0	0 (with identifier)
PAL B/G	1	0	1
NTSC2	1	1	0 (short blanking)

Selection of 625/525 (standard; interlaced mode) or 624/524 lines (non-interlaced mode)

Selection is achieved using the NORM input. When NORM = 0, 625/525 (standard) lines are selected; when NORM = 1, 624/524 line are selected.

Output Dimensions

All push-pull outputs: standard output 2 mA.

White measurement pulse, WMP: 3-state output 2 mA.

Phase detector, PH: 3-state output 2 mA.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7	V
V_I	input voltage	−0.5	V_{DD} + 0.5 *	V
I_I	maximum input current	–	±10	mA
I_O	maximum output current	–	±10	mA
I_{DD}	maximum supply current in V_{DD}	–	25	mA
P_{tot}	maximum power dissipation	–	400	mW
T_{stg}	storage temperature range	−55	+150	°C

* Input voltage should not exceed 7 V.

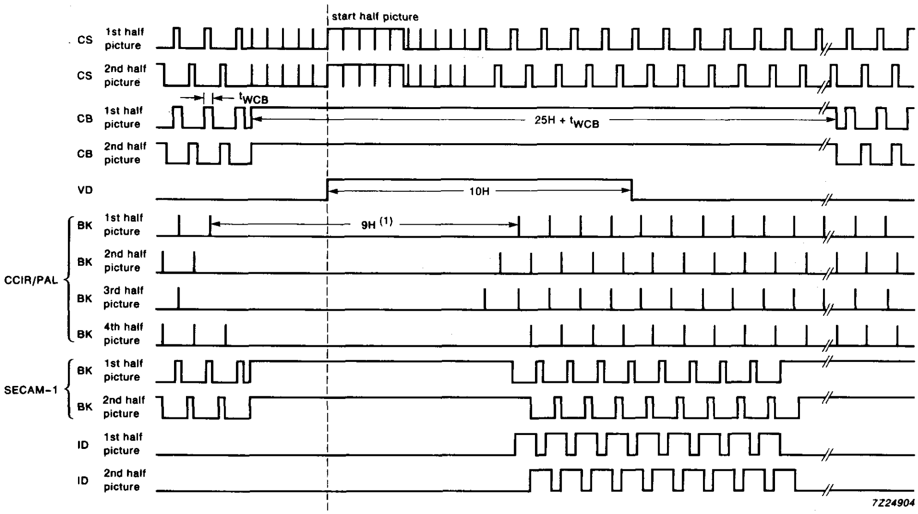
CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = -25 to +70 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	–	5.5	V
I_{DD}	supply current (quiescent)	T_{amb} = 25 °C	–	–	10	μA
Inputs						
$\pm I_I$	input leakage current	T_{amb} = 25 °C	–	–	100	nA
CMOS COMPATIBLE; X, Y, Z, NORM, CS0, CS1, LM0, LM1 AND VLE						
V_{IH}	input voltage HIGH		$0.7V_{DD}$	–	–	V
V_{IL}	input voltage LOW		–	–	$0.3V_{DD}$	V
SCHMITT TRIGGER INPUTS; ECS, RR AND SI						
V_{T+}	positive-going threshold		–	2.5	4	V
V_{T-}	negative-going threshold		1	1.5	–	V
V_H	hysteresis		0.4	1	–	V
OSCILLATOR INPUTS; OSCI AND FSI						
V_{IH}	input voltage HIGH		$0.7V_{DD}$	-	–	V
V_{IL}	input voltage LOW		–	–	$0.3V_{DD}$	V
Outputs PUSH-PULL OUTPUTS; CB, CS, BK, ID, HD, VD, CLP AND CLO						
V_{OH}	output voltage HIGH	$-I_O$ = 2 mA; V_{DD} = 5 V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 2 mA; V_{DD} = 5 V	–	–	0.5	V
OSCILLATOR OUTPUTS; OSCO AND FSO						
V_{OH}	output voltage HIGH	$-I_O$ = 0.75 mA; V_{DD} = 5 V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 0.75 mA; V_{DD} = 5 V	–	–	0.5	V
3-STATE OUTPUTS; WMP AND PH						
V_{OH}	output voltage HIGH	$-I_O$ = 2 mA; V_{DD} = 5 V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 2 mA; V_{DD} = 5 V	–	–	0.5	V
$\pm I_{OZ}$	OFF-state current	T_{amb} = 25 °C	–	–	50	nA

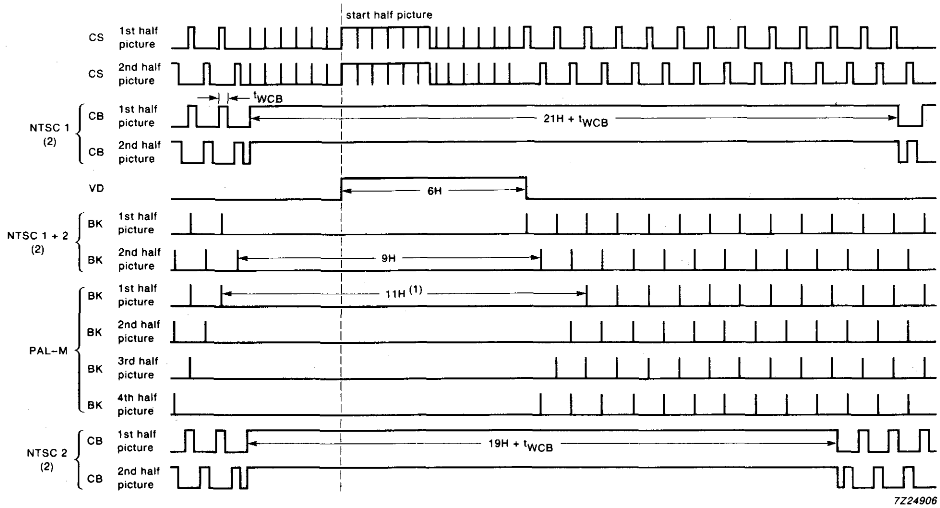
OUTPUT WAVEFORMS

The output waveforms for the different modes of operation are illustrated by Figs 5 and 6.



(1) H = 1 horizontal scan.

Fig.5 Typical output waveforms for PAL/CCIR and SECAM. In the 624-line mode the output waveforms are identical to the first half picture of PAL/CCIR and are not interlaced.



(1) H = 1 horizontal scan.

(2) NTSC mode reset; the fourth half picture is identical to the second half picture for NTSC.

Fig.6 Typical output waveforms for NTSC and PAL-M. In the 524-line mode the output waveforms are identical to the first half picture of NTSC and are not interlaced.

WAVEFORM TIMING

The waveform timing depends on the frequency of the oscillator input (f_{OSCI}). This is illustrated in the table below as the number (N) of oscillations at OSCI. The timings are derived from N x t_{OSCI} ± 100 ns.
One horizontal scan (H) = 320 x t_{OSCI} = $1/f_H$.
Where t_{OSCI} = 200 ns for PAL/SECAM and 198.6 ns for NTSC/PAL-M

SYMBOL	PARAMETER	PAL	NTSC	PAL-M	SECAM	UNIT	N
Composite sync (CS)							
t_{WSC1}	horizontal sync pulse width	4.8	4.77	4.77	4.8	µs	24
t_{WSC2}	equalizing pulse width	2.4	2.38	2.38	2.4	µs	12
t_{WSC3}	serration pulse width	4.8	4.77	4.77	4.8	µs	24
-	duration of pre-equalizing pulses	2.5	3	3	2.5	H	-
-	duration of post-equalizing pulses	2.5	3	3	2.5	H	-
-	duration of serration pulses	2.5	3	3.5	2.5	H	-
Composite blanking (CB) HORIZONTAL BLANKING PULSE WIDTH							
t_{WCB}	PAL/SECAM/PAL-M	12	–	11.12	12	µs	60
t_{WCB}	NTSC1	–	11.12	–	–	µs	56
t_{WCB}	NTSC2	–	10.53 *	–	–	µs	53
FRONT PORCH							
t_{PCBCS}	front porch	1.6	1.59	1.59	1.6	µs	8
DURATION OF VERTICAL BLANKING							
-	PAL/SECAM/PAL-M	25H + t_{WCB}	–	21H + t_{WCB}	25H + t_{WCB}	–	-
-	NTSC1	–	21H + t_{WCB}	–	–	–	-
-	NTSC2	–	19H + t_{WCB}	–	–	–	-
Burst key (BK) (not SECAM)							
t_{WBK}	burst key pulse width	2.4	2.38	2.38	–	µs	12
t_{PCSBK}	CS to burst key delay	5.6	5.56	5.76	–	µs	28
-	burst suppression	9	9	11	–	H	-

* Horizontal blanking pulse width for NTSC2 can be 11.12 µs maximum

SYMBOL	PARAMETER	PAL	NTSC	PAL-M	SECAM	UNIT	N
Burst key (BK) (not SECAM) (continued)							
POSITION OF BURST SUPPRESSION							
-	first half picture	H623 to H6	H523 to H6	H523 to H8	–	–	-
-	second half picture	H310 to H318	H261 to H269	H260 to H270	–	–	-
-	third half picture	H622 to H5	H523 to H6	H522 to H7	–	–	-
-	fourth half picture	H311 to H319	H261 to H269	H259 to H269	–	–	-
Burst key (BK) (SECAM)							
t_{WBK}	chroma pulse width	–	–	–	7.2	μs	36
t_{PBKCS}	CS to chroma delay	–	–	–	1.6	μs	8
DURATION OF VERTICAL BLANKING							
-	SECAM1	–	–	–	note 1	–	-
-	SECAM2	–	–	–	note 2	–	-
Clamp pulse (CLP)							
t_{WCLP}	clamp pulse width	2.4	2.38	2.38	2.4	μs	12
t_{PCSCLP}	CS to CLP delay	1.6	1.59	1.59	1.6	μs	8
Horizontal drive (HD)							
t_{WHD}	pulse width	7.2	7.15	7.15	7.2	μs	36
t_{PHDCS}	CS to HD delay	0.8	0.79	0.79	0.8	μs	4
-	repetition period	64	63.56	63.56	64	μs	-
Vertical drive (VD)							
-	VD duration	10	6	6	10	H	-
t_{PVDCS}	CS to VD delay	1.6	1.59	1.59	1.6	μs	8
White measurement pulse (WMP)							
-	pulse width	2.4	2.38	2.38	2.4	μs	12
-	CS to WMP delay	34.4	34.16	34.16	34.4	μs	172
-	duration of WMP	10	9	9	10	H	-

Line twenty-one acquisition and display (LITOD)

SAA5252

FEATURES

- Complete stand-alone Line 21 decoder in one package
- On-chip display RAM allowing full page Text mode
- Enhanced character display modes
- Full colour captions
- RGB interface for standard colour decoder ICs
- Automatic handling of Field 2 data
- Automatic selection of (1H, 1V), (2H, 1V) or (2H, 2V) scan modes
- Onboard OSD facility using Character generator
- RGB inputs to support existing OSD ICs
- I^2C-bus or "stand alone" pin control
- Automatic data-ready signal generation on data acquisition
- Can decode signals recorded on standard VHS and S-VHS tape.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	30	–	mA
V_{syn}	CVBS sync amplitude	0.1	0.3	0.6	V
V_{vid}	CVBS video amplitude	0.7	1.0	1.4	V
T_{amb}	operating ambient temperature	−20	–	+70	°C
T_{stg}	storage temperature	−55	–	+125	°C

GENERAL DESCRIPTION

The SAA5252 (LITOD) is a single-chip CMOS device, which will acquire, decode and display Line 21 Closed Captioning data from a 525 line composite video signal. Operation as an On-Screen Display (OSD) device is also possible. Normal and line progressive scan modes are supported.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5252P	24	DIL	plastic	SOT101

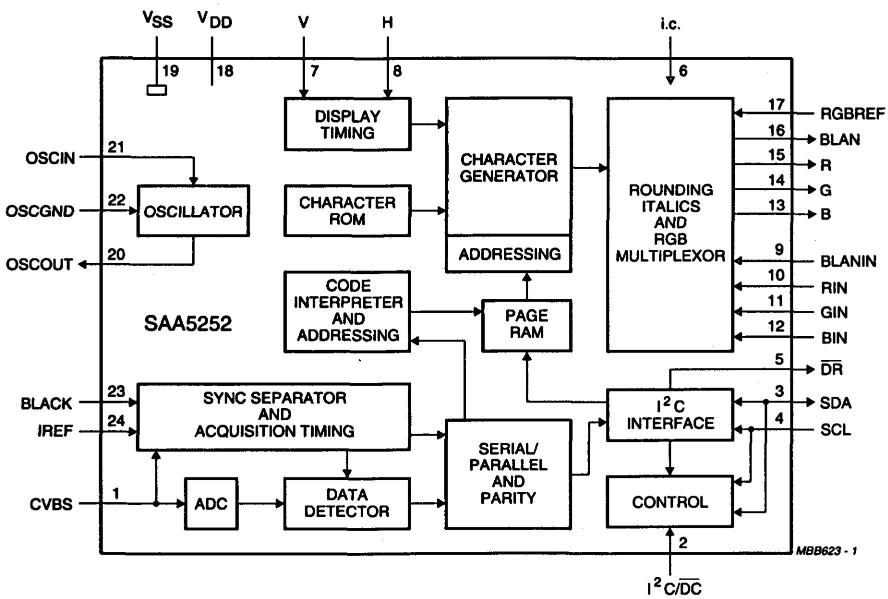


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CVBS	1	composite video input; signal should be connected via 100 nF capacitor
I²C/$\overline{DC}$	2	selects I²C or Direct Control
SDA	3	serial data port for I²C-bus or mode select input for direct control
SCL	4	serial clock input for I²C-bus or mode select input for direct control
$\overline{DR}$	5	data-ready signal to microcontroller (active-LOW) or mode select input for direct control
i.c.	6	internally connected; connect to V_{SS} for normal operation
V	7	field reference for display timing
H	8	line reference for display timing
BLANIN	9	video blanking input from external OSD device
RIN	10	RED video input from external OSD device
GIN	11	GREEN video input from external OSD device
BIN	12	BLUE video input from external OSD device
B	13	BLUE video output
G	14	GREEN video output
R	15	RED video output
BLAN	16	video blanking output
RGBREF	17	voltage defining output HIGH level for RGB pins for closed captioning output
V_{DD}	18	+5 V supply
V_{SS}	19	0 V ground
OSCOUT	20	oscillator output
OSCIN	21	oscillator input
OSCGND	22	oscillator ground
BLACK	23	video black level storage; connected to V_{SS} via 100 nF capacitor
IREF	24	reference current input; connected to V_{SS} via 27 kΩ resistor

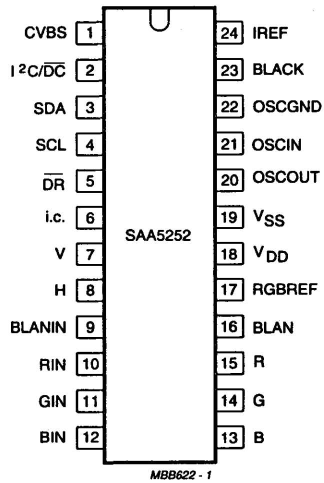


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)		−0.3	+6.5	V
V_I	maximum input voltage (any input)	note 1	−0.3	V_{DD} +0.5	V
V_O	maximum output voltage (any output)	note 1	−	V_{DD} +0.5	V
V_{dif}	difference between V_{SS} and OSCGND		−	±0.25	V
I_{IOK}	DC input or output diode current		−	±20	mA
I_O	maximum output current (each output)		−	±10	mA
T_{amb}	operating ambient temperature		−20	+70	°C
T_{stg}	storage temperature		−55	+125	°C
	electrostatic handling				
$V_{stat(HBM)}$	Human body model	note 2	−2000	+2000	V
$V_{stat(MM)}$	machine model	note 3	−200	+200	V

Notes

1. This maximum value has an absolute maximum of 6.5 V independent of V_{DD}.
2. The Human body model ESD simulation is equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor, which produces single discharge transient. Reference Philips Semiconductors Test Method UZW-BO/FQ-A302 (similar to MIL-STD 883C method 3015.7)
3. The Man machine ESD simulation is equivalent to discharging a 200 pF capacitor via a resistor and series inductor with effective dynamic values of 25 Ω and 2.5 μH, which produces a damped oscillating discharge. Reference Philips Semiconductors Test Method UZW-BO/FQ-B302 (similar to EIAJ IC-121 Test Method 20 condition C).

Quality

This device will meet the requirements of the Philips Semiconductors General Quality Specification UZW-BO/FQ-0601. This details the acceptance criteria for all Q & R tests applied to the product.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	positive supply voltage		4.5	5.0	5.5	V
I_{DD}	total supply current		–	30	–	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
V_{ivid}	video input amplitude (peak-to-peak value)		0.7	1.0	1.4	V
V_{idat}	caption data amplitude		0.25	0.35	0.49	V
Z_{src}	source impedance		–	–	250	Ω
V_I	input switching level of sync separator		1.7	2.0	2.3	V
Z_I	input impedance		2.5	5	–	kΩ
C_I	input capacitance		–	–	10	pF
IREF						
R_{24}	resistor to ground		–	27	–	kΩ
V_{24}	voltage on pin 24		–	$V_{DD}/2$	–	V
H						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_I	maximum input current		−1	–	+1	mA
C_I	input capacitance		–	–	10	pF
t_r	pulse rise time		–	–	5	µs
t_f	pulse fall time		–	–	5	µs
t_W	pulse width					
	1H		1	12	63	µs
	2H		1	6	31	µs
V						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
I_I	maximum input current		−1	–	+1	mA
t_r	pulse rise time		–	–	5	ns
t_f	pulse fall time		–	–	5	ns
t_W	pulse width		1	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGBREF						
V_I	input voltage		−0.3	−	V_{DD}	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	−	+10	μA
RGB inputs						
V_{IL}	LOW level input voltage		−0.3	−	0.8	V
V_{IH}	HIGH level input voltage		2.0	−	V_{DD}+0.5	V
Z_I	input impedance		2.5	5	−	kΩ
BLANIN						
V_{IL}	LOW level input voltage		−0.3	−	0.8	V
V_{IH}	HIGH level input voltage		2.0	−	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	−	+10	μA
t_r	input rise time	between 10% and 90%	−	−	80	ns
t_f	input fall time	between 90% and 10%	−	−	80	ns
I²C/$\overline{DC}$						
V_{IL}	LOW level input voltage		0	−	0.8	V
V_{IH}	HIGH level input voltage		2.0	−	V_{DD}	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	−	+10	μA
SCL						
V_{IL}	LOW level input voltage		−0.3	−	1.5	V
V_{IH}	HIGH level input voltage		3.0	−	V_{DD}+0.5	V
f_{CLK}	clock frequency		0	−	100	kHz
t_r	input rise time	between 10% and 90%	−	−	2	μs
t_f	input fall time	between 90% and 10%	−	−	2	μs
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	−	+10	μA
C_I	input capacitance		−	−	10	pF
Inputs/Outputs						
Ceramic resonator (see Fig.5)						
f_{OSC}	oscillation frequency		11.82	12	12.18	MHz
C0	parallel capacitance		−	5.35	−	pF
C1	series capacitance		−	37.4	−	pF
L1	series inductance		−	35.5	−	μH
R1	series resistance		−	6	25	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BLACK						
C_{blk}	storage capacitance to ground		–	100	–	nF
V_{blk}	black level voltage for nominal sync amplitude		1.8	2.15	2.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
SDA (open drain)						
V_{IL}	LOW levelinput voltage		−0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	between 10% and 90%	–	–	2	μs
t_f	input fall time	between 90% and 10%	–	–	2	μs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	between 3 V and 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF
DR (open drain)						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
t_f	output fall time	measured between 4.0 V and 1.0 V with 3.3 kΩ to 5 V	–	–	50	ns
C_L	load capacitance		–	–	100	pF
Outputs						
R, G, B (caption mode)						
V_{OL}	LOW level output voltage	I_{OL} = +2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = −2 mA	RGBREF −0.3	RGBREF	RGBREF +0.4	V
Z_O	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10% and 90%	–	–	10	ns
t_f	output fall time	between 90% and 10%	–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BLAN						
V_{OL}	LOW lecvel output voltage	I_{OL} = +0.2 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	1.1	–	2.8	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10% and 90%	–	–	10	ns
t_f	output fall time	between 90% and 10%	–	–	10	ns
T_{sk}	skew delay between display and R, G, B, BLAN		–	–	10	ns
I²C Timings (see Fig.3)						
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;\,DAT}$	data set-up time		250	–	–	ns
$t_{HD;\,DAT}$	data hold time		170	–	–	ns
$t_{SU;\,STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;\,STA}$	START hold time		4	–	–	µs
$t_{SU;\,STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs
t_r	output rise time	between 10% and 90%	–	–	10	ns
t_f	output fall time	between 90% and 10%	–	–	10	ns

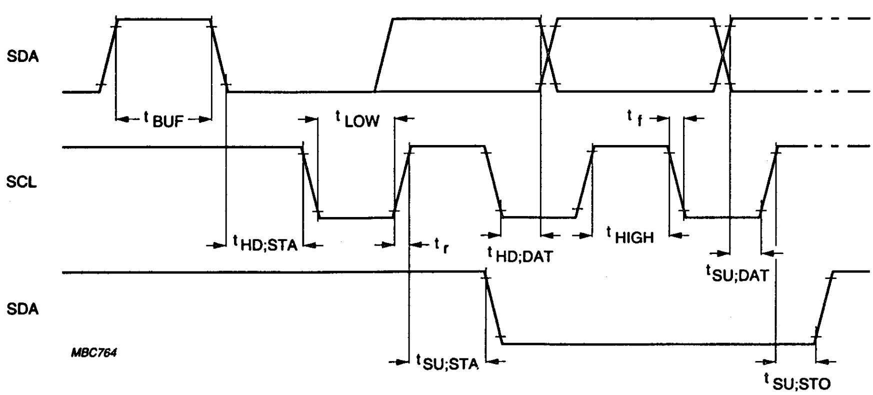
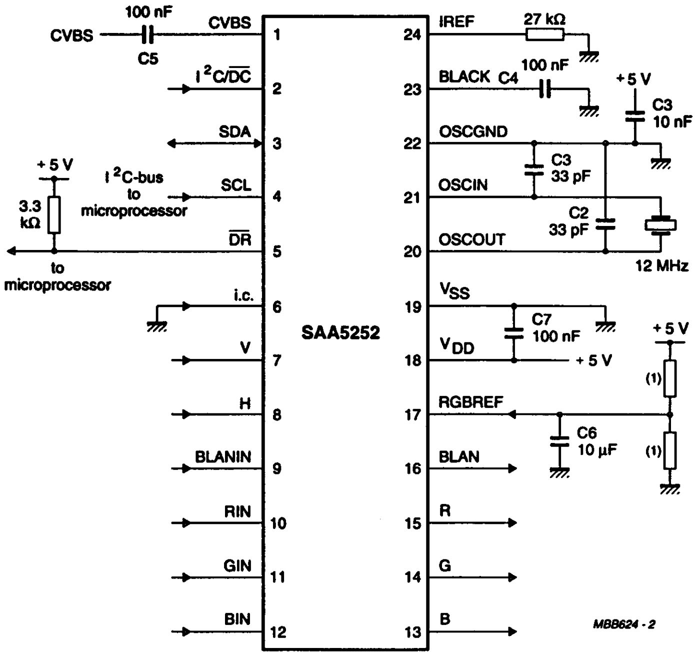


Fig.3 I²C-bus timing diagram.

APPLICATION INFORMATION



(1) Value dependant on application.

Fig.4 Application diagram.

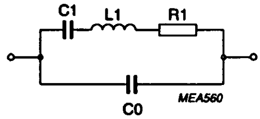


Fig.5 Ceramic resonator equivalent circuit.

DISPLAY GENERATOR

General Description

The displayed characters are defined on a 5 by 12 matrix within a 7 by 13 window, allowing one blank pixel either side of the character and a blank pixel row above. There are a number of display options available controlled by Register 1, or external pins in stand-alone mode.
The three display modes are video, text and caption, the device is powered up in the video mode.
The display generator reads the Pre-amble Address Code (PAC) then the data associated with that row. Each character is then rounded after which it can be italicised and/or underlined, depending on the PAC or mid-row codes, before being passed on to the output circuitry.
Figure 6 shows the character set.

Display of external On Screen Display (OSD) facilities

The R, G, B and BLAN outputs of the display have the capability to be put in a 3-state mode allowing other OSD devices to take control of the television R, G, B and BLAN signals.

When the BLANIN is held HIGH then the R, G, B and BLAN outputs from display are disabled and the R, G, B and BLAN signals come directly from the RGBIN and BLANIN inputs. This will allow On Screen Display to be placed on top of the captioning without any corruption, leaving the captions intact when the On Screen Display is switched off (BLANIN goes LOW). In this form of operation the RGBIN and RGBOUT pins can be considered transparent; BLANIN goes through the normal output buffer to BLAN.

Table 1 Register map (WRITE).

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
00	DF1/2	RGB, BLAN +ve/–ve	H +ve/–ve	V +ve/–ve	H3	H2	H1	H0
01	CLEAR	CH 2/1	NARROW/ WIDE	ACQ OFF	EN1	EN0	M1	M0
02	–	–	–	–	ROW3	ROW2	ROW1	ROW0
03	–	–	–	COL4	COL3	COL2	COL1	COL0
04	–	OSD6	OSD5	OSD4	OSD3	OSD2	OSD1	OSD0

Table 2 Register map (READ).

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
00	POR	0	0	0	F1/F2	EDS	PARITY SHUTDOWN	DATA READY
01	PARITY ERROR	DATA BIT 7	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1
02	PARITY ERROR	DATA BIT 7	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1

b3 b2 b1 b0	row	b6 b5 b4 → / column	0 0 1 1	0 1 0 2	0 1 1 3	1 0 0 4	1 0 1 5	1 1 0 6	1 1 1 7
0 0 0 0	0	white	®			@	P	ú	p
0 0 0 1	1	white underline	°	!	1	A	Q	a	q
0 0 1 0	2	green	½	"	2	B	R	b	r
0 0 1 1	3	green underline	¿	#	3	C	S	c	s
0 1 0 0	4	blue	™	$	4	D	T	d	t
0 1 0 1	5	blue underline	¢	%	5	E	U	e	u
0 1 1 0	6	cyan	£	&	6	F	V	f	v
0 1 1 1	7	cyan underline	♪	'	7	G	W	g	w
1 0 0 0	8	red	à	(	8	H	X	h	x
1 0 0 1	9	red underline		)	9	I	Y	i	y
1 0 1 0	A	yellow	è	á	:	J	Z	j	z
1 0 1 1	B	yellow underline	â	+	;	K	[	k	ç
1 1 0 0	C	magenta	ê	,	<	L	é	l	÷
1 1 0 1	D	magenta underline	î	-	=	M	]	m	Ñ
1 1 1 0	E	italics	ô	.	>	N	í	n	ñ
1 1 1 1	F	italics underline	û	/	?	O	ó	o	█

(hatched box) signifies "flash on" command

(empty box) signifies a transparent space

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The '0' and 'zero' use the same character, 4Fh.

Fig.6 Character set.

I²C INTERFACE

Description of WRITE registers

The write subaddresses auto increment from 0 through to 4 at which point they stay until a new write subaddress is sent. Registers are set to all logic 0 at power-up.

REGISTER 0 WRITE (CONTROL BYTE 1)

- D0 to D3 H0 to H3 set the offset position from the start of the line sync pulse, this will be set to a nominal value on reset.
- D4 Field sync pulse expected to be negative going logic 0 or positive going logic 1.
- D5 Line sync pulse expected to be negative going logic 0 or positive going logic 1.
- D6 Video outputs will be positive going logic 0 or negative going logic 1.
- D7 Data field select. When set to logic 0 Field 1 is decoded, when set to logic 1 Field 2 is decoded.

REGISTER 1 WRITE (CONTROL BYTE 2)

- D0, D1 Display mode selection bits. Table 3 shows the possible display modes.
- D2,D3 Enhanced caption mode selection bits. Table 4 shows the possible enhanced caption modes.
- D4 When set to logic 1 acquisition of caption data is inhibited to allow the display to be used for On Screen Display purposes.
- D5 Acquisition window selection. When set to logic 0 only line 21 is checked for caption data. When set to logic 1, lines 19 to 23 of both fields are checked, allowing encrypted video signals to be handled.
- D6 User channel selection.
- D7 Clears the page memory when set HIGH. The page memory will be cleared within two fields (30 ms).

Table 3 Display modes.

DISPLAY MODE OPTIONS	M1	M0
Video only	0	0
Text mode	0	1
Normal caption mode	1	0
Enhanced caption mode	1	1

Table 4 Enhanced caption modes.

ENHANCED CAPTION MODES	EN1	EN0
Enhanced caption modes	EN1	EN0
Shadowed character/Video background	0	0
Shadowed character/Mesh background	0	1
Normal character/Video background	1	0
Normal character/Mesh background	1	1

REGISTER 2 WRITE (ON SCREEN DISPLAY DATA ROW ADDRESS)

- D0 to D3 Row 0 to 3, sets the row address for on screen display. This stored value will be incremented by overflow increments of Register 3.

REGISTER 3 WRITE (ON SCREEN DISPLAY DATA COLUMN ADDRESS)

- D0 to D4 Columns 0 to 4, sets the column address for On Screen Display. This stored value will be incremented by writes to Register 4.

REGISTER 4 WRITE (ON SCREEN DISPLAY DATA)

- D0 to D6 OSD0 to 6, On Screen Display data bits writing to this register causes Register 3 to increment its stored value.

Description of READ registers

The read subaddresses auto increment from 0 through to 2 at which point they stay until a new read subaddress is sent.

REGISTER 0 READ (STATUS)

All these bits are reset to logic 0 after the register is read.

- D0 Data ready (new data has been acquired)
- D1 Parity error shut-down, goes HIGH when SAA5252 has a parity shut-down condition.
- D2 Indicates the following bytes are extended data service bytes
- D3 Indicates Field 1 or Field 2 data bytes

D7 Indicates a Power-On Reset (POR) has occurred, all I^{2}C-bus write registers have been reset to zero.

REGISTER 1 READ (FIRST DATA BYTE)

D0 to D6 Data Bit 1 to Data Bit 7 (see note).

D7 Parity error flag bit. Bit goes HIGH when a parity error has occurred.

REGISTER 2 READ (SECOND DATA BYTE)

D0 to D6 Data Bit 1 to Data Bit 7 (see note).

D7 Parity error flag bit. Bit goes HIGH when a parity error has occurred.

Note In the Line 21 Specification data bits are numbered D1 to D8

Interface to Microcontroller using I^{2}C-bus

The interface to the microcontroller is via the two-wire serial I^{2}C-bus, and optionally by a Data-Ready signal ($\overline{\text{DR}}$). On power up the microcontroller initializes the device by an I^{2}C-bus WRITE to Registers 0 (Control Byte 1). The I^{2}C-bus subaddress is then auto incremented to point to Register 1 (Control Byte 2). These two registers configure the device to the users requirements.

If the device is to be used for data acquisition only, then there are three methods by which the microcontroller can be informed of the arrival of valid Line 21 data:

- It can poll the $\overline{\text{DR}}$ pin, if the function has been enabled, and wait for it to go LOW.
- It can use the negative edge of the $\overline{\text{DR}}$ signal to cause an interrupt.
- It can poll the Data Ready bit (bit D0 of the status byte, I^{2}C-bus READ Register 0).

When valid data is detected, the microcontroller must initiate an I^{2}C-bus READ of Registers 0, 1 and 2. The first and second data bytes from the most recently received Line 21 are in Register 1 and Register 2 respectively.

The $\overline{\text{DR}}$ pin, and the Data Ready bit (Status Byte D0) will be cleared after any register has been read. POR is reset after Register 0 has been read.

STAND-ALONE (NON I^{2}C) OPERATION

To set the SAA5252 for stand-alone operation pin 2 (I^{2}C/$\overline{\text{DC}}$) is tied LOW. This will change the operation of the SCL, SDA and $\overline{\text{DR}}$ pins to mode select inputs which will select as shown in Table 5.

In the caption mode the SAA5252 operates in the basic Normal character/Black background mode. This complies with the FCC ruling. In the Enhanced caption mode the set up will be Shadowed character/Video background. SDA and SCL in the stand-alone operation act as bits M0 and M1 in Table 3

Table 5 Stand-alone modes.

$\overline{\text{DR}}$	SCL	SDA	MODE OF OPERATION	CHANNEL RECEPTION
0	0	0	Video mode	Channel 1
0	0	1	Text mode	Channel 1
0	1	0	Normal captions	Channel 1
0	1	1	Enhanced captions	Channel 1
1	0	0	Video mode	Channel 2
1	0	1	Text mode	Channel 2
1	1	0	Normal captions	Channel 2
1	1	1	Enhanced captions	Channel 2

PURCHASE OF PHILIPS I^{2}C COMPONENTS

Digital multistandard colour decoder with SCART interface (DMSD2-SCART)

SAA7151B

1. FEATURES

- 8-bit performance on chip for luminance and chrominance signal processing for PAL, NTSC and SECAM standards
- Separate 8-bit luminance and 8-bit chrominance input signals from Y/C, CVBS, S-Video (S-VHS or Hi8) sources
- SCART signal insertion by means of RGB/YUV convertion; fast switch handling
- Horizontal and vertical sync detection for all standards
- Real time control output RTCO
- Fast sync recovery of vertical blanking for VCR signals (bottom flutter compensation)
- Controls via the I^2C-bus
- User programmable aperture correction (horizontal peaking)
- Cross-colour reduction by chrominance comb-filtering (NTSC) or by special cross-colour cancellation (SECAM)
- 8-bit quantization of output signals in 4:1:1 or 4:2:2 formats
- 720 active samples per line
- The YUV bus supports a data rate of 13.5 MHz (CCIR 601).
  - (864 x f_H) for 50 Hz
  - (858 x f_H) for 60 Hz
- Compatible with memory-based features (line-locked clock)
- One 24.576 MHz crystal oscillator for all standards

2. GENERAL DESCRIPTION

The SAA7151B is a digital multistandard colour-decoder having two 8-bit input channels, one for CVBS or Y, the other for chrominance or time-multiplexed colour-difference signals.

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37 and 52)	4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37 and 52)	-	100	250	mA
V_I	input levels	TTL-compatible			
V_O	output levels	TTL-compatible			
T_{amb}	operating ambient temperature	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7151B	68	mini-pack PLCC	plastic	SOT188

5. BLOCK DIAGRAM

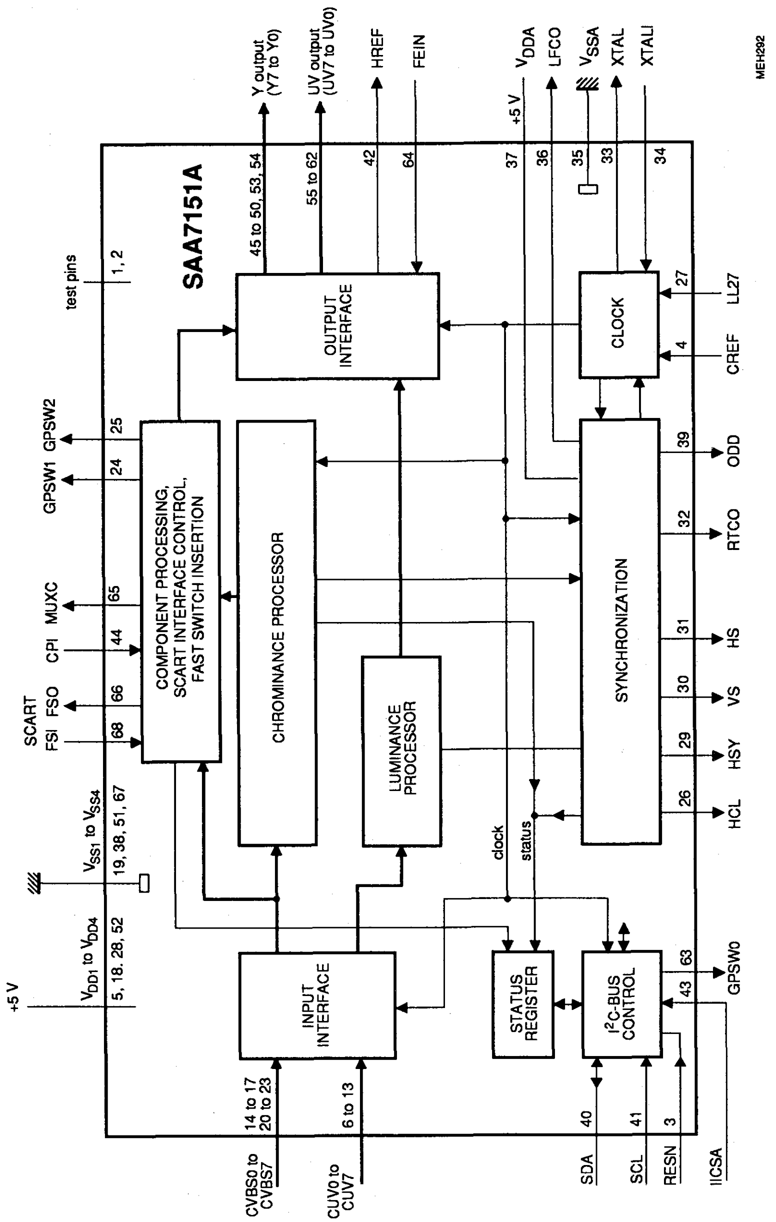

Fig. 1 Block diagram (application circuits see Figures 17, 18 and 19).

6. PINNING

SYMBOL	PIN	DESCRIPTION
SP	1	connected to ground (shift pin for testing)
AP	2	connected to ground (action pin for testing)
RESN	3	reset, active-LOW
CREF	4	clock reference, sync from external to ensure in-phase signals on the Y-, CUV- and YUV-bus
V_{DD1}	5	+5 V supply input 1
CUV0	6	chrominance input data bits CUV7 to CUV0 (digitized chrominance signals in two's complement format from a S-Video source (S-VHS, Hi8) or time-multiplexed colour-difference signals from a YUV(RGB) source or both in combination)
CUV1	7	
CUV2	8	
CUV3	9	
CUV4	10	
CUV5	11	
CUV6	12	
CUV7	13	
CVBS0	14	CVBS lower input data bits CVBS3 to CVBS0 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS1	15	
CVBS2	16	
CVBS3	17	
V_{DD2}	18	+5 V supply input 2
V_{SS1}	19	ground 1 (0 V)
CVBS4	20	CVBS upper input data bits CVBS7 to CVBS4 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS5	21	
CVBS6	22	
CVBS7	23	
GPSW1	24	status bit output FSST0 or port 1 output for general purpose (programmable by subaddress 0C)
GPSW2	25	status bit output FSST1 or port 2 output for general purpose (programmable by subaddress 0C)
HCL	26	black level clamp pulse output (begin and stop programmable), e.g. for TDA8708A (ADC)
LL27	27	line-locked system clock input signal (27 MHz)
V_{DD3}	28	+5 V supply input 3
HSY	29	hor. sync pulse reference output (begin and stop programmable), e.g. for gain adj.TDA8708A (ADC)
VS	30	vertical sync output signal (Fig.10)
HS	31	horizontal sync output signal (Fig.14; start point programmable)
RTCO	32	real time control output; serial increments of HPLL and FSCPLL and status PAL or SECAM sequence (Fig.9)
XTAL	33	24.576 MHz clock output (open-circuit for use with external oscillator)
XTALI	34	24.576 MHz connection for crystal or external oscillator (TTL compatible squarewave)

SYMBOL	PIN	DESCRIPTION
V_{SSA}	35	analog ground
LFCO	36	line frequency control output signal, multiple of horizontal frequency (nominal 6.75 MHz)
V_{DDA}	37	+5 V supply input for analog part
V_{SS2}	38	ground 2 (0 V)
ODD	39	odd/even field identification output (odd = HIGH)
SDA	40	I^2C-bus data line
SCL	41	I^2C-bus clock line
HREF	42	horizontal reference for YUV data outputs (for active line 720Y samples long)
IICSA	43	set module address input of I^2C-bus (LOW = 1000 101X; HIGH = 1000 111X)
CPI	44	clamping pulse input (digital clamping of external UV signals)
Y7	45	Y signal output bits Y7 to Y2 (luminance), part of the digital YUV-bus
Y6	46	
Y5	47	
Y4	48	
Y3	49	
Y2	50	
V_{SS3}	51	ground 3 (0 V)
V_{DD4}	52	+5 V supply input 4
Y1	53	Y signal output bits Y1 to Y0 (luminance), part of the digital YUV-bus
Y0	54	
UV7	55	UV signal output bits UV7 to UV0, part of the digital YUV-bus
UV6	56	
UV5	57	
UV4	58	
UV3	59	
UV2	60	
UV1	61	
UV0	62	
GPSW0	63	port output for general purpose (programmable by subaddress 0D)
FEIN	64	fast enable input (active-LOW to control fast switching due to YUV data; HIGH = YUV high-Z
MUXC	65	multiplexer control output; source select signal for external ADC (UV signal multiplexing)
FSO	66	fast switch and sync insertion output; gated FS signal from FSI or sync insertion pulse in full screen RGB mode
V_{SS4}	67	ground 4 (0 V)
FSI	68	fast switch input signal fed from SCART/peri-TV connector (indicates fast insertion of RGB signals)

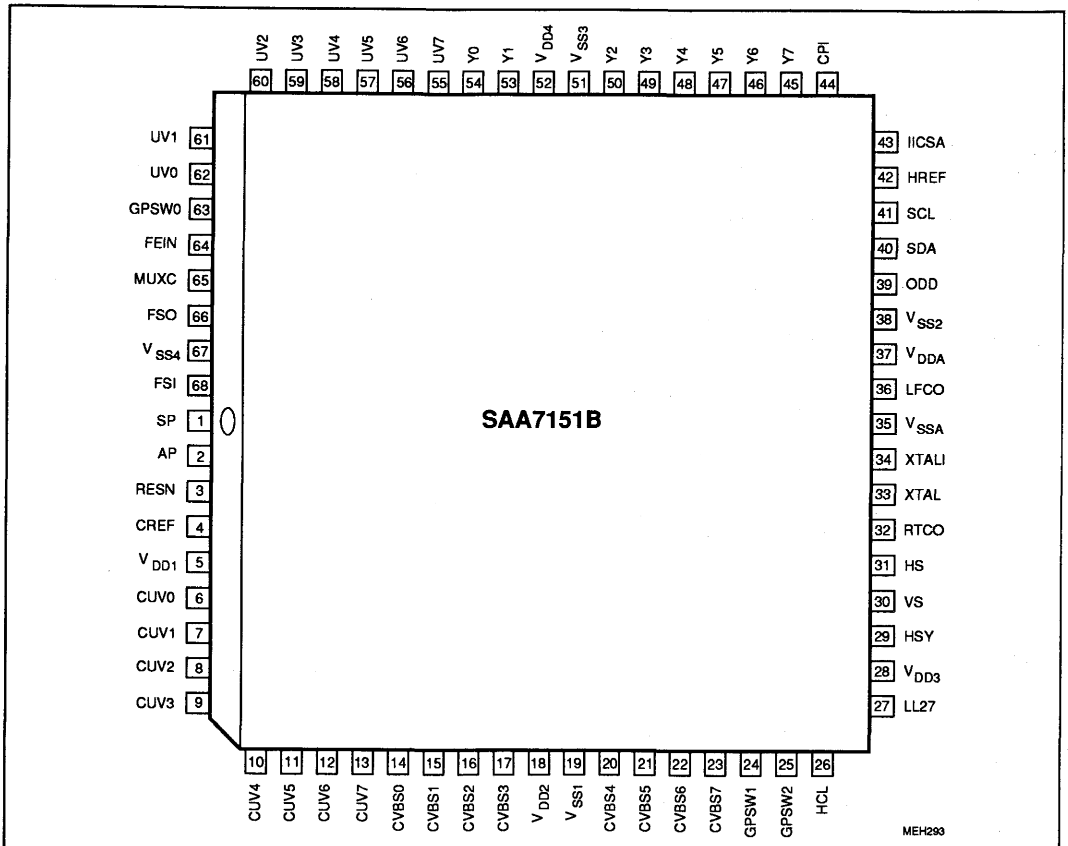

Fig.2 Pin configuration.

7. FUNCTIONAL DESCRIPTION

System configuration

The SAA7151B system processes digital TV signals with line-locked clock in PAL, SECAM and NTSC standards (CVBS or S-Video) as well as RGB signals coming from a SCART/peri-TV connector. The different source signals are switched, if necessary matrixed and converted (Fig.3 and Table 1).
8-bit CVBS data (digitized composite video) and 8-bit UV data (digitized chrominance and/or time-multiplexed colour-difference signals) are fed to the SAA7151B. The data rate is 27 MHz.

Chrominance processing

The 8-bit chrominance input signal (signal "C" out of CVBS or Y/C in Fig.4a) is fed via the input interface to a bandpass filter for eliminating the DC component, then to the quadrature demodulator. Subcarrier signals from the local oscillator (DTO1) with 90 degree phase shift are applied to its multiplier inputs. The frequency depends on set TV standard.

The multipliers operate as a quadrature demodulator for all PAL and NTSC signals; it operates as a frequency down-mixer for SECAM signals.
The two multiplier output signals are converted to a serial UV data stream and applied to two low-pass filter stages, then to a gain controlled amplifier. A final multiplexed low-pass filter achieves, together with the preceding stages, the required bandwidth performance.
The from PAL and NTSC originated signals are applied to a comb-filter.
The signals, originated from SECAM, are fed through a cloche filter (0 Hz centre frequency), a phase demodulator and a differentiator to obtain frequency-demodulated colour-difference signals.

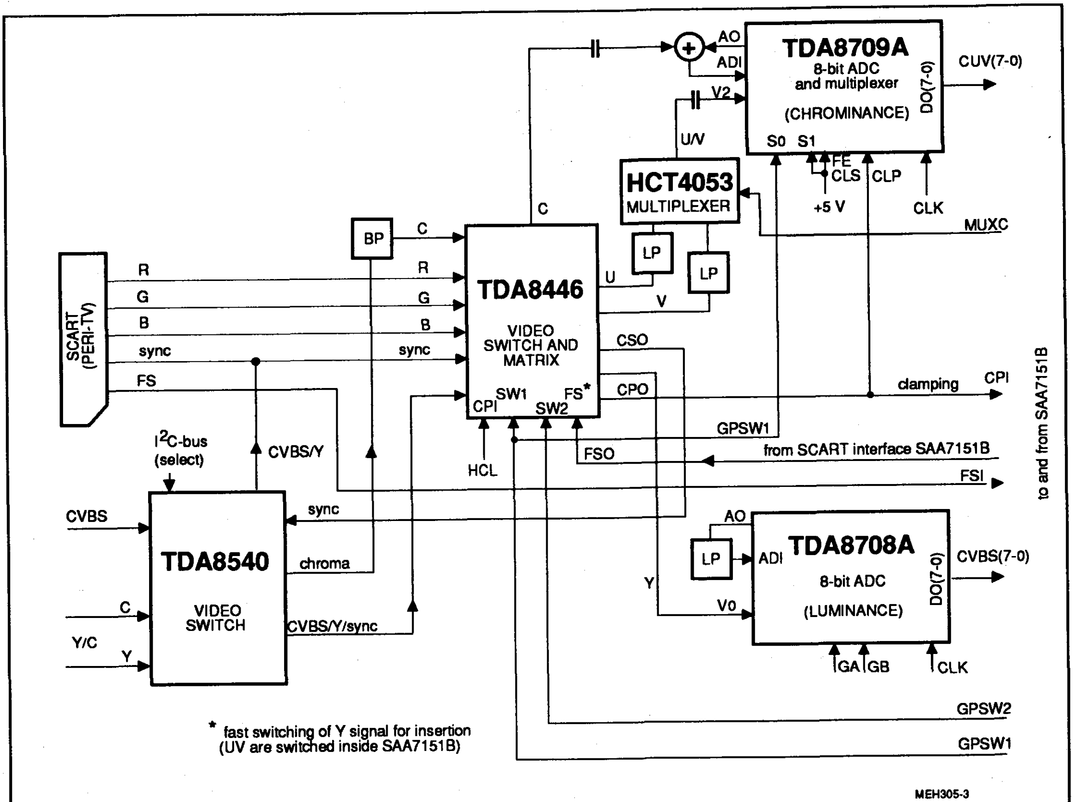

Fig.3 System configuration, RGB fast switch interface included (SCART).

The SECAM signals are fed after de-emphasis to a cross-over switch, to provide the both serial-transmitted colour-difference signals. These signals are finally fed via the fast switch to the output formatter stages and to the output interface. Chrominance signals are output in parallel (4:2:2) on the YUV-bus. The data rate of Y signal (pixel rate) is 13.5 MHz. UV signals have a data rate of 13.5 MHz/2 for the 4:2.2 format (Table 2) respectively 13.5 MHz/4 for the 4:1.1 format (Table 3)

Component processing and SCART interface control

The 8-bit multiplexed colour-difference input signal (signal CUV, Fig.1, out of matrixed RGB in Fig.3) is fed via the input interface to a chrominance stop filter (UV signal only can pass through; Figures 20 to 22). Here it is clamped and fed to the offset compensation which can be enabled or disabled via the I^{2}C-bus.

For matrixed RGB signals – the full screen SCART mode and the fast insertion mode (blanking/switching) are selectable. The chrominance stop filter is automatically bypassed in full screen SCART mode.

Full screen RGB mode (SCART):

The CUV digital input signal (7-0) consists of time-multiplexed samples for U and V. An offset correction for both signals is applied to correct external clamping errors. An internal timing correction compensates for slight differences in timing during sampling. The U and V signals are delay-compensated and fed to the output formatter. The format 4:2:2 or 4:1:1 is generated by a switchable filter.
The control signals for the front end (Figures 3 and 18) MUXC, status bits FSST1, FSST0 (outputs GPSW2, GPSW1) and FSO are generated by the SAA7151B.

Table 1 SCART interface control (Fig.3)

MODE	CONNECTION FSO	GPSW 2	GPSW 1	MUXC	chroma output of TDA8446 to TDA8709A	TDA8709A selected input	CUV (7-0)	luminance fast switch TDA8446	input selector (via I^2C-bus) TDA8540
RGB only	0 0	0 0	0 0	0 1	high-Z	VIN2	U/V	sync (RGB)	sync (RGB)
Y/C or CVBS only	0 0	0 0	1 1	0 1	C	VIN1	C	Y (Y/C) or CVBS	Y (Y/C) or CVBS
Fast switch	0 0	1 1	0 0	0 1	C	VIN2	0.5(C+U)/ 0.5(C+V)	Y (Y/C) or CVBS	Y (Y/C) or CVBS
	0 0	1 1	1 1	0 1	not used				
RGB only	1 1	0 0	0 0	0 1	high-Z	VIN2	U/V	Y (RGB)	sync (RGB)
	1 1	0 0	1 1	0 1	not used				
Fast switch	1 1	1 1	0 0	0 1	C	VIN2	0.5(C+U)/ 0.5(C+V)	Y (RGB)	Y (Y/C) or CVBS
	1 1	1 1	1 1	0 1	not used				

Fast insertion mode:

Fast insertion is applied by FSI pulse to ensure correct timing. The RGB source signal is matrixed into UV and inserted into the CVBS or Y/C source signal after two field periods if FSI pulses are received. The output FSO is set to HIGH during a determined insertion window (screen plain minus 6 % of horizontal and vertical deflection). Switch over depends on the phase of FSI in relation to the valid pixel sequence depending on the phase-different weighting factors. They are applied to the original and the inserted UV data (Figures 5 and 6)
The control signals for the front end (Table 1) MUXC, FSO, status bits FSST1 and FSST0 (outputs GPSW2 and GPSW1) are generated by the SAA7151B .

The amplitude of chrominance and colour-difference signals are scaled down by factor 2 to avoid overloading of the chrominance analog-to-digital converter. The amplitudes are reduced in the TDA8446 by signals on lines GPSW2 and GPSW1.

Luminance processing

The luminance input signal, a digital CVBS format or an 8-bit luminance format (S-Video), is fed through a sample rate converter to reduce the data rate to 13.5 MHz (Fig.4b).

Sample rate is converted by means of a switchable pre-filter. High frequency components are emphasized to compensate for loss in the following chrominance trap filter. This chrominance trap filter (f_0 = 4.43 MHz or f_0 = 3.58 MHz centre frequency selectable) eliminates the most of the colour carrier signal, therefore, it must be bypassed for S-Video signals.

The high frequency components of the luminance signal can be "peaked" in two bandpass filters with selectable transfer characteristic.
A coring circuit (±1 LSB) can improve the signal , this signal is then added to the original signal. A switchable amplifier achieves a common DC amplification, because the DC gains are different in both chrominance trap modes. Additionally, a cut-off sync pulse is generated for the original signal in both modes.

Synchronization

The luminance output signal is fed to the synchronization stage. Its bandwidth is reduced to 1 MHz in a low-pass filter (sync pre-filter).
The sync pulses are sliced and fed to the phase detectors to be compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to

Digital multistandard colour decoder with SCART interface (DMSD2-SCART)

SAA7151B

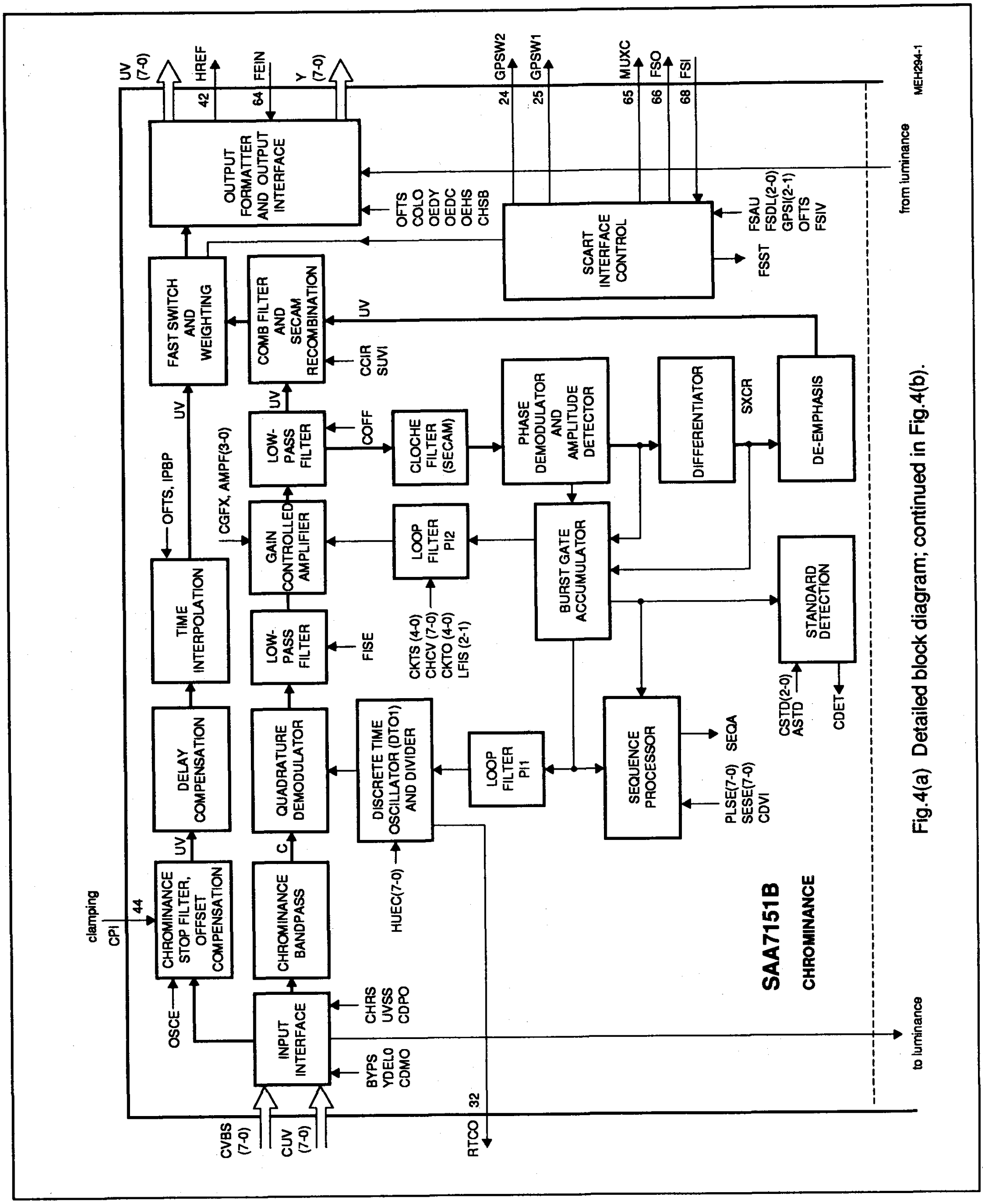

Fig.4(a) Detailed block diagram; continued in Fig.4(b).

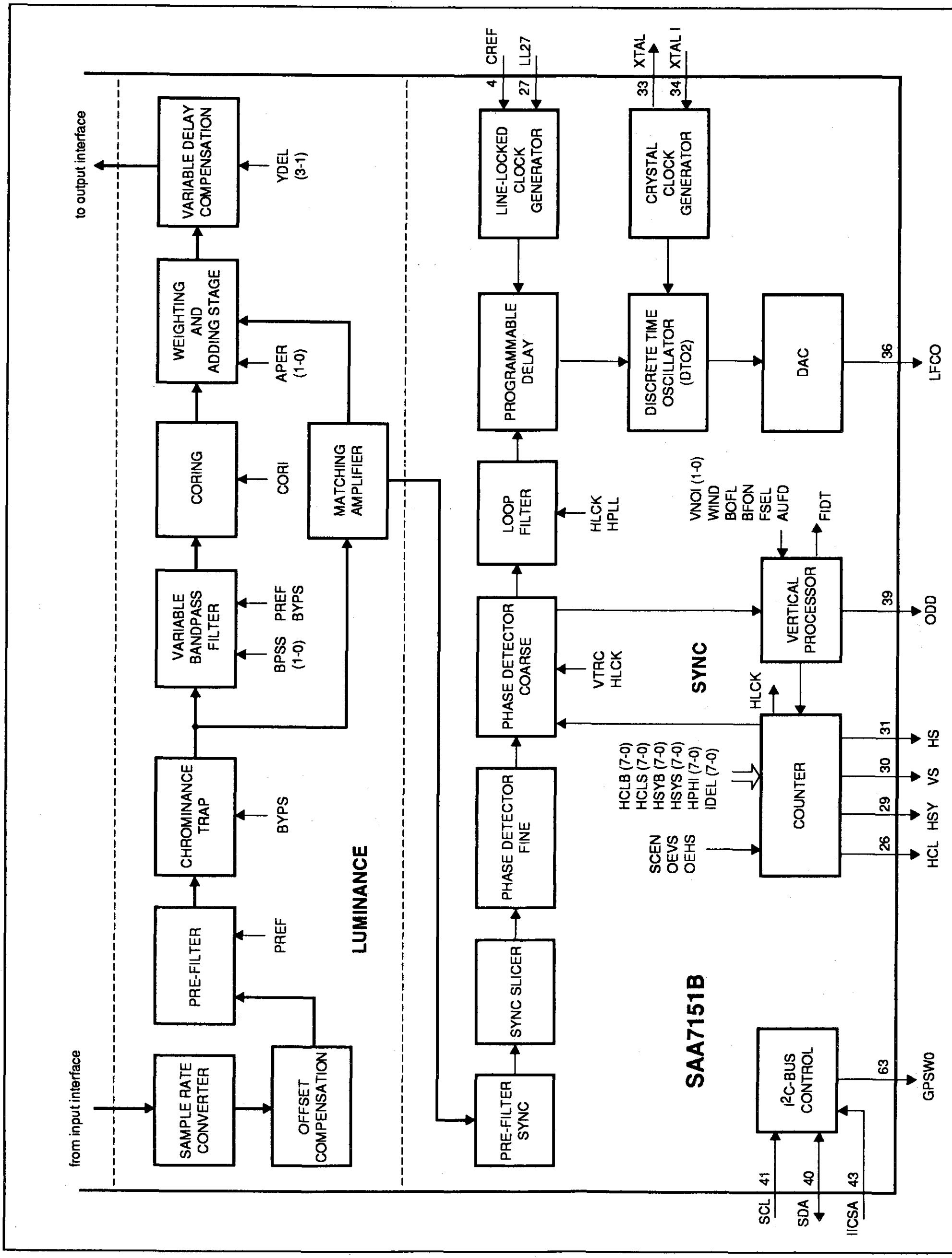

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Fig.4(b) Detailed block diagram; continued from Fig.4(a).

accumulate all phase deviations. There are three groups of output timing signals:

a. signals related to data output signals (HREF)
b. signals related to the input signals (HSY, and HCL)
c. signals related to the internal sync phase

All horizontal timings are derived from the main counter, which represents the internal sync phase. The HREF signal only with its critical timing is phase-compensated in relationship to the data output signal. Future circuit improvements could slightly influence the processing delays of some internal stages to achieve a changed timing due to the timing groups b and c.
The HREF signal only controls the data multiplexer phase and the data output signals.

All timings of the following diagrams are measured with nominal input signals, for example coming from a pattern generator. Processing delay times are taken between input and data output, respectively between internal sync reference (main counter = 0) and the rising edge of HREF.

Line locked clock frequency

LFCO is required in an external PLL (SAA7157) to generate the line-locked clock frequency LL27 and CREF.

YUV-bus, digital outputs

The 16-bit YUV-bus transfers digital data from the output interfaces to a feature box, or to the digital-to-analog converter (DAC). Outputs are controlled via the I²C-bus in normal selections, or they are controlled by output enable chain (FEIN, pin 64). The YUV-bus data rate 13.5 MHz. Timing is achieved by marking each second positive rising edge of the clock LL27 synchronized by CREF.

YUV-bus formats 4 : 2 : 2 and 4 : 1 : 1

The output signals Y7 to Y0 are the bits of the digital luminance signal. The output signals UV7 to UV0 are the bits of the digital colour-difference signal. The frames in the Tables 2 and 3 are the time to transfer a full set of samples. In case of 4 : 2 : 2 format two luminance samples are transmitted in comparision to one U and one V sample within one frame. The time frames are controlled by the HREF signal, which determines the correct UV data phase. The YUV data outputs can be enabled or set to 3-state position by means of the FEIN signal. FEIN = LOW enables the output; HIGH on this pin forces the Y and U/V outputs to a high-impedance state (Fig,5).

Table 2 for the 4 : 2 : 2 format (720 pixels per line). The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

OUTPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Table 3 for the 4 : 1 : 1 format (720 pixels per line). The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

OUTPUT	PIXEL BYTE SEQUENCE							
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7 (MSB)	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

Signal levels (Figures 11 and 12)

The nominal input and output signal levels are defined by a colour bar signal with 75 % colour, 100 % saturation and 100 % luminance amplitude (EBU colour bar).

CUV-bus input format

The CUV-bus transfers the digital chrominance/colour-difference signals from the ADC to the SAA7151B (Fig.5; Table 1):

- normal mode for digital chrominance transmission.
- UV colour-difference mode for colour-difference signals UV (out of matrixed RGB signals)
- FS mode (fast switch mode; UV inserted into chrominance signal C with addition of the two signal spectra).

RTCO output

The RTCO output signal (Fig.9) contains serialized information about actual clock frequency, subcarrier frequency and PAL/SECAM sequence. This signal may preferably be used with the frequency-locked digital video encoder SAA7199B.

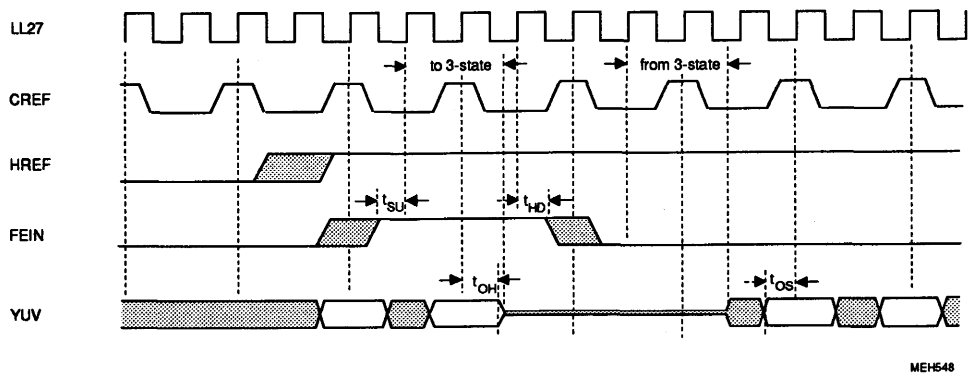


Fig.5 Timing example of fast enable input (FEIN).

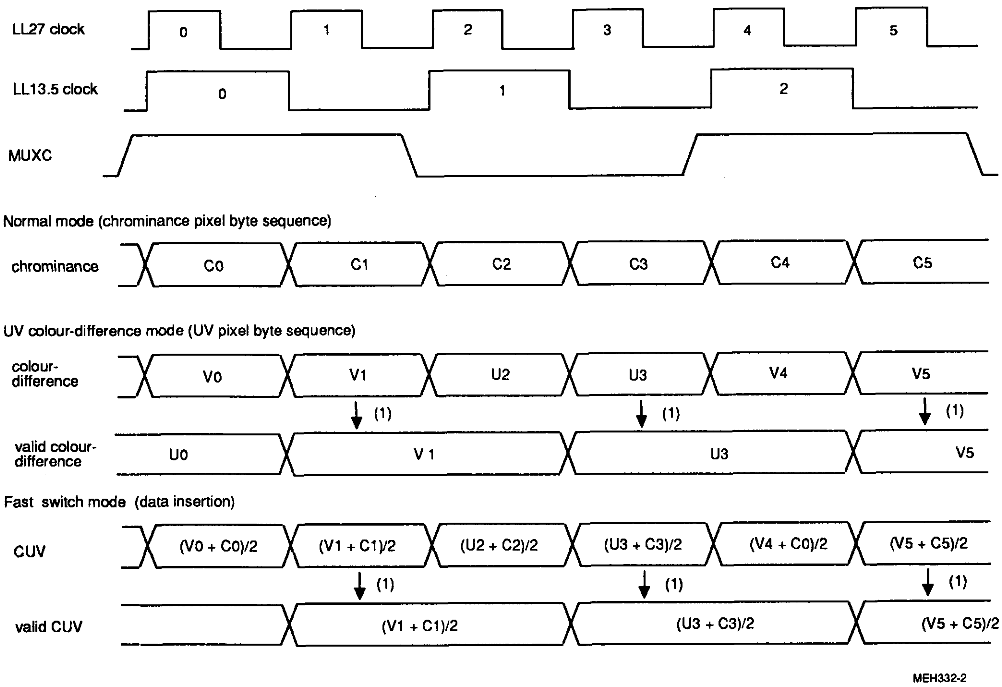


Fig.6 CUV input formats.
(1) each second sample only after a MUXC change is taken for down-sampling to 13.5 MHz to reduce cross-talk components between U and V signals.

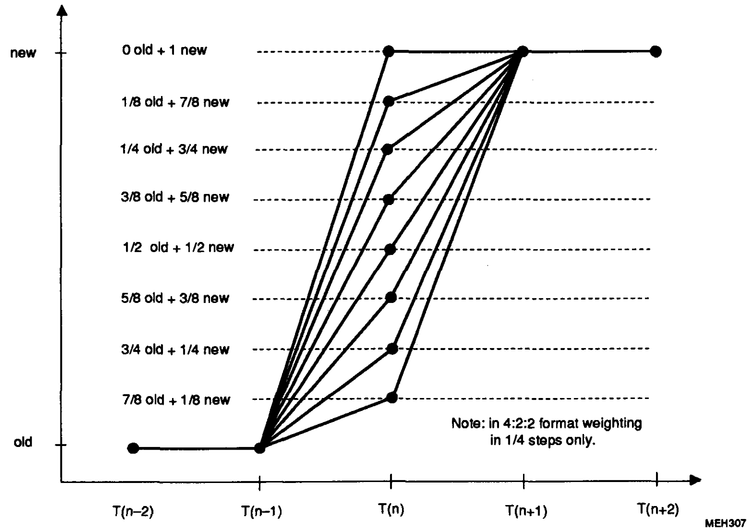


Fig.7 Addition of weighted components.

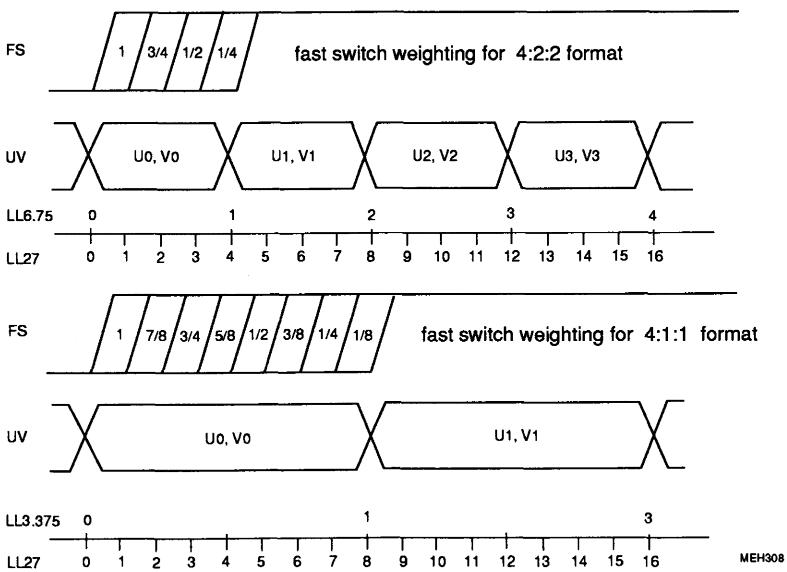


Fig.8 Weighting factors of fast switching for 4:2:2 and 4:1:1 formats.

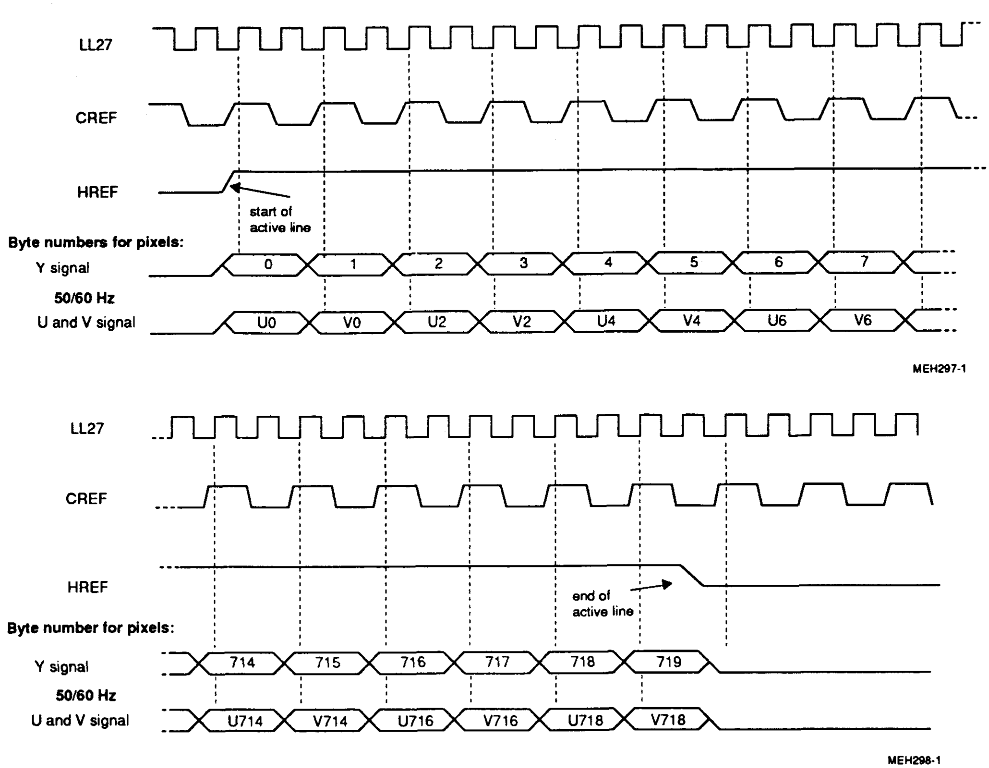
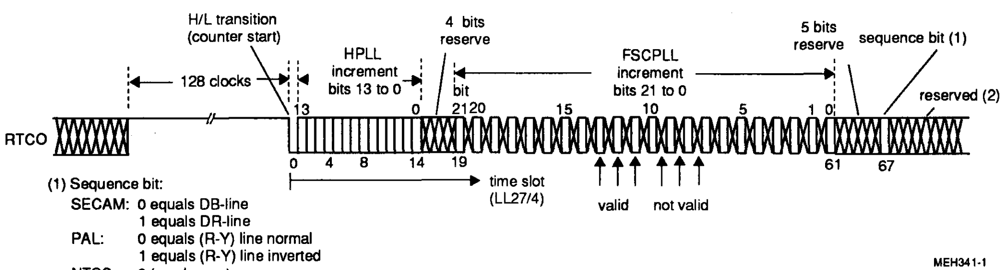


Fig.9 Line control by HREF in 4:2:2 format for 50 Hz and 60 Hz systems.



(1) Sequence bit:
SECAM: 0 equals DB-line
1 equals DR-line
PAL: 0 equals (R-Y) line normal
1 equals (R-Y) line inverted
NTSC: 0 (no change)
(2) Reserve bits: 236 for 50 Hz systems; 233 for 60 Hz systems.

Fig.10 RTCO timing.

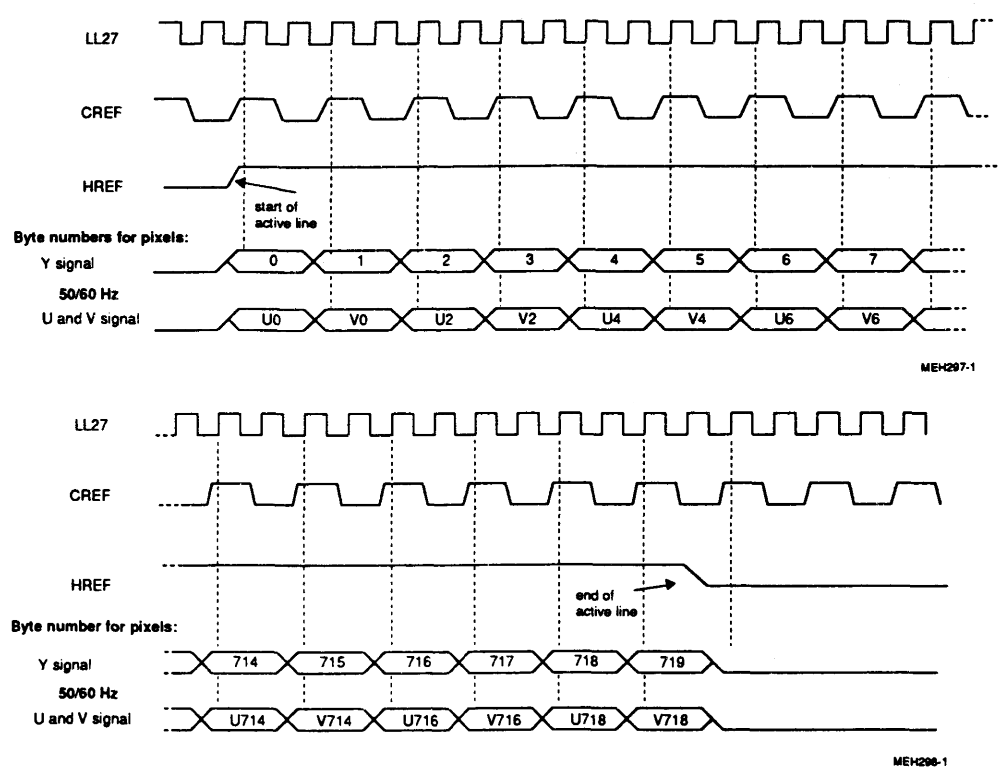
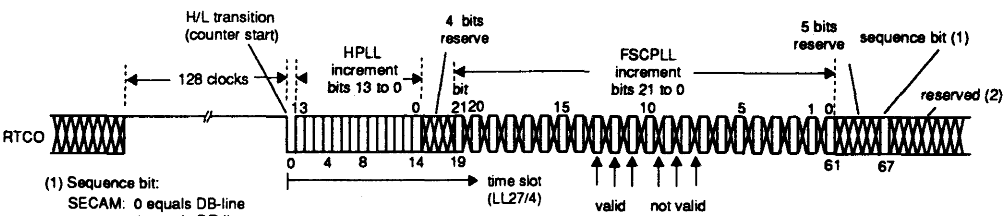


Fig.9 Line control by HREF in 4:2:2 format for 50 Hz and 60 Hz systems.



(1) Sequence bit:
SECAM: 0 equals DB-line
1 equals DR-line
PAL: 0 equals (R-Y) line normal
1 equals (R-Y) line inverted
NTSC: 0 (no change)

(2) Reserve bits: 236 for 50 Hz systems; 233 for 60 Hz systems.

MEH341-1

Fig.10 RTCO timing.

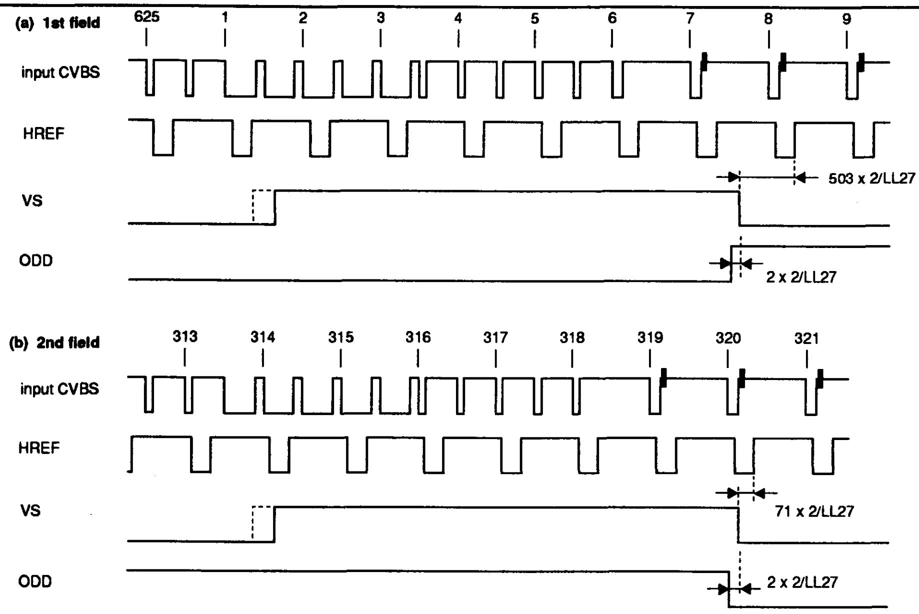


Fig.11(a) Vertical timing diagram at 50 Hz.

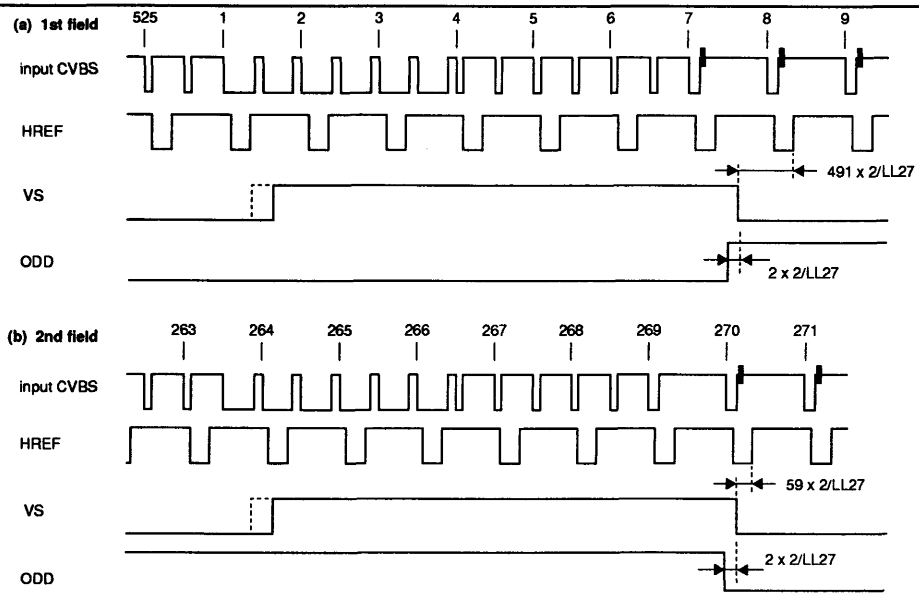
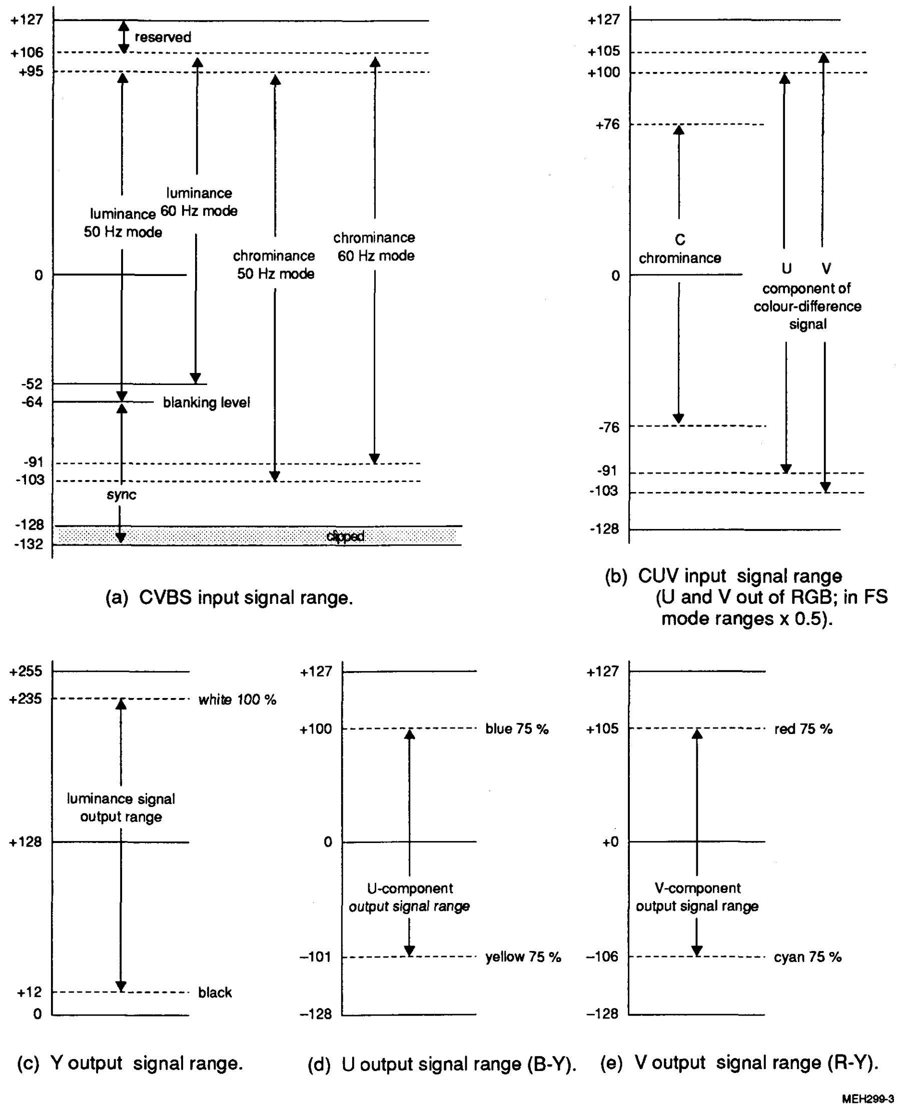
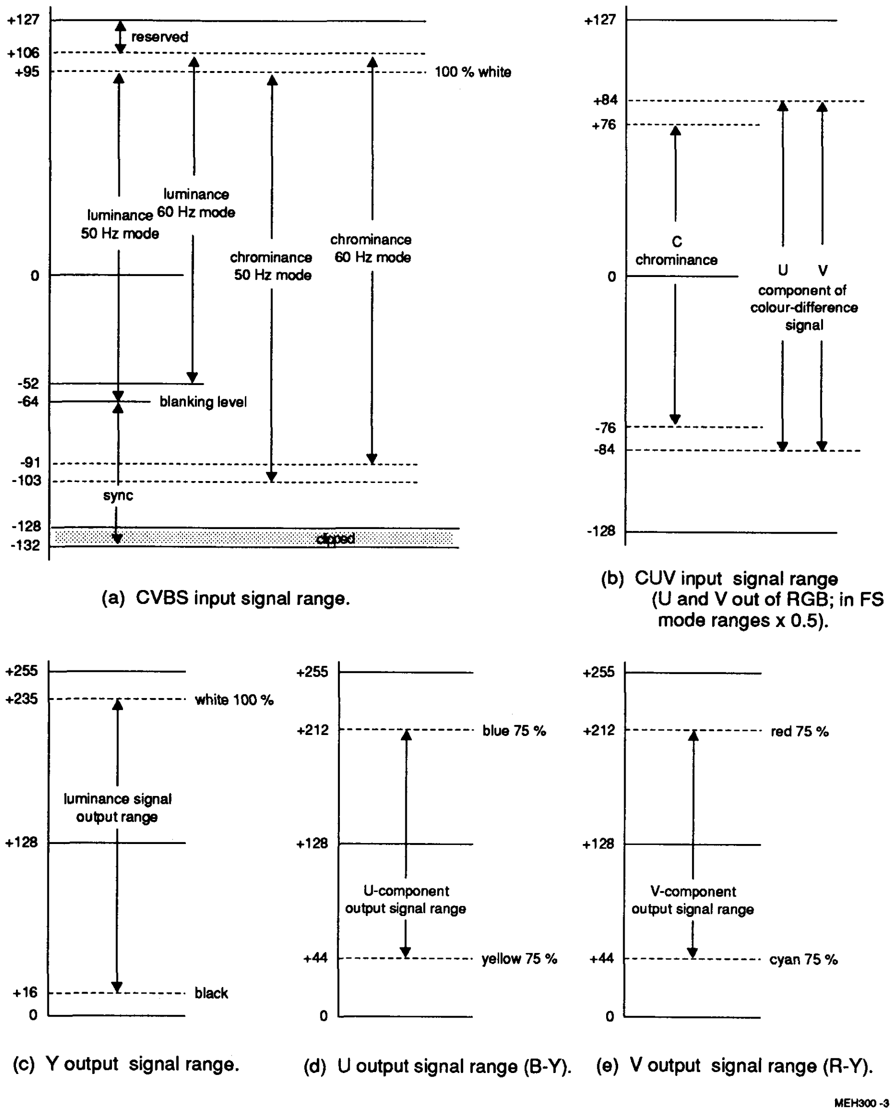


Fig.11(b) Vertical timing diagram at 60 Hz.



Notes: 1. All levels are related to EBU colour bar.
2. Values in decimal at 100 % luminance and 75 % chrominance amplitude.

Fig.12 Input and output signal ranges in DTV mode (digital TV).



Notes:
1. All levels are related to EBU colour bar.
2. Values in decimal at 100 % luminance and 75 % chrominance amplitude.
3. For SECAM input signals the CCIR levels will be exceeded.

Fig.13 Input and output signal ranges in CCIR mode.

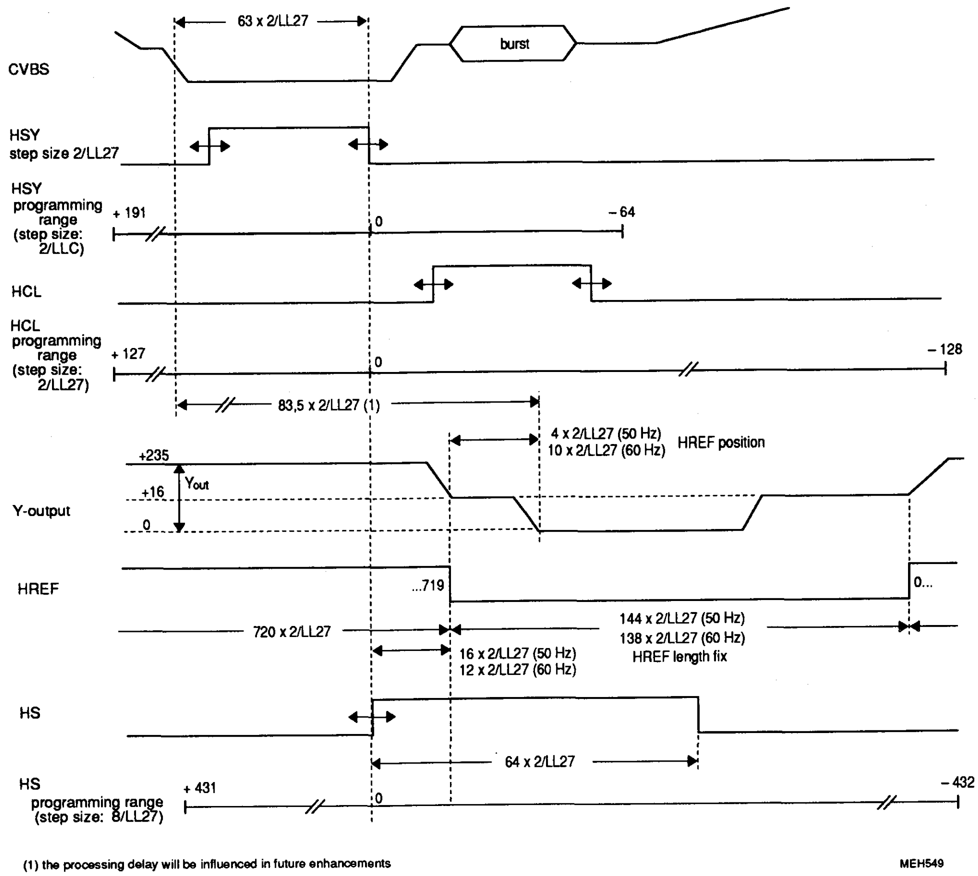


Fig.14 Horizontal sync and clamping timing for 50/60 Hz (signals HSY, HCL, HREF and HS).

8. LIMITING VALUES

In accordance with the Absolute Maximum Rating ystem (IEC 134); ground pins 19, 35, 38, 51 and 67 as well as supply pins 5, 18, 28, 37 and 52 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37, 52)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{SS\ A} - V_{SS(1\ to\ 4)}$	-	±100	mV
V_I	voltage on all inputs	−0.5	V_{DD}+0.5	V
V_O	voltage on all outputs ($I_{O\ max}$ = 20 mA)	−0.5	V_{DD}+0.5	V
P_{tot}	total power dissipation	-	2.5	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±2000	V

9. CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 18, 28, 37, 52)		4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37, 52)	V_{DD} = 5 V; inputs LOW; outputs not connected	-	100	250	mA
I²C-bus, SDA and SCL (pins 40 and 41)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3	-	V_{DD}+0.5	V
$I_{40,41}$	input current		-	-	±10	µA
I_{ACK}	output current on pin 40	acknowledge	3	-	-	mA
V_{OL}	output voltage at acknowledge	I_{40} = 3 mA	-	-	0.4	V
Data, clock and control inputs (pins 3, 4, 6 to 17, 20 to 23, 27, 34, 64 and 68); Figures 12 and 13						
V_{IL}	LL27 input voltage (pin 27)	LOW	−0.5	-	0.6	V
V_{IH}		HIGH	2.4	-	V_{DD}+0.5	V
V_{IL}	other input voltages	LOW	−0.5	-	0.8	V
V_{IH}		HIGH	2.0	-	V_{DD}+0.5	V
I_{leak}	input leakage current		-	-	10	µA
C_I	input capacitance	data inputs; note 1	-	-	8	pF
		I/O high-impedance	-	-	8	pF
		clock inputs	-	-	10	pF
$t_{SU.DAT}$	input data set-up time	Fig.15	11	-	-	ns
$t_{HD.DAT}$	input data hold time		3	-	-	ns

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.; inputs and outputs are protected against electrostatic discharge in normal handling. Normal precautions appropriate to handle MOS devices is recommended ("Handling MOS Devices").

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
YUV-bus, HREF and VS outputs (pins 30, 42, 45 to 50 and pins 53 to 62), Figures 9 and 12 to 13						
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitor		15	-	50	pF
LFCO output (pin 36)						
V_o	output signal (peak-to-peak value)	note 2	1.4	-	2.6	V
V_{36}	output voltage range		1	-	V_{DD}	V
Control outputs (pins 24 to 26, 29, 31, 32, 33, 39, 63, 65 and 66); Fig.11, 14 and 15						
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitor		7.5	-	25	pF
Timing of YUV-bus and control outputs		Figures 9 and 11				
t_{OH}	output signal hold time	YUV, HREF, VS at C_L = 15 pF;	13	-	-	ns
		controls at C_L = 7.5 pF	13	-	-	ns
t_{OS}	output set-up time	YUV, HREF, VS at C_L = 50 pF;	20	-	-	ns
		controls at C_L = 25 pF	20	-	-	ns
t_{SZ}	data output disable transition time	to 3-state condition	22	-	-	ns
t_{ZS}	data output enable transition time	from 3-state condition	20	-	-	ns
Chrominance PLL						
f_C	catching range		±400	-	-	Hz
Crystal oscillator		Figures 17 and 18; note 3				
f_n	nominal frequency	3rd harmonic	-	24.576	-	MHz
$\Delta f / f_n$	permissible deviation f_n		-	-	±50	10^{-6}
	temperature deviation from f_n		-	-	±20	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	-	70	°C
	load capacitance C_L		8	-	-	pF
	series resonance resistance R_S		-	40	80	Ω
	motional capacitance C_1		-	1.5±20%	-	fF
	parallel capacitance C_0		-	3.5±20%	-	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Line locked clock input LL27 (pin 27)		Fig.8 and 15				
t_{LL27}	cycle time	note 4	35	-	39	ns
t_p	duty factor	t_{LL27H}/t_{LL27}	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns

Notes to the characteristics

1. Data output signals are Y7 to Y0 and UV7 to UV0. All other are control output signals.
2. Levels are measured with load circuit. YUV-bus, HREF and VS outputs with 1.2 kΩ in parallel to 50 pF at 3 V (TTL load); LFCO output with 10 kΩ in parallel to 15 pF and other outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
3. Recommended crystal: Philips 4322 143 05291.
4. t_{SU}, t_{HD}, t_{OH} and t_{OD} include t_r and t_f.

Table 4 High-impedance control for YUV-bus (Fig.15)

OEDY	OEDC	FEIN	Y(7:0)	UV(7:0)
0	0	0	Z	Z
0	1	0	Z	active
1	0	0	active	Z
1	1	0	Z	Z
X	X	1	Z	Z

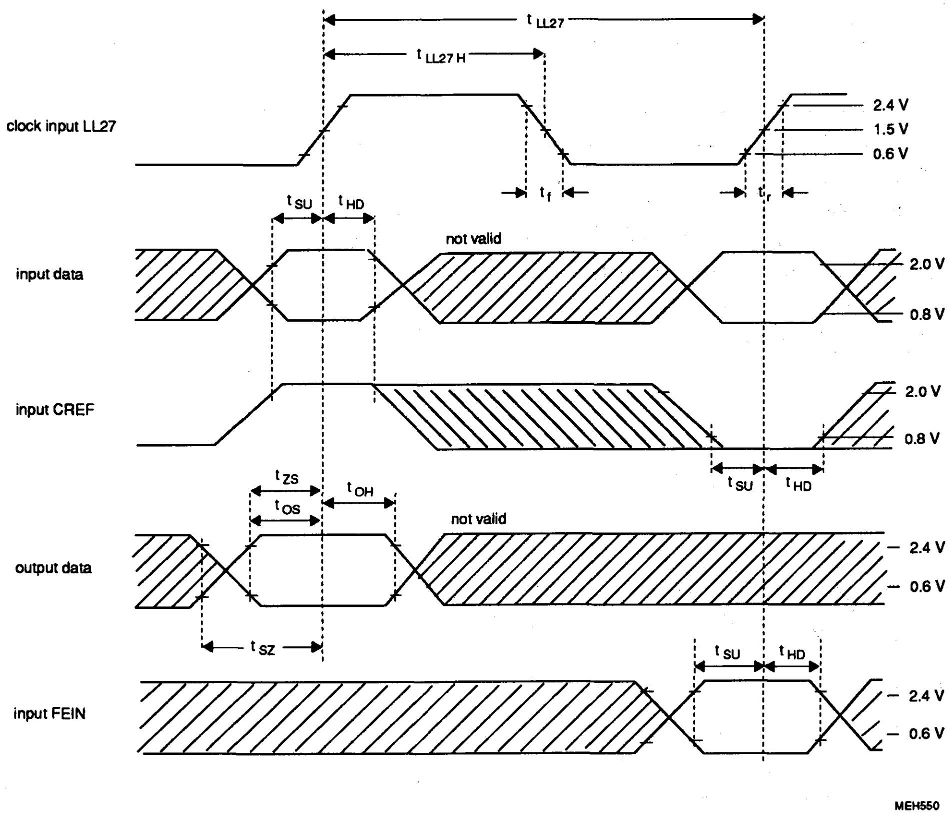


Fig.15 Data input and output timing diagram.

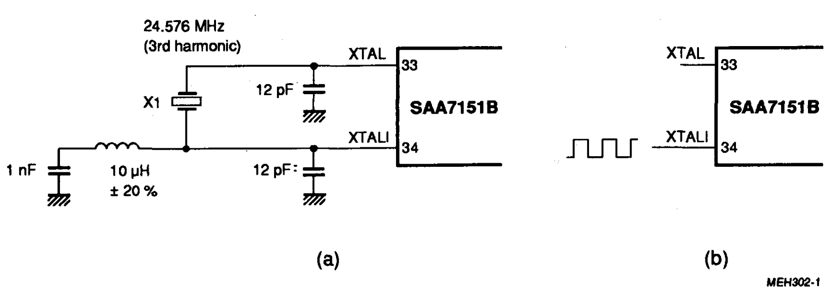


Fig.16 Oscillator application (a) and optional clock from external (b).

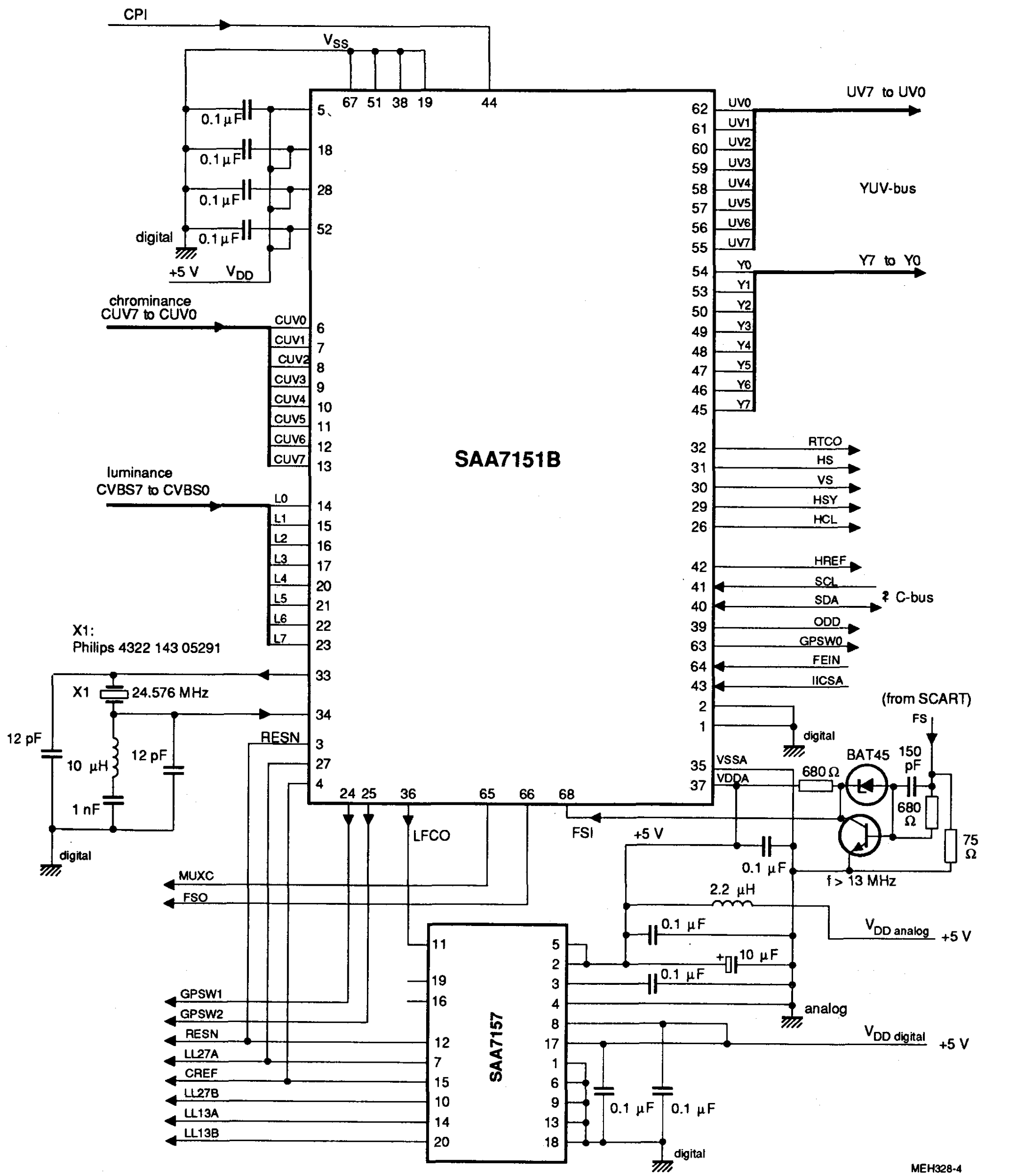


Fig.17 Application of SAA7151B.

Digital multistandard colour decoder with SCART interface (DMSD2-SCART)

SAA7151B

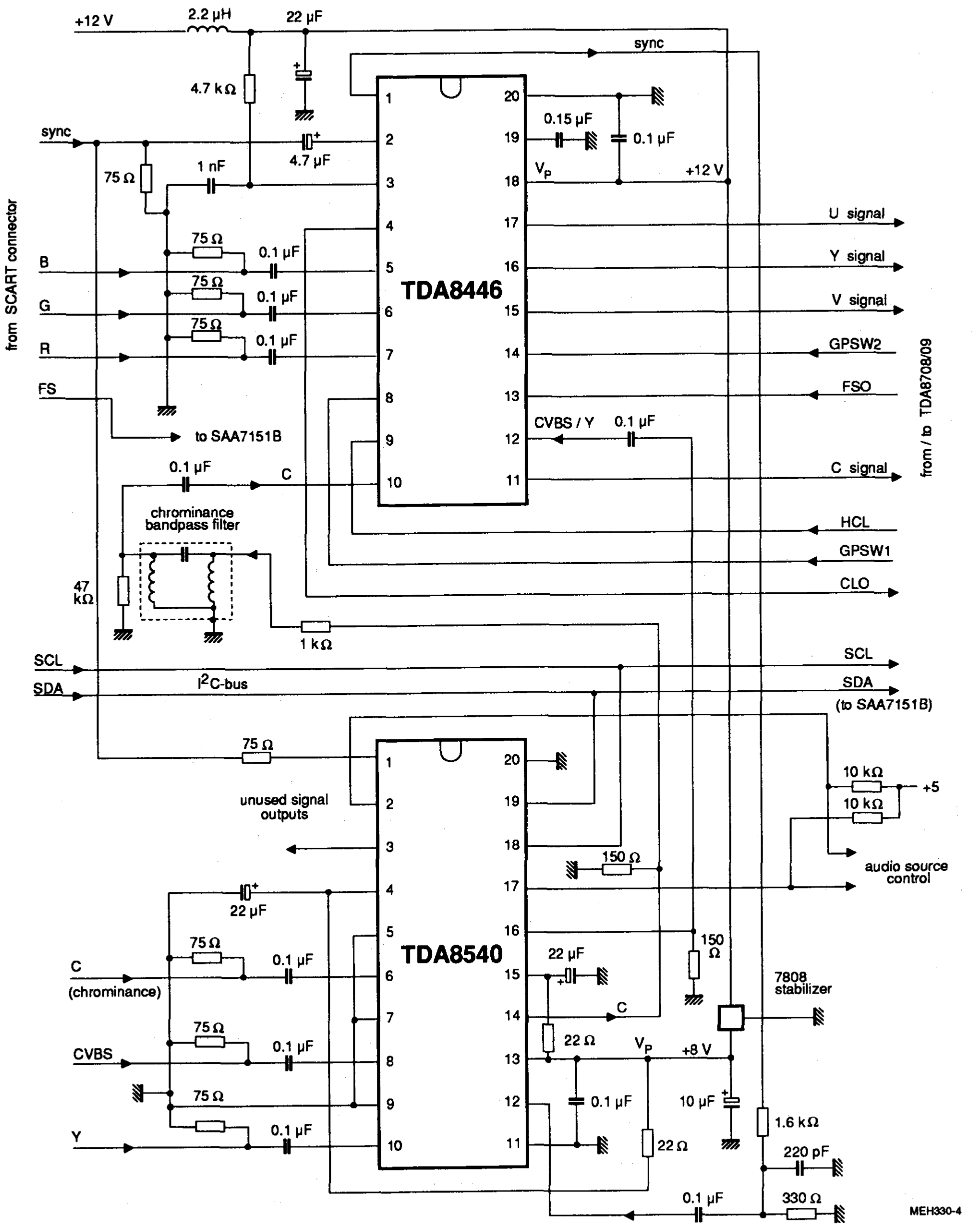


Fig.18 Application of input signal selecting (SCART interface).

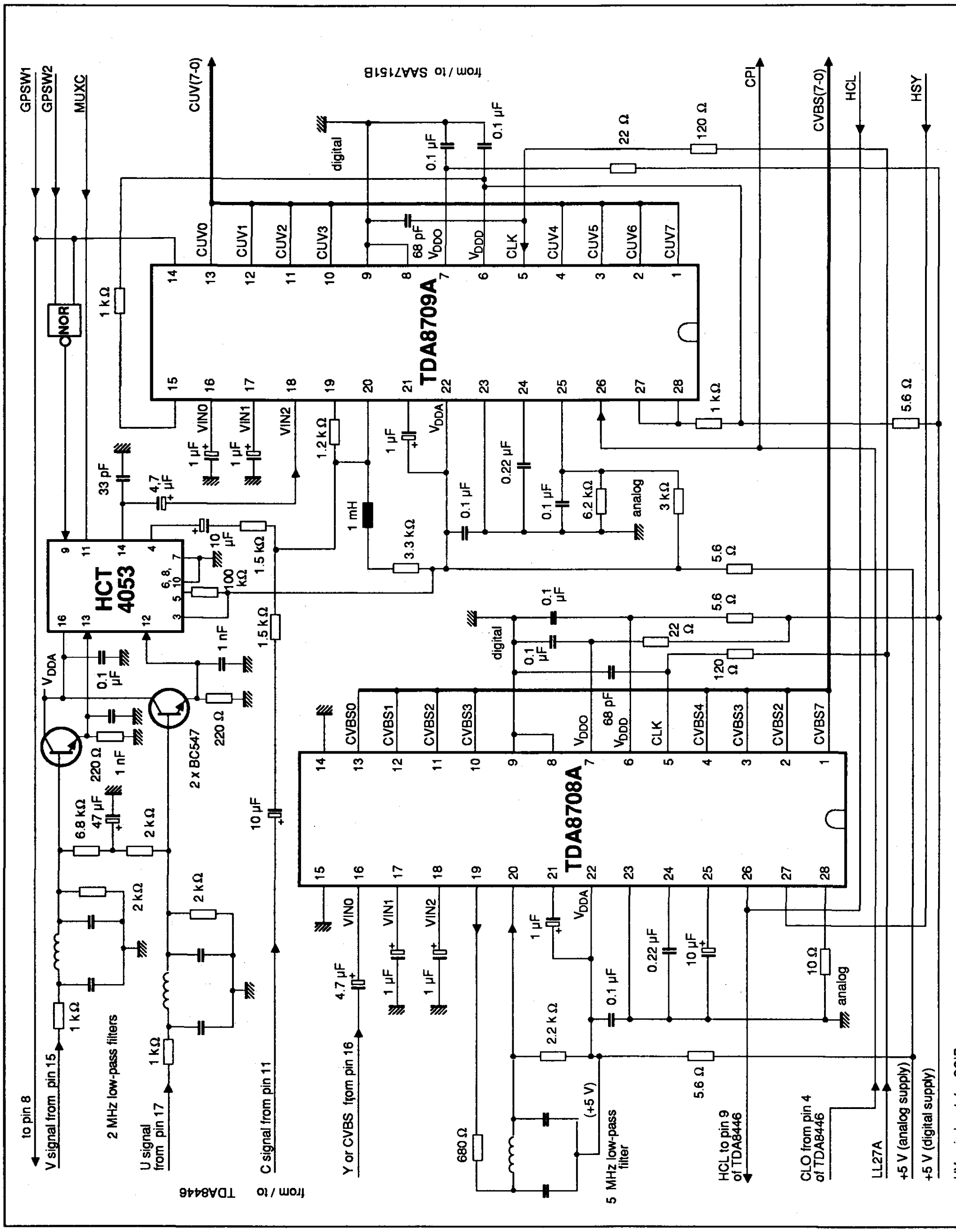


Fig.19 Application circuit analog-to-digital conversions.

10. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A	--------	DATAn	A	P

S = start condition
SLAVE ADDRESS = **1000 101X** (IICSA = LOW) **or 1000 111X** (IICSA = HIGH)
A = acknowledge, generated by the slave
SUBADDRESS* = subaddress byte (Table 5)
DATA = data byte (Table 5)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Remarks:
- Prior to reset of the IC all outputs are undefined.
- After power-on reset, the control register 12 (hex) is set to 00 (hex).

Table 5 I²C-bus; DATA for status byte (X in address byte = 1; slave address 8B (hex) at IICSA = LOW or 8F (hex) at IICSA = HIGH)

FUNCTION		DATA D7	D6	D5	D4	D3	D2	D1	D0
status byte		STTC	HLCK	FIDT	FSST1	FSST0	CDET2	CDET1	CDET0

Function of the bits:

STTC	Status time constant (to be used for gogical combfilter SAA7152)	0 = TV mode; 1 = VCR mode
HLCK	Horizontal PLL information:	0 = HPLL locked; 1 = HPLL unlocked
FIDT	Field information:	0 = 50 Hz system detected; 1 = 60 Hz system detected

FSST1 to FSST0 — Fast swiching output mode:

FSST1	FSST0	mode
0	0	RGB; FSI = HIGH (pin 68)
0	1	Y/C; FSI = LOW (pin 68)
1	0	fast switching (toggle)
1	1	not used

CDET2 to CDET0 — Identified colour standard

CDET2	CDET2	CDET2	standard
0	0	0	PAL-B/G, -H, -I; 50 Hz
0	0	1	PAL-N; 50 Hz
0	1	0	SECAM; 50 Hz
0	1	1	PAL-M; 60 Hz
1	0	0	PAL 4.43; 60 Hz
1	0	1	NTSC-M; 60 Hz
1	1	0	NTSC 4.43; 60 Hz
1	1	1	black/white

Table 6 I^2C-bus; subaddress and data bytes for writing (X in address byte = 0; slave address 8A (hex) at IICSA = LOW or 8E at IICSA = HIGH)

function	subaddress byte	data byte D7	D6	D5	D4	D3	D2	D1	D0
increment delay	00	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0
H-sync HSY begin	01	HSYB7	HSYB6	HSYB5	HSYB4	HSYB3	HSYB2	HSYB1	HSYB0
H-sync HSY stop	02	HSYS7	HSYS6	HSYS5	HSYS4	HSYS3	HSYS2	HSYS1	HSYS0
H-clamp HCL begin	03	HCLB7	HCLB6	HCLB5	HCLB4	HCLB3	HCLB2	HCLB1	HCLB0
H-clamp HCL stop	04	HCLS7	HCLS6	HCLS5	HCLS4	HCLS3	HCLS2	HCLS1	HCLS0
H-sync after PHI1	05	HPHI7	HPHI6	HPHI5	HPHI4	HPHI3	HPHI2	HPHI1	HPHI0
luminance control	06	BYPS	PREF	BPSS1	BPSS0	BFBY	CORI	APER1	APER0
hue control	07	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
miscellaneous controls #1	08	CSTD2	CSTD1	CSTD0	CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0
miscellaneous controls #2	09	OSCE	LFIS1	LFIS0	CKTS4	CKTS3	CKTS2	CKTS1	CKTS0
PAL switch sensitivity	0A	PLSE7	PLSE6	PLSE5	PLSE4	PLSE3	PLSE2	PLSE1	PLSE0
SECAM switch sensitivity	0B	SESE7	SESE6	SESE5	SESE4	SESE3	SESE2	SESE1	SESE0
miscellaneous controls #3	0C	FSAU	GPSI2	GPSI1	CGFX	AMPF3	AMPF2	AMPF1	AMPF0
miscellaneous controls #4	0D	COLO	CHSB	GPSW0	SUVI	SXCR	FSDL2	FSDL1	FSDL0
miscellaneous controls #5	0E	CCIR	COFF	OEHS	OEVS	UVSS	CHRS	CDMO	CDPO
miscellaneous controls #6	0F	AUFD	FSEL	HPLL	SCEN	VTRC	MUIV	FSIV	WIND
miscellaneous controls #7	10	ASTD	OFTS	IPBP	CDVI	YDEL3	YDEL2	YDEL1	YDEL0
chroma gain reference	11	CHCV7	CHCV6	CHCV5	CHCV4	CHCV3	CHCV2	CHCV1	CHCV0
miscellaneous controls #8	12	OEDY	OEDC	VNOI1	VNOI0	BFON	BOFL2	BOFL1	BOFL0

Function of the bits of Table 6

IDEL7 to IDEL0 "00"

Increment delay time , step size = 4/LL27 = 148 ns*

D7 D6 D5 D4	D3 D2 D1 D0	decimal multiplier	note
1 1 1 1	1 1 1 1	–1 to –110	minimum –148 ns
1 0 0 1	0 0 1 0		–16.3 μs (outside available range)
1 0 0 1	0 0 0 1	–111 to –214	–16.44 μs
0 0 1 0	1 0 1 0		–31.7 μs (maximum value at FSEL = 1)
0 0 1 0	1 0 0 1	–215	–31.85 μs (outside central counter range at FSEL = 1 **)
0 0 1 0	1 0 0 0	–216	–32.0 μs (maximum value at FSEL = 0 **)
0 0 1 0	0 1 1 1	–217 to –256	–32.148 μs (outside central counter range at FSEL = 0 **)
0 0 0 0	0 0 0 0		–37.9 μs (outside central counter **)

* an internal sign-bit D8 set to HIGH indicates that all values are always negative

** H-PLL does not operate in this condition; the system clock frequency is set to a value fixed by the last update and is within ±7.1 % of the nominal frequency.

HSYB7 to HSYB0 HSYS7 to HSYS0 "01" and "02"	Horizontal sync begin, step size = 2/LL27 = 74 ns Horizontal sync stop, step size = 2/LL27 = 74 ns

D7 D6 D5 D4	D3 D2 D1 D0	decimal multiplier	note
1 0 1 1	1 1 1 1	191 to 1	−14.2 μs (maximum negative value)
0 0 0 0	0 0 0 1		−74 ns
0 0 0 0	0 0 0 0	0	0 equals reference value
1 1 1 1	1 1 1 1	−1 to −64	+74 ns
1 1 0 0	0 0 0 0		+4.7 μs

HCLB7 to HCLB0 HCLS7 to HCLS0 "03" and "04"	Horizontal clamp begin, step size = 2/LL27 = 74 ns Horizontal clamp stop, step size = 2/LL27 = 74 ns

D7 D6 D5 D4	D3 D2 D1 D0	decimal multiplier	note
0 1 1 1	1 1 1 1	127 to 1	−9.4 μs (maximum negative value)
0 0 0 0	0 0 0 1		−74 ns
0 0 0 0	0 0 0 0	0	0 equals reference value
1 1 1 1	1 1 1 1	−1 to −128	+74 ns
1 0 0 0	0 0 0 0		+9.5 μs (maximum positive value)

HPHI7 to HPHI0 "05"	Horizontal sync start, step size = 8/LL27 = 296 ns

D7 D6 D5 D4	D3 D2 D1 D0	decimal multiplier	note
0 1 1 1 0 1 1 0	1 1 1 1 1 1 0 1	+127 to +109	) forbidden (outside available central) counter range)
0 1 1 0	1 1 0 0	+108 to +1	−32 μs (maximum negative value)
0 0 0 0	0 0 0 1		−0.296 ns
0 0 0 0	0 0 0 0	0	0 equals reference value
1 1 1 1 1 0 0 1	1 1 1 1 0 1 0 1	−1 to −107	+0.296 μs +31.7 μs (maximum positive value)
1 0 0 1 1 0 0 0	0 1 0 0 0 0 0 0	−108 to −128	) forbidden (outside available central) counter range)

BYPS "06"	Input mode select bit: 0 = CVBS mode (chroma trap active) 1 = S-Video mode (chroma trap by-passed)
PREF	Use of pre-emphasis (to be used if chrominance trap is active): 0 = pre-filter bypassed; 1 = pre-filter on
BPSS1 to BPSS0	Aperture bandpass to select different centre frequencies (Figures 23 to 38):

BPSS1	BPSS0	centre frequency
0	0	4.1 MHz
0	1	3.8 MHz
1	0	2.6 MHz
1	1	2.9 MHz

"06" continued	
BFBY	Bandfilter bypass switching: 0 = bandfilter active; 1 = bandfilter bypassed
CORI	Coring function: 0 = coring off; 1 = ±1 LSB coring
APER1 to APER0	Aperture factor (Figures 23 to 38):

APER1	APER0	factor
0	0	0
0	1	0.25
1	0	0.5
1	1	1

HUE7 to HUE0 "07"	Hue control from +178.6° to −180.0°, equals data bytes 7F to 80 (hex); 0° equals 00.
CSTD2 to CSTD0 "08"	Forced colour standard of input signal;

CSTD2	CSTD1	CSTD0	standard
0	0	0	PAL-B/G, -H, -I; 50 Hz
0	0	1	PAL-N; 50 Hz
0	1	0	SECAM; 50 Hz
0	1	1	PAL-M; 60 Hz
1	0	0	PAL 4.43; 60 Hz
1	0	1	NTSC-M; 60 Hz
1	1	0	NTSC 4.43; 60 Hz
1	1	1	black/white

CKTQ4 to CKTQ0	Colour killer threshold QAM (PAL/NTSC):

CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0	
1	1	1	1	1	
1	0	0	0	0	approximately −30 to −24 dB
0	0	0	0	0	−24 dB to −18 dB

OSCE "09"	External UV offset compensation: 0 = disabled; 1 = enabled
LFIS1 to LFIS0	Chrominance gain control (AGC filter):

LFIS1	LFIS0	control of loop filter time constant
0	0	slow
0	1	medium
1	0	fast
1	1	actual gain, stored (for test purposes only)

CKTS4 to CKTS0	Colour killer threshold SECAM as previously described under CKTQ subaddress"08"

PLSE7 to PLSE0 "0A"	PAL switch sensitivity from LOW to HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.
SESE7 to SESE0 "0B"	SECAM switch sensitivity from LOW to HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.
FSAU; GPSI2, and GPSI1 "0C"	Set port outputs (general purpose switching, internal)
CGFX	Chrominance gain pre-determination: 0 = gain controlled via loop; 1 = gain set by AMPF-bits
AMPF3 to AMPF0	Chrominance amplification factor

FSAU	GPSI2	GPSI1	output GPSW2 (pin 25)	output GPSW1 (pin 24)
0	0	0	LOW	LOW
0	0	1	LOW	HIGH
0	1	0	HIGH	LOW
0	1	1	HIGH	HIGH
1	X	X	status bit FSST1 set	status bit FSST0 set

AMPF3	AMPF2	AMPF1	AMPF0	gain
0	0	0	0	–6 dB
0	1	0	0	0 dB
0	1	0	1	+1.5 dB
.	.	.	.	+3 to +16.5 dB (approximately 1.5 dB steps)
1	1	1	1	+17 dB

COLO "0D"	Colour-on bit:	0 = colour-killer automatically enabled ; 1 = forced colour-on.
CHSB	Chrominance (UV) output code:	0 = two's complement; 1 = straightly binary
GPSW0	General purpose port output (pin 63):	0 = LOW; 1 = HIGH
SUVI	SECAM UV output signal polarity:	0 = U and V positive; 1 = U and V negative
SXCR	SECAM cross-colour reduction:	0 = off; 1 = on
FDSL2 to FDSL0	Fast switching delay adjustment in 37 ns steps:	

FDSL2	FDSL1	FDSL0	delay
0	0	0	0
0	0	1	37 ns
0	1	0	74 ns
0	1	1	111 ns
1	0	0	–148 ns (negative delay)
1	0	1	–111 ns
1	1	0	–74 ns
1	1	1	–37 ns

CCIR "0E"	Set CCIR mode: 0 = digital TV mode (DTV); 1 = CCIR mode
COFF	Set colour off: 0 = colour on; 1 = colour off
OEHS	Enable horizontal sync outputs HS and HREF: 0 = output high-impedance; 1 = HS and HREF enabled
OEVS	Enable vertical sync output VS: 0 = output high-impedance; 1 = VS enabled
UVSS	Select UV pixel sample: 1 = first pixel after U/V signal has changed; 0 = second pixel (free of crosstalk signals)
CHRS	S-Video input mode: 0 = chrominance signal from CVBS or CUV input and controlled by BYPS (subaddress 06); 1 = S-Video mode; chrominance signal from CUV input
CDMO, CDPO	Chrominance delay: see table below

Chrominance delay:

CDMO	CDPO	
0	0	no delay
1	X	–37 ns (negative delay)
0	1	+37 ns

AUFD "0F"	Automatical field detection: 0 = field selection by FSEL-bit; 1 = automatical field detection
FSEL	Field select (AUFD-bit = 0): 0 = 50 Hz (625 lines); 1 = 60 Hz (525 lines)
HPLL	Horizontal PLL: 0 = PLL closed; 1 = PLL open, horizontal frequency fixed
SCEN	Sync and clamping pulse enable: 0 = HCL and HSY outputs HIGH (pins 26 and 29); 1 = HCL and HSY outputs active.
VTRC	VTR/TV mode select: 0 = TV mode (slow time constant); 1 = VTR mode (fast time constant).
MUIV	MUXC signal invertion: 0 = inverted; 1 = not inverted
FSIV	Fast switch input signal inversion: 0 = not inverted; 1 = inverted
WIND	Narrow fast switch window : 0 = off; 1 = on
ASTD "10"	Automatic standard switching: 0 = off; 1 = on
OFTS	Select output format: 0 = 4 : 1 : 1 format; 1 = 4 : 2 : 2 format.
IPBP	External UV signal interpolation filter: 0 = active; 1 = bypassed
CDVI	Chrominance PLL filter selection for: 0 = VTR or TV source; 1 = fast time constant for FSC-PLL (only for special applications)
YDEL3 to YDEL0	Luminance delay compensation in 37 ns steps: see table below

Luminance delay compensation in 37 ns steps:

YDEL3	YDEL2	YDEL1	YDEL0	delay
0	0	0	0	) 0 to 259 ns (step 0 to 7)
0	1	1	1	)
1	0	0	0	) –296 to –37 ns (negative delay; step –8 to –1)
1	1	1	1	)

CHCV7 to CHCV0 "11"

Chroma gain reference value

D7	D6	D5	D4	D3	D2	D1	D0	gain	
1	1	1	1	1	1	1	1	maximum gain	
	:				:			to	)
1	0	1	1	0	0	1	1	DTV level	) default programmed values
	:				:			to	) dependend on application
0	0	1	1	1	1	0	1	CCIR level	)
	:				:			to	)
0	0	0	0	0	0	0	0	minimum gain	

OEDY "12"

Enable Y signals on YUV-bus: 0 = output high-impedance; 1 = output active (dependent on FEIN)

OEDC

Enable UV signals on YUV-bus: 0 = output high-impedance; 1 = output active ((dependent on FEIN)

VNOI1, VNOI0

Vertical noise reduction mode:

VNOI1	VNOI0	mode
0	0	normal
0	1	searching
1	0	free-running
1	1	bypassed

BFON

Bottom flutter compensation switching: 0 = off; 1 = on (controlled by BOFL-bit)

BOFL2 to BOFL0

Bottom flutter compensation

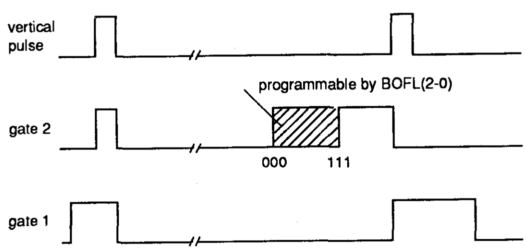
BOFL2	BOFL1	BOFL0	start at line number
0	0	0	297 for PAL (247 for NTSC; active to end of field)
0	0	1	298 for PAL (248 for NTSC; active to end of field)
.	.	.	. .
1	1	0	303 for PAL (253 for NTSC; active to end of field)
1	1	1	304 for PAL (254 for NTSC; active to end of field)

The bottom flutter circuit is able to compensate for horizontal phase jump of up to ±16 µs.

Note: The bottom flutter gate is active at

- HPLL is locked
- HPLL in VTR mode
- the vertical noise limiter (VNL) is in the VTR mode
- gating is switched by BFON-bit = 1 (subaddress 12)

Gate 2	Gate 1	HPLL function
0	0	normal
1	0	disabled
0	1	double speed
1	1	unused



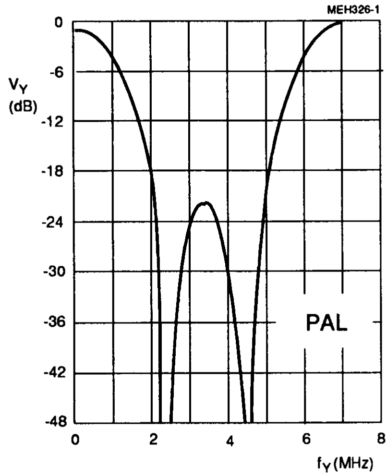


Fig.20 Frequency response of chroma stop filter in colour-difference mode for 50 Hz PAL. Filter is only active in fast switching mode, but bypassed in RGB mode. The selected filter is dependent on actual detected colour standard.

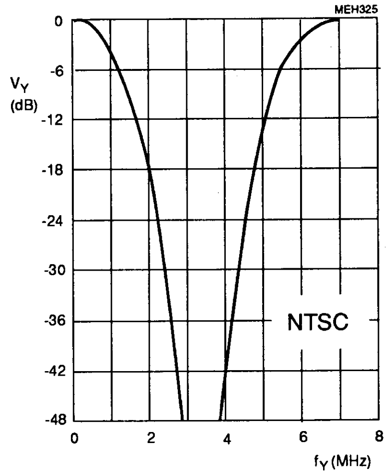


Fig.21 Frequency response of chroma stop filter in colour-difference mode for 60 Hz NTSC. Filter is only active in fast switching mode, but bypassed in RGB mode. The selected filter is dependent on actual detected colour standard.

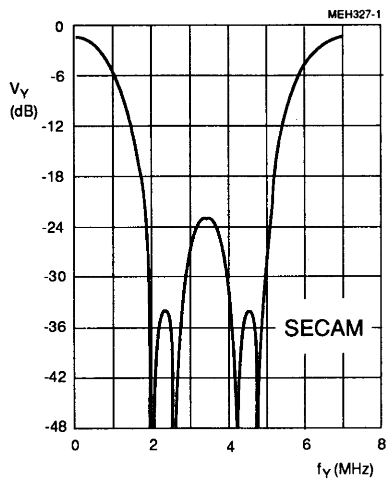


Fig.22 Frequency response of chroma stop filter in colour-difference mode for 50 Hz SECAM. Filter is only active in fast switching mode, but bypassed in RGB mode. The selected filter is dependent on actual detected colour standard.

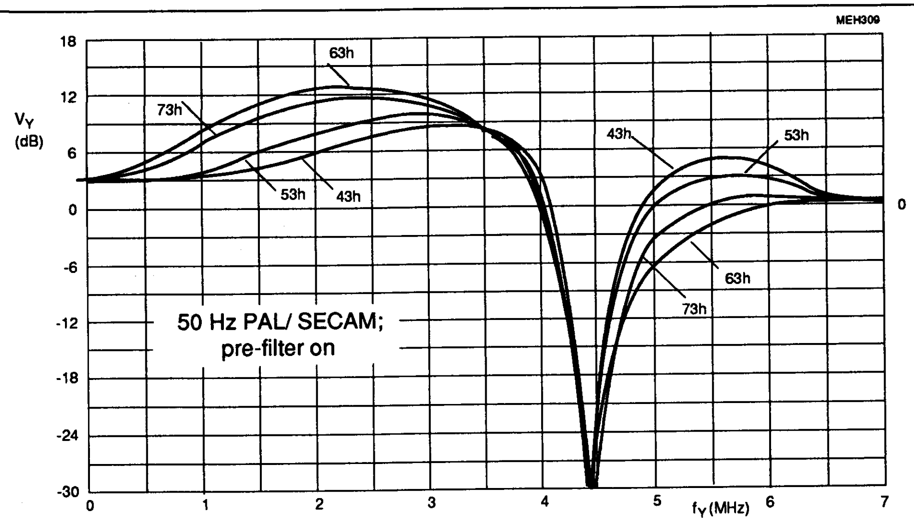


Fig.23 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter on ; and bandfilter on.

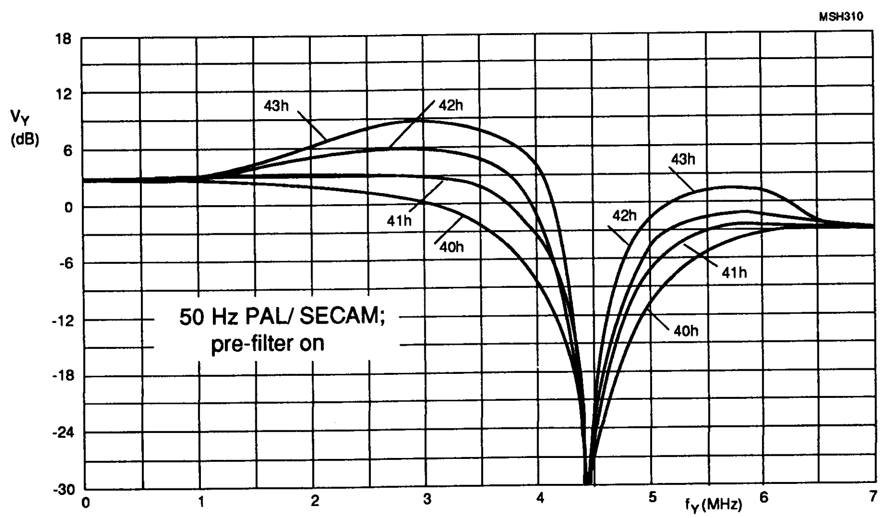


Fig.24 3.8 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter on and bandfilter on.

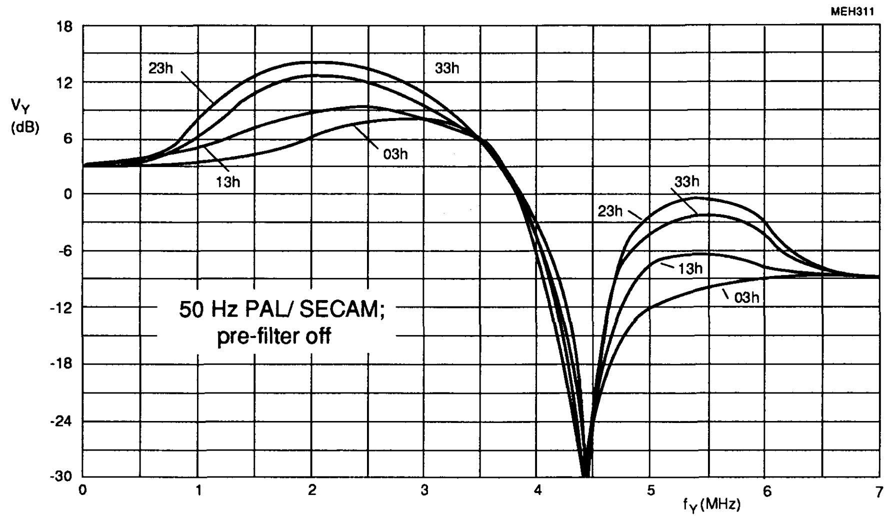


Fig.25 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter off ; and bandfilter on.

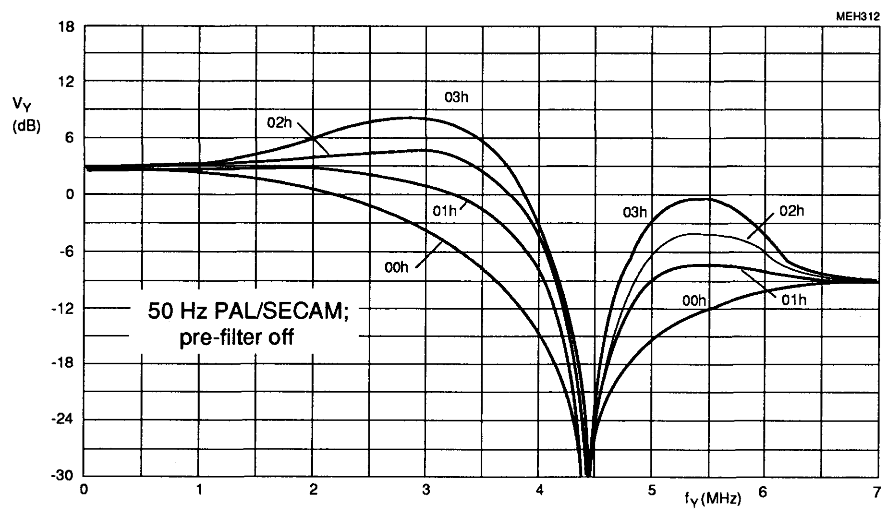


Fig.26 4.1 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter off and bandfilter on.

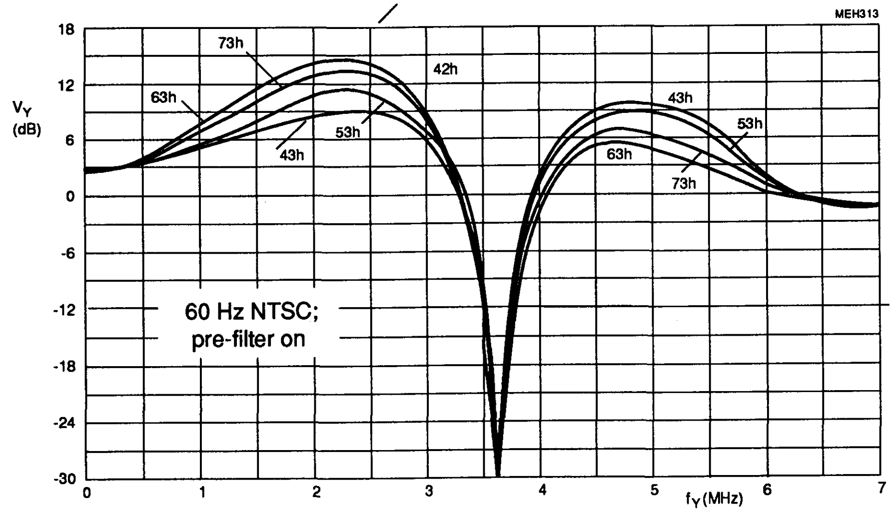


Fig.27 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter on ; and bandfilter on.

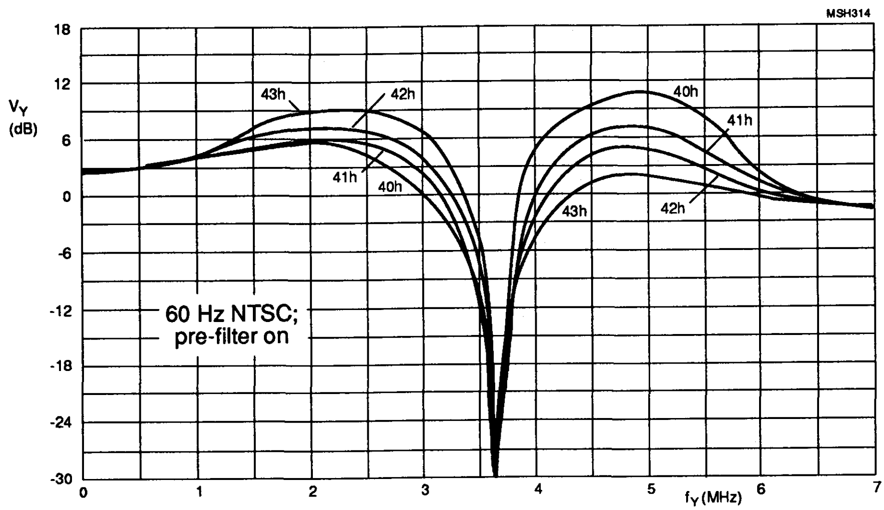


Fig.28 3.8 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter on and bandfilter on.

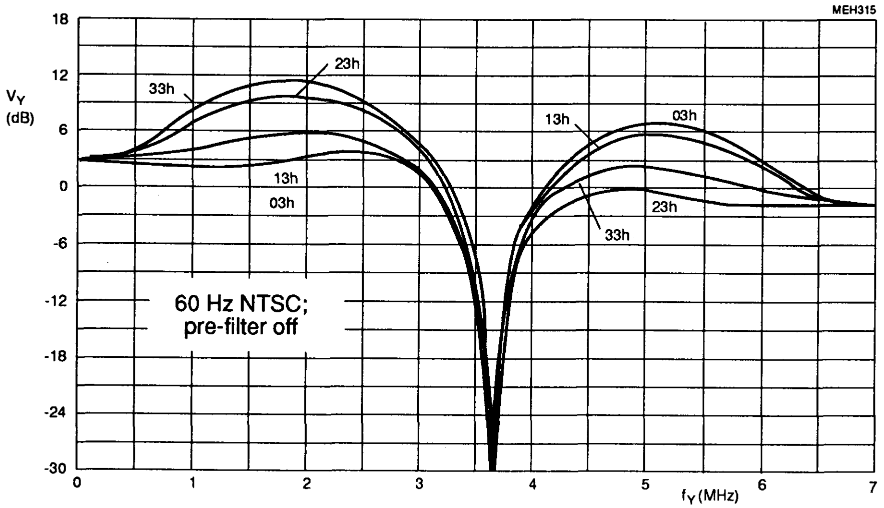


Fig.29 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter off ; and bandfilter on.

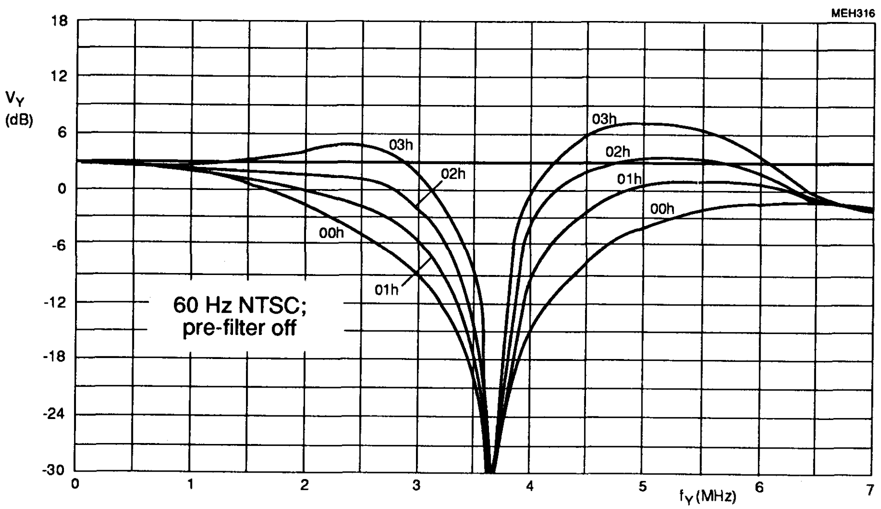


Fig.30 4.1 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter off and bandfilter on.

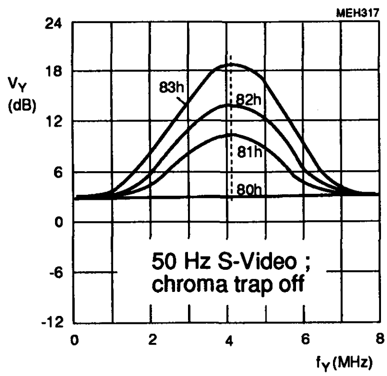


Fig.31 4.1 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

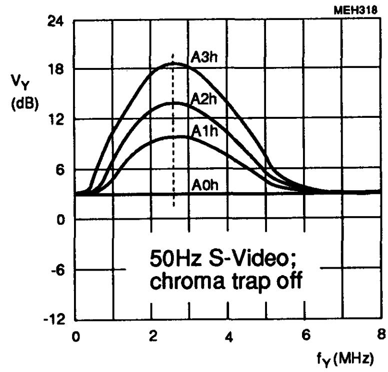


Fig.32 2.6 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

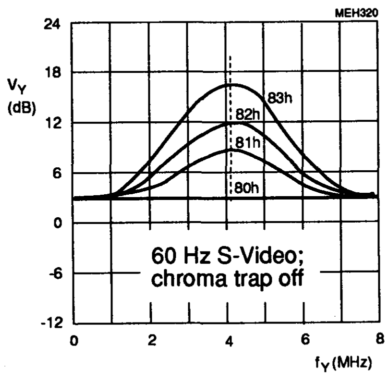


Fig.33 4.1 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

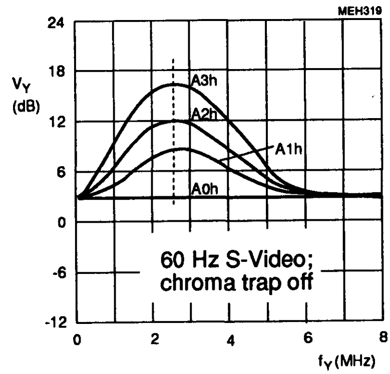


Fig.34 2.6 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

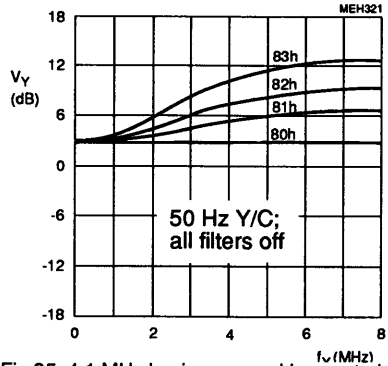


Fig.35 4.1 MHz luminance peaking control in 50 Hz / S-VHS mode as a function of four different aperture factors controllable by subaddress byte 06.

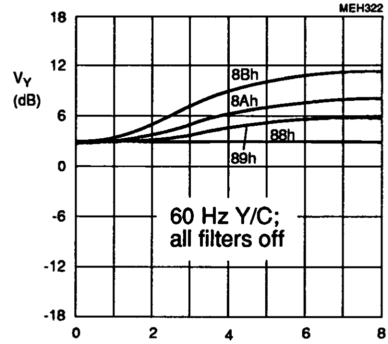


Fig.36 4.1 MHz luminance peaking control in 60 Hz / S-VHS mode as a function of four different aperture factors controllable by subaddress byte 06.

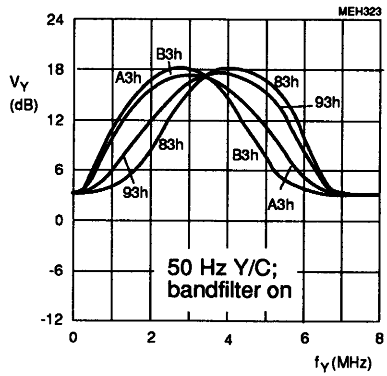


Fig.37 Maximum luminance peaking control in 50 Hz / S-VHS mode as a function of four aperture centre frequencies controllable by subaddress byte 06.

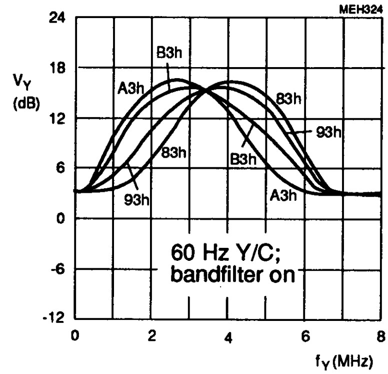


Fig.38 Maximum luminance peaking control in 60 Hz / S-VHS mode as a function of four aperture centre frequencies controllable by subaddress byte 06.

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

11. PROGRAMMING EXAMPLE

Coefficients to set operation for application circuits Figures 17, 18 and 19. Values recommended for PAL CVBS input signal and 4:2:2 CCIR output signal (all numbers of the Table 6 are hex values).

Table 7 Recommended default values (note 1)

SUBADDRESS	BIT NAME	FUNCTION	VALUE (HEX)
00	IDEL(7-0)	increment delay	4D
01	HSYB(7-0)	horizontal sync HSY begin	3D
02	HSYS(7-0)	horizontal sync HSY stop	0D
03	HCLB(7-0)	horizontal clamping HCL begin	F3
04	HCLS(7-0)	horizontal clamping HCL stop	C6
05	HPHI(7-0)	horizontal sync after PHI1	FB
06	BYPS, PREF, BPSS(1-0) BFBY, CORI, APER(1-0)	luminance bandwidth control:	02 (note 2)
07	HUEC(7-0)	hue control (0 degree)	00
08	CSTD(2-0), CKTQ(4-0)	miscellanous controls #1	09
09	OSCE, LFIS(1-0),CKTS(4-0)	miscellanous controls #2	C0
0A	PLSE(7-0)	PAL switch sensitivity	4D
0B	SESE(7-0)	SECAM switch sensitivity	40
0C	FSAU, GPSI(2-1), CGFX, AMPF(3-0)	miscellanous controls #3	80
0D	COLO, CHSB, GPSW0, SUVI, SXCR, FSDL(2-0)	miscellanous controls #4	60
0E	CCIR, COEF, OEHS, OEVS UVSS, CHRS, CDMO, CDPO	miscellanous controls #5	B4
0F	AUFD, FSEL, HPLL, SCEN, VTRC, MUIV, FSIV, WIND	miscellanous controls #6	9F
10	ASTD, OFTS, IPBP, CDVI, YDEL(3-0)	miscellanous controls #7	C0
11	CHCV(7-0)	nominal chrominance gain	4F
12	OEDY, OEDC, VNOI(1-0), BFON, BOFL(2-0)	miscellanous controls #8	C2

Notes to Table 7

1 Slave address is 8A (hex) at IICSA = LOW or 8E (hex) at IICSA = HIGH.

2 Dependent on applications (Figures 23 to 38)

1. FEATURES

- Comb filter circuit for luminance and chrominance separation
- Applicable for standards
  PAL B/G, M and N
  PAL 4.43 (525 lines; 60 Hz)
  NTSC M and N
  NTSC 4.43 (50 and 60 Hz)
- Luminance and chrominance bypasses with short delay in case of no filtering
- Line-locked system clock; CCIR-compatible
- I^2C-bus controlled

2. GENERAL DESCRIPTION

The CMOS digital comb filter circuit is located between video analog-to-digital converters and the video multistandard decoder SAA7151B (not applicable for SAA7191B). The two-dimensional filtering is only appropriate for standard signals from a source with constant phase relationship between subcarrier signal and horizontal frequency. The comb-filter has to be switched off for VTR signals and for separate VBS and and C signals. In VCR and S-Video operation the luminance low-pass and the chrominance bandpass parts can still be used for noise reduction purposes.

The processing delay is
21 x LL27 clocks in active mode or
3 x LL27 in short delay bypass mode (BYPS = 1).

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pins 11, 34, 44)	4.5	5.0	5.5	V
I_P	total supply current	-	85	180	mA
V_i	input levels	TTL-compatible			
V_o	output levels	TTL-compatible			
LL27	typical system clock frequency	-	27	-	MHz
T_{amb}	operating ambient temperature range	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7152	44	PLCC	plastic	SOT187

5. BLOCK DIAGRAM

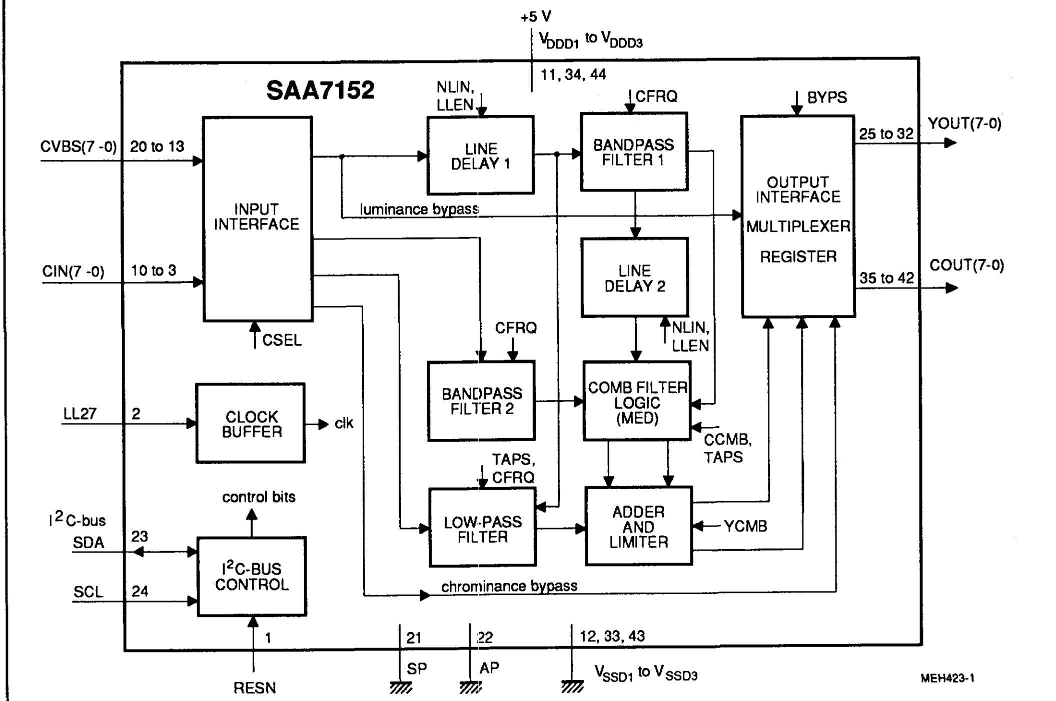


Fig.1 Block diagram.

6. PINNING

SYMBOL	PIN	DESCRIPTION
RESN	1	reset input; active-LOW
LL27	2	line-locked system clock input (27 MHz)
CIN0	3	chrominance input data bits CIN0 to CIN7
CIN1	4	
CIN2	5	
CIN3	6	
CIN4	7	
CIN5	8	
CIN6	9	
CIN7	10	

SYMBOL	PIN	DESCRIPTION
V_{DD1}	11	+5 V supply input 1
V_{SS1}	12	ground 1 (0 V)
CVBS0	13	CVBS input data bits o to 7
CVBS1	14	
CVBS2	15	
CVBS3	16	
CVBS4	17	
CVBS5	18	
CVBS6	19	
CVBS7	20	
SP	21	connected to ground (shift pin for testing)
AP	22	connected to ground (action pin for testing)
SDA	23	I^2C-bus data line
SCL	24	I^2C-bus clock line
YOUT7	25	luminance (Y) output data bits 7 to 0
YOUT6	26	
YOUT5	27	
YOUT4	28	
YOUT3	29	
YOUT2	30	
YOUT1	31	
YOUT0	32	
V_{SS2}	33	ground 2 (0 V)
V_{DD2}	34	+5 V supply input 2
COUT7	35	chrominance (C) output data bits 7 to 0
COUT6	36	
COUT5	37	
COUT4	38	
COUT3	39	
COUT2	40	
COUT1	41	
COUT0	42	
V_{SS3}	43	ground 3 (0 V)
V_{DD3}	44	+5 V supply input 3

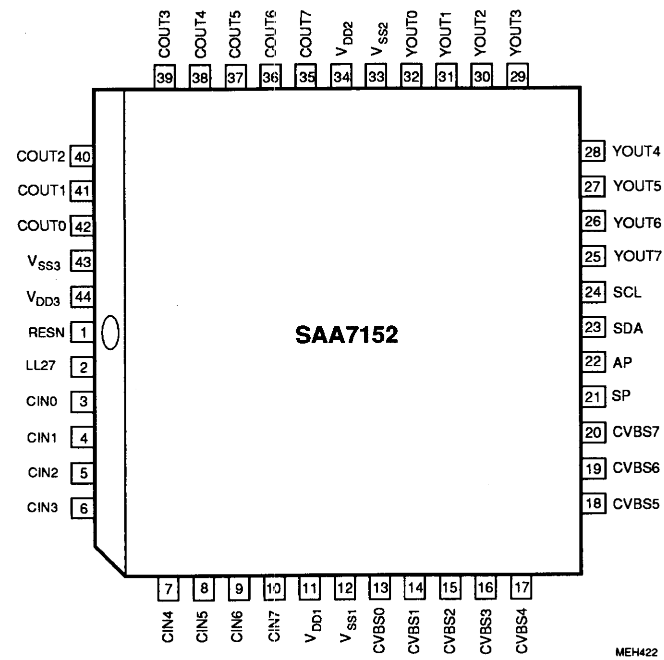


Fig.2 Pin configuration.

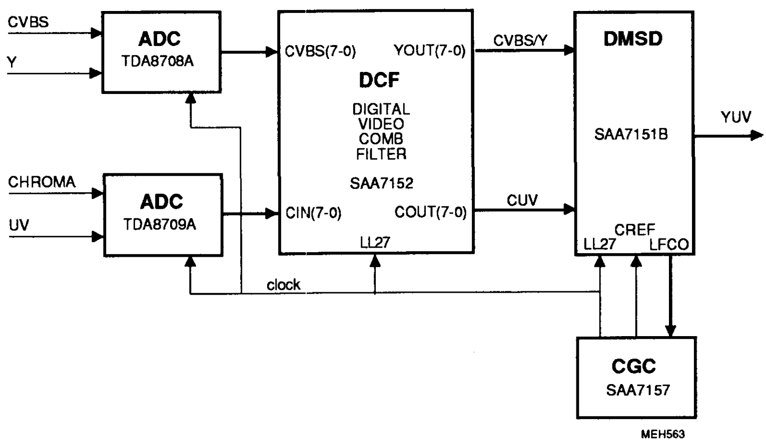


Fig.3 System environment.

7. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A	------	DATAn	A	P

S = start condition
SLAVE ADDRESS = 1011 0010 (B2 h)
A = acknowledge, generated by the slave
SUBADDRESS* = subadress byte (Table 1)
DATA = data byte (Table 1)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; subaddress and data bytes for writing (after X = 0 in address byte)

FUNCTION	SUBADDRESS	DATA D7	D6	D5	D4	D3	D2	D1	D0
Controls	00	BYPS	CSEL	CCMB	YCMB	TAPS	CFRQ	NLIN	LLEN

Function of the bits of Table 1:	
BYPS	Select bypass with a short delay; all other functions are disabled: 0 = no bypass; 1 = comb filter bypassed (delay is 3 LLC)
CSEL	Input mode select: 0 = CVBS selected; 1 = Y/C selected
CCMB	Select comb filtering: 0 = chrominance is bandpassed; 1 = chrominance is comb-filtered
YCMB	Enable chrominance substruction from CVBS signal: 0 = disabled, CVBS/Y signal is only low-passed 1 = enabled (chrominance trap or comb filtering)
TAPS	Selects tap for switching Y and C to adder: 0 = for bandpass/low-pass combination 1 = for comb filter active
CFRQ	Select centre frequency and matching factor of chrominance filter: 0 = 4.43 MHz; 1 = 3.58 MHz
NLIN	Select delay (number of lines): 0 = 4-line comb filter for standard PAL 1 = 2-line comb filter for standard NTSC
LLEN	Selects the number of clocks for each line delay: 0 = 1728 clocks (625 lines); 50 Hz) 1 = 1716 clocks (525 lines; 60 Hz)

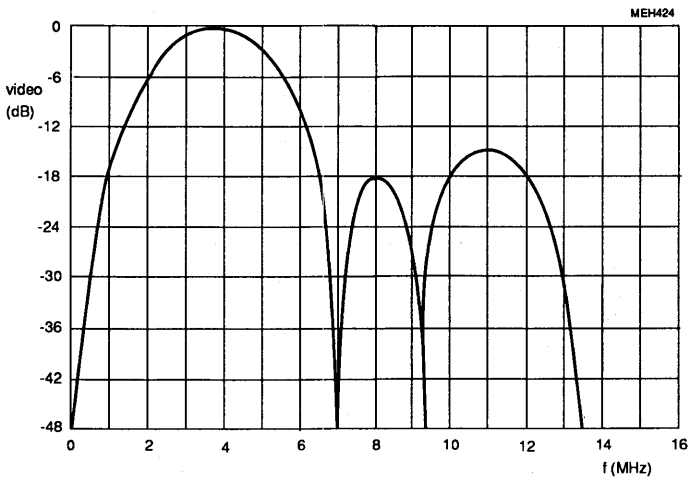


Fig.4 Frequency response of bandpass filters 1 and 2 with CFRQ-bit = 1.

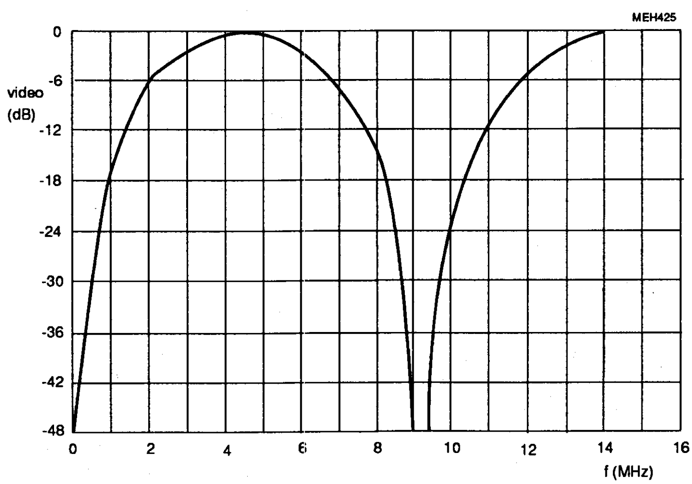


Fig.5 Frequency response of bandpass filters 1 and 2 with CFRQ-bit = 0.

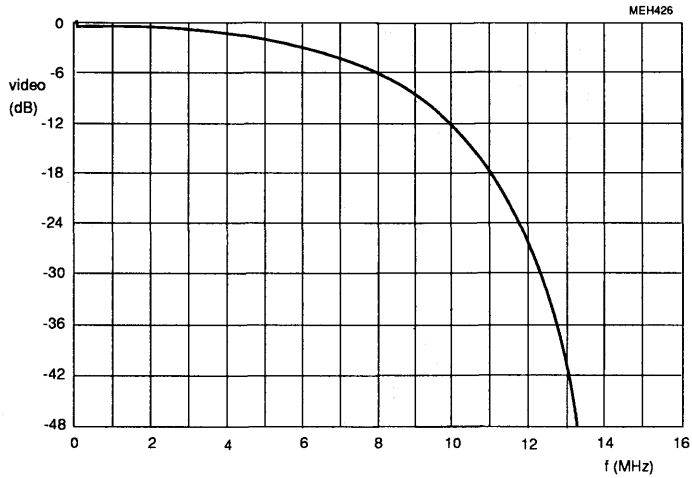


Fig.6 Frequency response of low-pass filter with CFRQ-bit = 1.

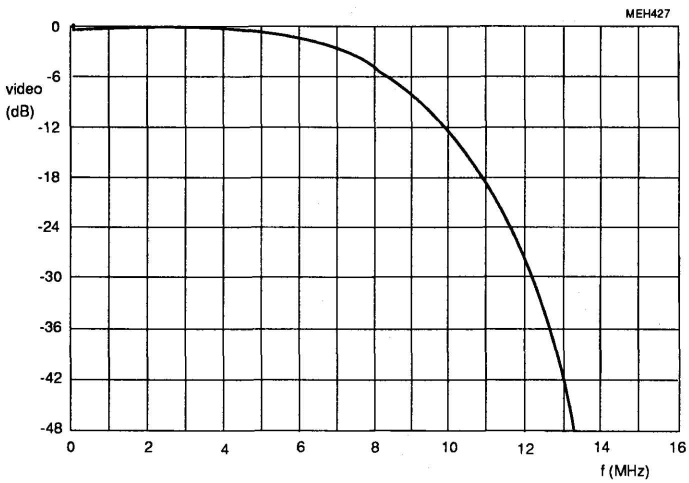


Fig.7 Frequency response of low-pass filter with CFRQ-bit = 0.

Purchase of Philips´ I^2C components conveys a license under the Philips´ I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

8. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 11, 34, 44)	–0.5	7.0	V
V_I	voltage on all inputs	–0.5	V_{DD}+0.5	V
V_O	voltage on all outputs ($I_{O\,max}$ = 20 mA)	–0.5	V_{DD}+0.5	V
P_{tot}	total power dissipation	-	1.0	W
T_{stg}	storage temperature range	–65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±2000	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.; inputs and outputs are protected against electrostatic discharge in normal handling. Normal precautions appropriate to handle MOS devices is recommended ("Handling MOS Devices").

9. CHARACTERISTICS

V_{DD1} to V_{DD3} = 5 V; T_{amb} = 0 to 70 °C and measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 11, 34, 44)		4.5	5	5.5	V
I_{DD}	total supply current (pins 11, 34, 44)	V_{DD} = 5 V; inputs LOW; outputs not connected	-	85	180	mA
I^2C-bus, SDA and SCL (pins 23 and 24)						
V_{IL}	input voltage LOW		–0.5	-	1.5	V
V_{IH}	input voltage HIGH		3	-	V_{DD}+0.5	V
$I_{23,24}$	input current		-	-	±10	µA
I_{ACK}	output current on pin 23	acknowledge	3	-	-	mA
V_{OL}	output voltage at acknowledge	I_{23} = 3 mA	-	-	0.4	V
Data and clock inputs (pins 2 to 10 and pins 13 to 20)						
V_{IL}	LL27 input voltage (pin 2)	LOW	–0.5	-	0.6	V
V_{IH}		HIGH	2.4	-	V_{DD}+0.5	V
V_{IL}	other input voltages	LOW	–0.5	-	0.8	V
V_{IH}		HIGH	2.0	-	V_{DD}+0.5	V
I_{leak}	input leakage current		-	-	10	µA
C_I	input capacitance	data inputs	-	-	8	pF
		clock inputs	-	-	10	pF
$t_{SU.DAT}$	input data set-up time	Fig.8	11	-	-	ns
$t_{HD.DAT}$	input data hold time		3	-	-	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data outputs (pins 25 to 32 and pins 35 to 42)						
V_{OL}	output voltage LOW		0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitor		8	-	25	pF
Timing of data outputs		Fig.8				
t_{OH}	output signal hold time from positive edge of LL27	C_L = 8 pF	3	-	-	ns
t_{OD}	output delay from positive edge of LL27	C_L = 25 pF	-	-	32	ns
Line locked clock input LL27 (pin 2)		Fig.8				
t_{LL27}	cycle time	note 1	35	-	39	ns
t_p	duty factor	t_{LL27H}/t_{LL27}	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns

Note to the characteristics

1. t_{SU}, t_{HD}, t_{OH} and t_{OD} include t_r and t_f.

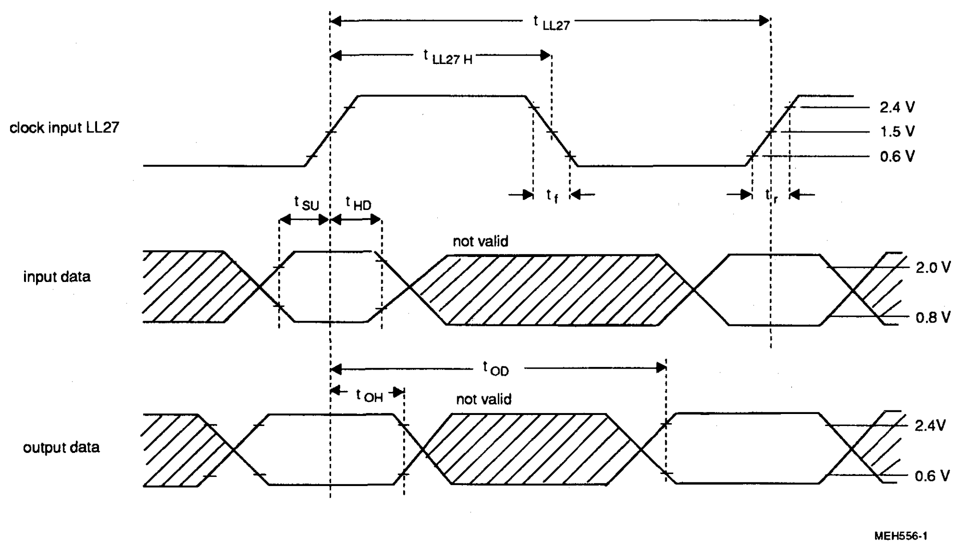


Fig.8 Data input and output timing.

Clock signal generator circuit for digital TV systems (SCGC)

SAA7157

Supercedes data of April 1991

FEATURES

- Clock generation suitable for digital TV systems (line-locked)
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LL1.5A, LL1.5B, LL3A and LL3B (4th and 2nd multiples of input frequency)
- PLL mode or VCO mode selectable
- Reset control and power fail detection
- Suitable for applications with feature box and picture memory

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	3	-	9	mA
I_{DDD}	digital supply current	10	-	60	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_i	input frequency range	6.0	-	7.25	MHz
V_I	input voltage LOW input voltage HIGH	0 2.0	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA7157 generates all clock signals required for a digital TV system suitable for the SAA715x family and the SAA7199B (DENC). The circuit operates in either the phase-locked loop mode (PLL) or voltage controlled oscillator mode (VCO).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7157	20	DIL	plastic	SOT146
SAA7157T	20	mini-pack (SO20)	plastic	SOT163A

Clock signal generator circuit for digital TV systems (SCGC)

SAA7157

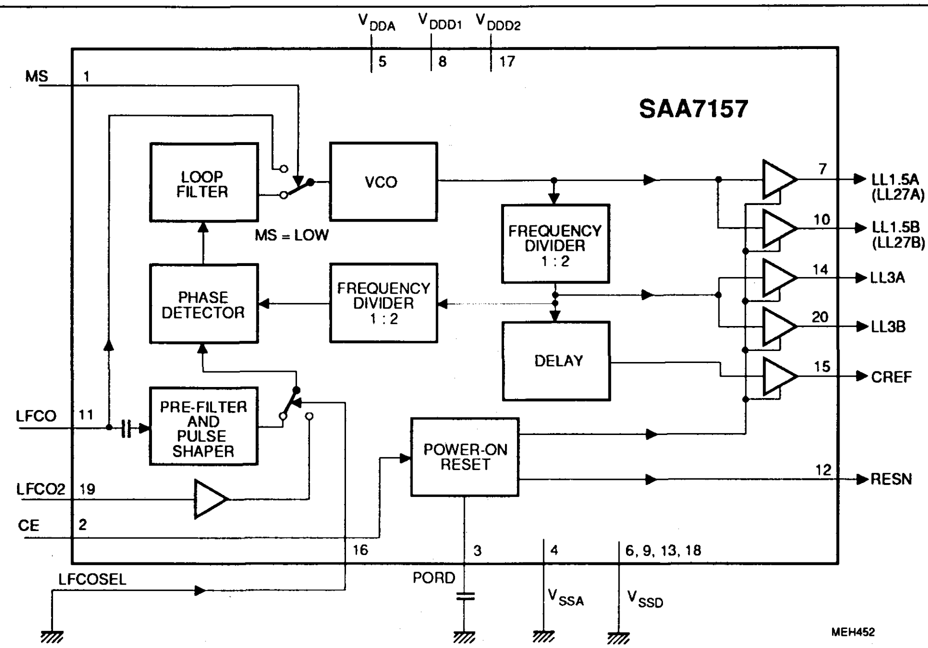


Fig.1 Block diagram.

FUNCTION DESCRIPTION

The SAA7157 generates all clock signals required for a digital TV system suitable for the SAA715x family consisting of an 8-bit analog-to-digital converter (ADC8), digital video multistandard decoder (DMSD2) and video enhancement and D/A processor circuit (VEDA). Optional extras (feature box, video memory etc.) can be driven via external buffers, advantageous for a digital TV system based on display standard conversion concepts.
The 6.75 MHz input signal LFCO (triangular waveform) coming from the DMSD or LFCO2 is multiplied to 27 MHz by the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LL1.5A (pin7) and LL1.5B (pin 10).
The 13.5 MHz frequencies are generated by dividers using ratio of 1:2 and are output on LL3A (pin 14) and LL3B (pin 20).

The rectangular output signals have 50 % duty factor. Outputs with equal frequency may be connected together externally. The clock outputs go HIGH during power-on reset (and chip enable) to ensure that no output clock signals are available before the PLL has locked-on.

Mode select MS

The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit operates as an oscillator and frequency divider. This function is not tested.

Source select LFCOSEL

Line frequency control signal (LFCO) is selected by LFCOSEL input.
LFCOSEL = LOW:
signal from LFCO (pin 11) is selected.
LFCOSEL = HIGH:
signal from LFCO2 (pin 19) is selected.
This function is not tested.

Chip enable CE

The buffer outputs are enabled and RESN is set to HIGH by CE = HIGH (Fig.4).
CE = LOW sets the clock outputs HIGH and RESN output LOW.

CREF output

TV2 digital clock reference output signal. Clock qualifier signal to TV system with 2 times of LFCO or LFCO2 frequency.

Power-on reset

Power-on reset is activated at power-on, when the supply voltage decreases below 3.5 V (Fig.4) or when chip enable is done. The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuits of this digital TV system.
The LFCO or LFCO2 input signals have to be applied before RESN becomes HIGH.

PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode)
CE	2	chip enable /reset (HIGH = outputs enabled)
PORD	3	power-on reset delay, dependent on external capacitor
V_{SSA}	4	analog ground (0 V)
V_{DDA}	5	analog supply voltage (+5 V)
V_{SSD1}	6	digital ground 1 (0 V)
LL1.5A	7	line-locked clock output signal 1.5A (4 times f_{LFCO})
V_{DDD1}	8	digital supply voltage 1 (+5 V)
V_{SSD2}	9	digital ground 2 (0 V)
LL1.5B	10	line-locked clock output signal 1.5B (4 times f_{LFCO})
LFCO	11	line-locked frequency control input signal 1
RESN	12	reset output (active-LOW, Fig.4)
V_{SSD3}	13	digital ground 3 (0 V)
LL3A	14	line-locked clock output signal 3A (2 times f_{LFCO})
CREF	15	clock reference output, qualifier signal (2 times f_{LFCO})
LFCOSEL	16	LFCO source select (LOW = LFCO selected)*
V_{DDD2}	17	digital supply voltage 2 (+5 V)
V_{SSD4}	18	digital ground 4 (0 V)
LFCO2	19	line-locked frequency control input signal 2*
LL3B	20	line-locked clock output signal 3B (2 times f_{LFCO})

PIN CONFIGURATION

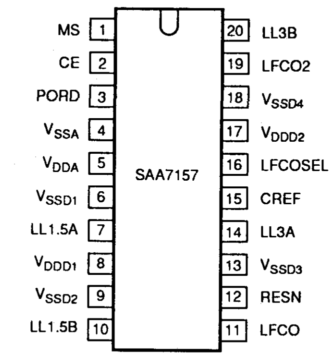


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins as well as supply pins together connected.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	−0.5	7.0	V
V_{DDD}	digital supply voltage (pins 8 and 17)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{DDA} - V_{DDD}$	-	±100	mV
V_O	output voltage (I_{OM} = 20 mA)	−0.5	V_{DDD}	V
P_{tot}	total power dissipation (DIL20)	0	1.1	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling** for all pins	-	tbf	V

* MS and LFCO2 functions are not tested. LFCO2 is a multiple of horizontal frequency.

** Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices ".

CHARACTERISTICS

V_{DDA} = 4.5 to 5.5 V; V_{DDD} = 4.5 to 5.5 V; f_{LFCO} = 6.0 to 7.25 MHz and T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
I_{DDA}	analog supply current (pin 5)		3	-	9	mA
I_{DDD}	digital supply current ($I_8 + I_{17}$)	note 1	10	-	60	mA
V_{reset}	power-on reset threshold voltage	Fig.4	-	3.5	-	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	-	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	-	V_{DDA}	V
f_{LFCO}	input frequency range		6.0	-	7.25	MHz
C_{11}	input capacitance		-	-	10	pF
Inputs MS, CE, LFCOSEL and LFCO2 (pins 1, 2, 16 and 19); note 3						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}	V
f_{LFCO2}	input frequency range for LFCO2		6.0	-	7.25	MHz
I_{LI}	input leakage current	LFCOSEL	50	-	150	μA
		others	-	-	10	μA
C_I	input capacitance		-	-	5	pF
Output RESN (pin 12)						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.4	-	V_{DDD}	V
t_d	RESN delay time	C_3 = 0.1μF; Fig.4	20	-	200	ms
Output CREF (pin 15)						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.4	-	V_{DDD}	V
f_{CREF}	output frequency CREF	Fig.3	-	2 $f_{LFCO(2)}$		MHz
C_L	output load capacitance		15	-	40	pF
t_{SU}	set-up time	Fig.3; note 1	12	-	-	ns
t_{HD}	hold time	Fig.3; note 1	4	-	-	ns
Output signals LL1.5A, LL1.5B, LL3A and LL3B (pins 7, 10, 14, and 20); note 3						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.6	-	V_{DDD}	V
t_{comp}	composite rise time	Fig.3; notes 1 and 2	-	-	8	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LL}	output frequency LL1.5A	Fig.3	-	4 $f_{LFCO(2)}$		MHz
	output frequency LL1.5B		-	4 $f_{LFCO(2)}$		MHz
	output frequency LL3A		-	2 $f_{LFCO(2)}$		MHz
	output frequency LL3B		-	2 $f_{LFCO(2)}$		MHz
t_r, t_f	rise and fall times	note 1; Fig.3	-	-	5	ns
t_{LL}	duty factor LL1.5A, LL1.5B, LL3A and LL3B (mean values)	note 1; Fig.3; at 1.5 V level	43	50	57	%

Notes to the characteristics

1. f_{LFCO} = 7.0 MHz and output load 40 pF (Fig.3). V_{SSA} and V_{SSD} short connected together.
2. t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Fig.3) including rise time, skew and jitter components. Measurements taken between 0.6 V and 2.6 V. Skew between two LLx clocks will not deviate more than ±2 ns if output loads are matched within 20 %.
3. MS and LFCO2 functions not tested.

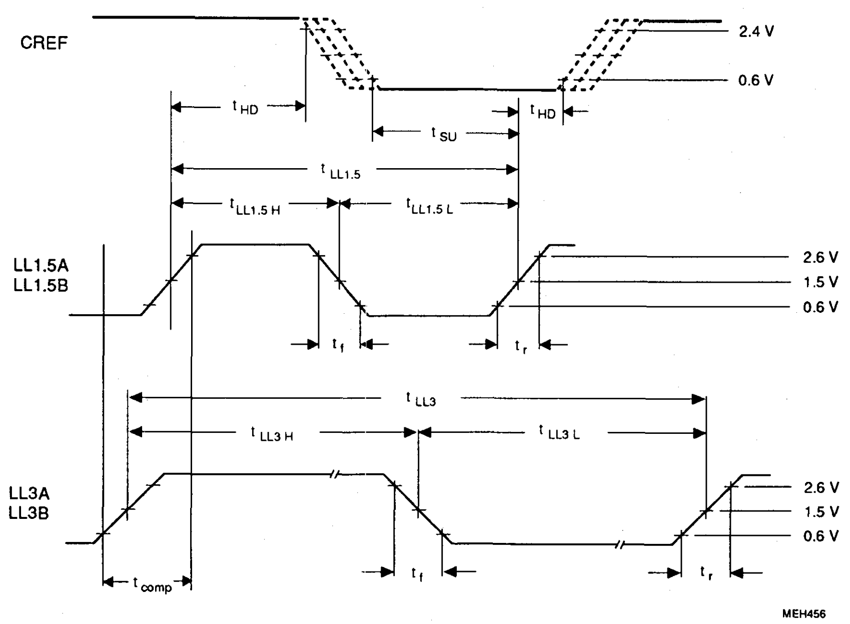


Fig.3 Output timing.

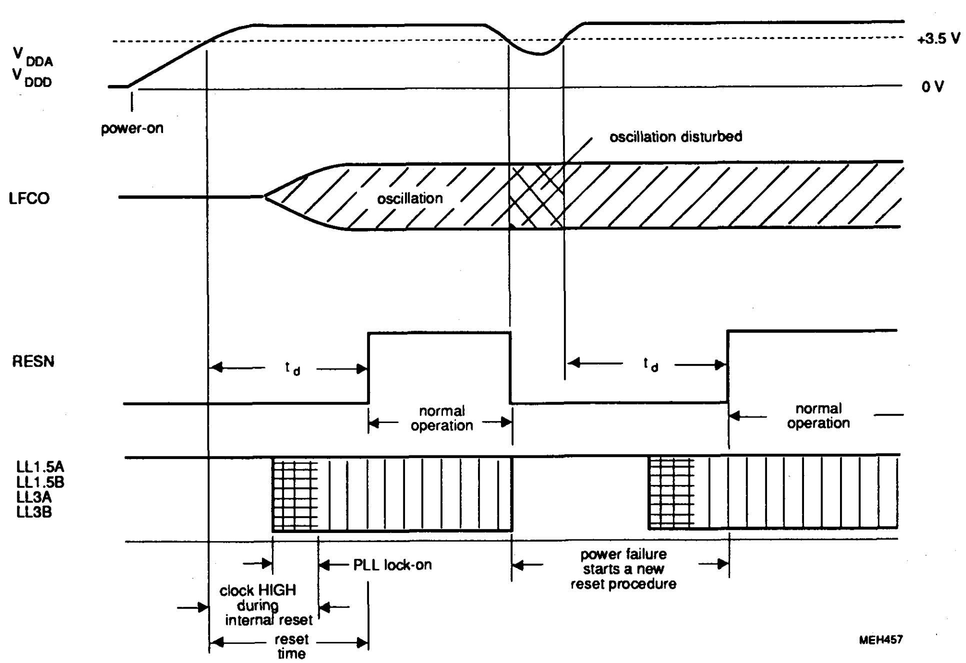


Fig.4 Reset procedure.

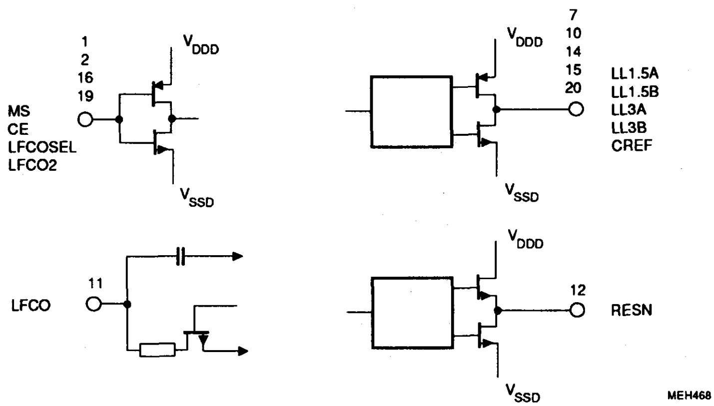


Fig.5 Internal circuit.

Video enhancement and D/A processor (VEDA3)

SAA7164

1. FEATURES

- CMOS circuit to enhance video data and to convert luminance and colour-difference signals from digital-to-analog
- 16-bit parallel input for 4:1:1 and 4:2:2 YUV data
- Data clock input LLC (line-locked clock) for a data rate up to 45 MHz
- 8-bit luminance and 8-bit multiplexed colour-difference formats (optional 7-bit formats)
- MC input to support various clock and pixel rates
- Formatter for YUV input data; 4:2:2 format, 4:1:1 format and filter characteristics selectable
- HREF input to determine the active line (number of pixels)
- Controllable peaking of luminance signal
- Coring stage with controllable threshold to eliminate noise in luminance signal
- Interpolation filter suitable for both formats to increase the data rate in chrominance path
- Polarity of colour-difference signals selectable
- Separate digital-to-analog converters (9-bit resolution for Y; 8-bit for colour-difference signals)
- 1 V (p-p)/ 75 Ω outputs realized by two resistors
- No external adjustments
- All functions controlled via I^2C-bus

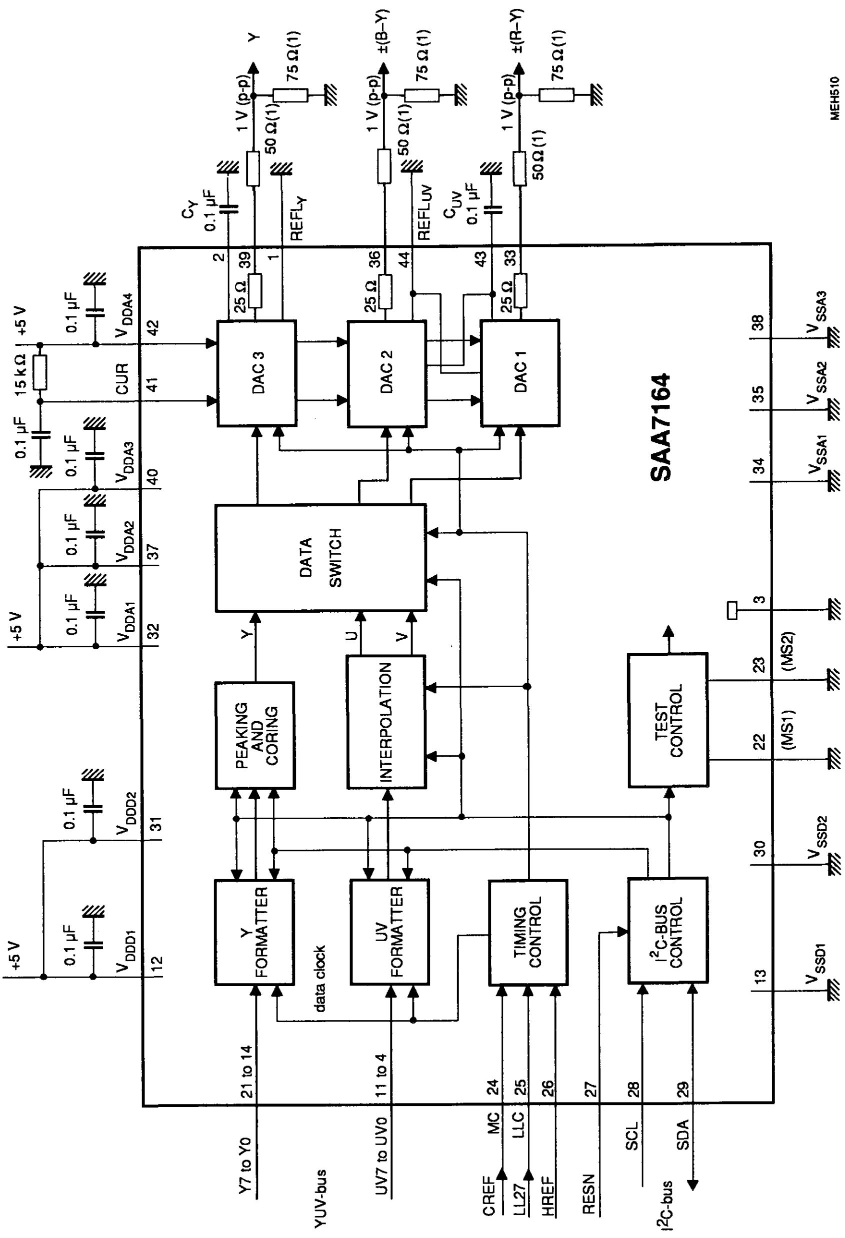
2. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage digital part	4.5	5	5.5	V
V_{DDA}	supply voltage analog part	4.75	5	5.25	V
I_{DD}	total supply current	-	-	160	mA
V_{IL}	input voltage LOW on YUV-bus	−0.5	-	0.8	V
V_{IH}	input voltage HIGH on YUV-bus	2	-	V_{DDD}+0.5	V
f_{LLC}	input data rate	-	-	45	MHz
$V_{o\,Y,CD}$	output signal Y, ±(R−Y) and ±(B−Y) (peak-to-peak value)	-	2	-	V
$R_{L\,Y,CD}$	output load resistance	125	-	-	Ω
ILE	DC integral linearity error in output signal (8-bit data)	-	-	1	LSB
DLE	DC differential error in output signal (8-bit data)	-	-	0.5	LSB
T_{amb}	operating ambient temperature range	0	-	70	°C

3. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9065	44	PLCC	plastic	SOT187

4. BLOCK DIAGRAM



(1) output amplitude determined by resistors ($R_L > 125\Omega$)

Fig.1 Block diagram and application circuit.

5. PINNING

SYMBOL	PIN	DESCRIPTION
$REFL_Y$	1	low reference of luminance DAC (connected to V_{SSA1})
C_Y	2	capacitor for luminance DAC (high reference)
SUB	3	substrate (connected to V_{SSA1})
UV0	4	UV signal input bits UV7 to UV0 (digital colour-difference signal)
UV1	5	
UV2	6	
UV3	7	
UV4	8	
UV5	9	
UV6	10	
UV7	11	
V_{DDD1}	12	+5 V digital supply voltage 1
V_{SSD1}	13	digital ground 1 (0 V)
Y0	14	Y signal input bits Y7 to Y0 (digital luminance signal)
Y1	15	
Y2	16	
Y3	17	
Y4	18	
Y5	19	
Y6	20	
Y7	21	
MS2	22	mode select 2 input for testing chip
MS1	23	mode select 1 input for testing chip
MC	24	data clock CREF (13.5 MHz e. g.); at MC = HIGH the LLC divider-by-two is inactive
LLC	25	line-locked clock signal (LL27 = 27 MHz)
HREF	26	data clock for YUV data inputs (for active line 768Y or 640Y long)
RESN	27	reset input (active LOW)
SCL	28	I^2C-bus clock line
SDA	29	I^2C-bus data line
V_{SSD2}	30	digital ground 2 (0 V)
V_{DDD2}	31	+5 V digital supply voltage 2
V_{DDA1}	32	+5 V analog supply voltage for buffer of DAC 1
(R–Y)	33	±(R–Y) output signal (analog signal)
V_{SSA1}	34	analog ground 1 (0 V)

SYMBOL	PIN	DESCRIPTION
V_{SSA2}	35	analog ground 2 (0 V)
(B–Y)	36	±(B–Y) output signal (analog colour-difference signal)
V_{DDA2}	37	+5 V analog supply voltage for buffer of DAC 2
V_{SSA3}	38	analog ground 3 (0 V)
Y	39	Y output signal (analog luminance signal)
V_{DDA3}	40	+5 V analog supply voltage for buffer of DAC 3
CUR	41	current input for analog output buffers
V_{DDA4}	42	supply and reference voltage for the three DACs
C_{UV}	43	capacitor for chrominance DACs (high reference)
$REFL_{UV}$	44	low reference of chrominance DACs (connected to V_{SSA1})

PIN CONFIGURATION

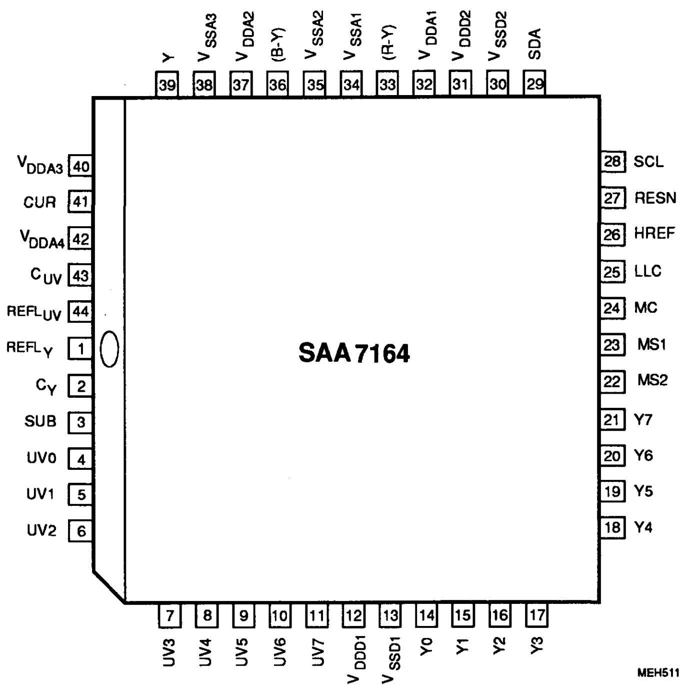


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The CMOS circuit SAA7164 processes digital YUV-bus data up to a data rate of 45 MHz. The data inputs Y7 to Y0 and UV7 to UV0 (Fig.1) are provided with 8-bit data. The data of digital colour-difference signals U and V are in a multiplexed state (serial in 4:2:2 or 4:1:1 format; Tables 2 and 3).

Data is read with the rising edge of LLC (line-locked clock) to achieve a data rate of LLC at MC = HIGH only. If MC is supplied with the frequency CREF (LLC/2 for example), data is read only at every second rising edge (Fig.3).The 7-bit YUV data are also supported by means of the R78-bit (R78 = 0). Additionally, the luminance data format is converted for internal use into a two's complement format by inverting MSB. The Y input byte (bits Y7 to Y0) represent luminance information; the UV input byte (bits UV7 to UV0) one of the two digital colour-difference signals in 4:2:2 format (Table 2).

The HREF input signal (HREF = HIGH) determines the start and the end of an active line (Fig.3), the number of pixels respectively . The analog output Y is blanked at HREF = LOW, the (B–Y) and (R–Y) outputs are in a colourless state. The blanking level can be set by the BLV-bit.
The SAA7164 controllable via the I^2C-bus

Y and UV formatters

The input data formats are formatted into the internally used processing formats (separate for 4:2:2 and 4:1:1 formats). The IFF, IFC and IFL bits control the input data format and determine the right interpolation filter (Figures 10 to 13).

Peaking and coring

Peaking is applied to the Y signal to compensate several bandwidth reductions of the external pre-processing. Y signals can be improved to obtain a better sharpness.

There are the two switchable bandpass filters BF1 and BF 2 controlled via the I^2C-bus by the bits BP1, BP0 and BFB. Thus, a frequency response is achieved in combination with the peaking factor K (Figures 5 to 9; K is determined by the bits BFB, WG1 and WG0).

The coring stage with controllable threshold (4 states controlled by CO1 and CO0 bits) reduces noise disturbances (generated by the bandpass gain) by suppressing the amplitude of small high-frequent signal components. The remaining high-frequent peaking component is available for a weighted addition after coring.

Table 1 LLC and MC configuration modes in DMSD applications

PIN	INPUT SIGNAL	COMMENT
LLC MC	LLC (LL27) CREF	The data rate on YUV-bus is half the clock rate on pin LLC, e. g. in SAA7151B, SAA7191 and SAA7191B single scan operation.
LLC MC	LLC (LL27) MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. in double scan applications.
LLC MC	LLC2/LL3 MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. SAA9051 single scan operation.
Note: YUV data are only latched with the rising edge of LLC at MC = HIGH.		

Table 2 Data format 4 : 2 : 2. (Fig.3)

INPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Interpolation

The chrominance interpolation filter consists of various filter stages, multiplexers and de-multiplexers to increase the data rate of the colour-difference signals by a factor of 2 or 4. The switching of the filters by the bits IFF, IFC and IFL is described previously. Additional signal samples with significant amplitudes between two consecutive signal samples of the low data rate are generated. The time-multiplexed U and V samples are stored in parallel for converting.

Data switch

The digital signals are adapted to the conversation range. U and V data have 8-bit formats again; Y can have 9 bits dependent on peaking. Blanking and switching to colourless level is applied here. Bits can be inverted by INV-bit to change the polarity of colour-difference output signals.

Digital-to-analog converters

Conversion is separate for Y, U and V. The converters use resistor chains with low-impedance output buffers. The minimum output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V floating. An application for 1 V/ 75 Ω on outputs is shown in Fig.1.

Each digital-to-analog converter has its own supply and ground pins suitable for decoupling. The reference voltage, supplying the resistor chain of all three DACs, is the supply voltage V_{DDA4}. The current into pin 41 is 0.3 mA ; a larger current improves the bandwidth but increases the integral non-linearity.

Table 3 Data format 4 : 1 : 1

INPUT	PIXEL BYTE SEQUENCE							
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

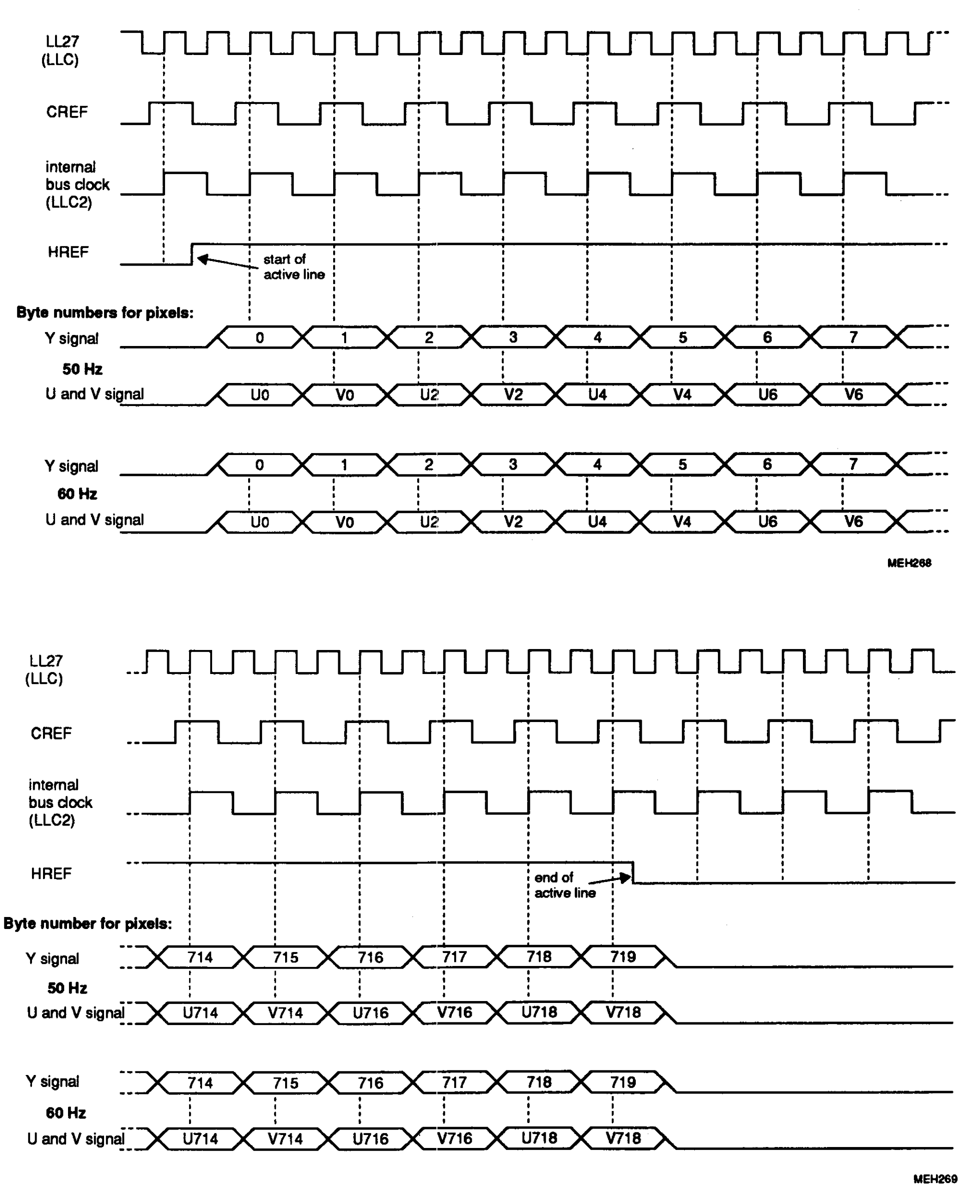


Fig.3 Line control by HREF for 4 : 2 : 2 format, CREF = 13.5 MHz; HREF = 720 pixel; 50 Hz and 60 Hz field.

7. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	−0.3	7	V
V_{DDD2}	supply voltage range (pin 31)	−0.3	7	V
V_{DDA1}	supply voltage range (pin 32)	−0.3	7	V
V_{DDA2}	supply voltage range (pin 37)	−0.3	7	V
V_{DDA3}	supply voltage range (pin 40)	−0.3	7	V
V_{DDA4}	supply voltage range (pin 42)	−0.3	7	V
$V_{diff\ GND}$	difference voltage $V_{SSD} - V_{SSA}$	-	±100	mV
V_n	voltage on all input pins 4 to 11, 14 to 27 and 41	−0.3	V_{DDD}	V
V_n	voltage on analog output pins 33, 36 and 39	−0.3	V_{DDD}	V
P_{tot}	total power dissipation	0	tbf	mW
T_{stg}	storage temperature range	−55	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

8. THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction-to-ambient in free air	46 K/W

9. CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; LLC = LL27; MC = CREF = 13.5 MHz; T_{amb} = 0 to 70 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	for digital part	4.5	5	5.5	V
V_{DDD2}	supply voltage range (pin 31)	for digital part	4.5	5	5.5	V
V_{DDA1}	supply voltage range (pin 32)	for buffer of DAC 1	4.75	5	5.25	V
V_{DDA2}	supply voltage range (pin 37)	for buffer of DAC 2	4.75	5	5.25	V
V_{DDA3}	supply voltage range (pin 40)	for buffer of DAC 3	4.75	5	5.25	V
V_{DDA4}	supply voltage range (pin 42)	DAC reference voltage	4.75	5	5.25	V
I_{DDD}	supply current (I_{DDD1} + I_{DDD2})	for digital part	-	-	140	mA
I_{DDA}	supply current (I_{DDA1} to I_{DDA4})	for DACs and buffers	-	-	20	mA
YUV-bus inputs (pins 4 to 11 and 14 to 21)		Figures 3 and 4				
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	µA
Inputs MS1, MS2, MC, LLC, HREF and RESN (pins 22 to 27)						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	µA
V_{24}	MC input voltage for LL27	27 MHz data rate	2.0	-	V_{DDD}+0.5	V
	CREF signal on MC input	CREF data rate; note 1	-	-	-	V
I²C-bus SCL and SDA (pins 28 and 29)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3.0	-	V_{DDD}+0.5	V
I_I	input current	V_I = LOW or HIGH	-	-	±10	µA
V_{OL}	SDA output voltage LOW (pin 29)	I_{29} = 3 mA	-	-	0.4	V
I_{29}	output current	during acknowledge	3	-	-	mA
Digital-to-analog converters (pins 1, 2, 41, 42, 43 and 44)						
V_{DAC}	input reference voltage for internal resistor chains (pin 42)		4.75	5	5.25	V
I_{CUR}	input current (pin 41)	R_{41-42} = 15 kΩ	-	300	-	µA
$V_{1,44}$	reference voltage LOW	pin connected to V_{SSA1}	-	0	-	V
C_L	external blocking capacitor to V_{SSA1} for reference voltage HIGH (pins 2 and 43)		-	0.1	-	µF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LLC}	data conversation rate (clock)	Fig.3	-	-	45	MHz
Res	resolution	luminance DAC	-	9	-	bit
		chrominance DACs	-	8	-	bit
ILE	DC integral linearity error	8-bit data	-	-	1.0	LSB
DLE	DC differential error	8-bit data	-	-	0.5	LSB
Y, ±(R–Y) and ±(B–Y) analog outputs (pins 39, 33 and 36)						
V_o	output signal voltage (peak-to-peak value)	without load	-	2	-	V
$V_{33,36,39}$	output voltage range	without load; note 2	0.2	-	2.2	V
V_{39}	output blanking level	Y output; note 3	-	16	-	LSB
$V_{33,36}$	output no-colour level	±(R–Y), ±(B–Y); note 4	-	128	-	LSB
$R_{33,36,39}$	internal serial output resistance		-	25	-	Ω
$R_{L\ 33,36,39}$	output load resistance	external load	125	-	-	Ω
B	output signal bandwidth	-3 dB	20	-	-	MHz
t_d	signal delay from input to Y output		-	tbf	-	ns
LLC timing (pins 25)		LLC; Fig.3				
t_{LLC}	cycle time		22.2	37	41	ns
$t_{p\,H}$	pulse width		40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
YUV-bus timing (pins 4 to 11 and 14 to 21)		Fig.5				
t_{SU}	input data set-up time		6	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
MC timing (pin24)		Fig.5				
t_{SU}	input data set-up time		6	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
RESN timing (pin 27)						
t_{SU}	set-up time after power-on or failure	active LOW; note 5	4 x t_{LLC}	-	-	ns

Notes to the characteristics

1. YUV-bus data is read at MC = HIGH (pin 24) clocked with LLC (Fig.5) . Data is read only with every second rising edge of LLC when CREF = LLC/2 on MC-pin 24.
2. 0.2 to 2.2 V ouput voltage range at 8-bit DAC input data. The data word can increase to 9-bit dependent on peaking factor.
3. The luminance signal is set to the digital black level: 16 LSB for BLV-bit = 0; 0 LSB for BLV-bit = 1.
4. The chrominance amplitudes are set to the digital colourless level of 128 LSB.
5. The circuit is prepared for a new data initialization.

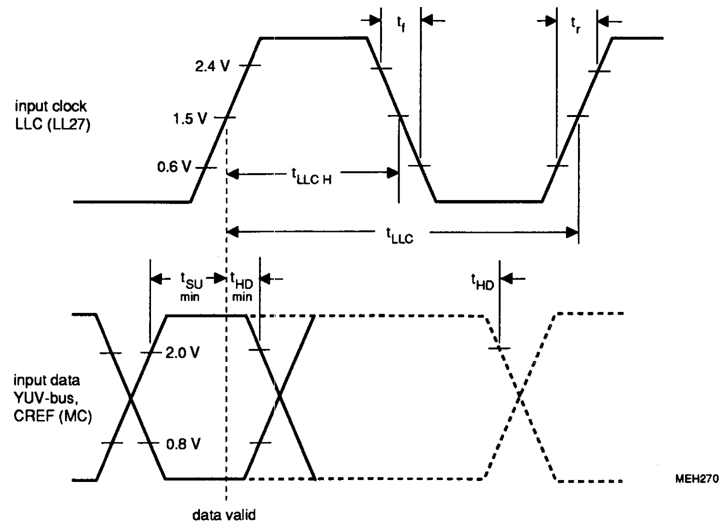


Fig.4 YUV-bus data and CREF timing.

PROCESSING DELAY	LLC CYCLES	REMARKS
YUV digital input to YUV analog output	44	at MC = "1"
	88	at MC = LLC/2

10. I2C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A	-------	DATAn	A	P

S	=	start condition
SLAVE ADDRESS	=	**1011 111X**
A	=	acknowledge, generated by the slave
SUBADDRESS*	=	subaddress byte (Table 4)
DATA	=	data byte (Table 4)
P	=	stop condition
X	=	read/write control bit X = 0, order to write (the circuit is slave receiver) X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I2C-bus transmission

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Peaking and coring	01	0	CO1	CO0	BP1	BP0	BFB	WG1	WG0
Input formats; interpolation	02	IFF	IFC	IFL	0	0	0	0	0
Input/output setting	03	0	0	0	0	DRP	BLV	R78	INV

Bit functions in data bytes:		
CO1 to CO0	Control of coring threshold:	CO1 CO0 → 0 0 coring off 0 1 small noise reduction 1 0 medium noise reduction 1 1 high noise reduction
BP1, BP0 and BFB	Bandpass filter selection:	BP1 BP0 BFB → 0 0 0 characteristic Fig.5 0 1 0 characteristic Fig.6 1 0 0 characteristic Fig.7 1 1 0 characteristic Fig.8 0 0 1 BF1 filter bypassed Fig.9 X X 1 not recommended

BFB, WG1 and WG0	Peaking factor K:	BFB	WG1	WG0	
		0	0	0	K = 1/8; minimum peaking
		0	0	1	K = 1/4
		0	1	0	K = 1/2
		0	1	1	K = 1; maximum peaking
		1	0	0	K = 0; peaking off
		1	0	1	K = 1/4; minimum peaking
		1	1	0	K = 1/2
		1	1	1	K = 1; maximum peaking
IFF, IFC, IFL	Input format and filter control at 13.5 MHz data rate:	IFF	IFC	IFL	
		0	0	0	4 : 1 : 1 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
		0	0	1	4 : 1 : 1 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
		0	1	0	4 : 1 : 1 format; –3 dB attenuation at 1.2 MHz video frequency; Fig.12
		1	0	0	4 : 2 : 2 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
		1	0	1	4 : 2 : 2 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
		1	1	X	4 : 2 : 2 format; –3 dB attenuation at 2.5 MHz video frequency; Fig.13
DRP	UV input data code:	0 = two´s complement; 1 = offset binary			
BLV	Blanking level on Y output:	0 = 16 LSB; 1 = 0 LSB			
R78	YUV input data solution:	0 = 7-bit data; 1 = 8-bit data			
INV	Polarity of colour-difference output signals:	0 = normal polarity equal to input signal 1 = inverted polarity			

Purchase of Philips´ I^{2}C components conveys a license under the Philips´ I^{2}C patent to use the components in the I^{2}C-system provided the system conforms to the I^{2}C specifications defined by Philips.

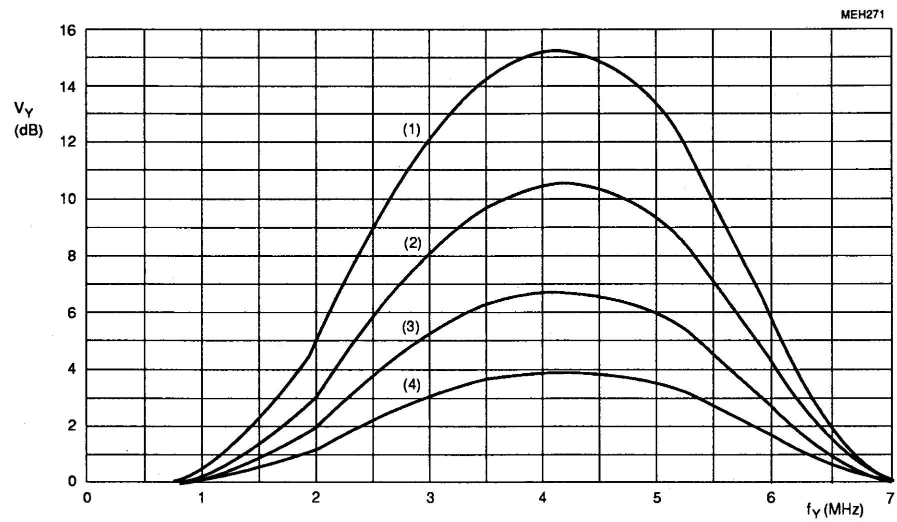


Fig.5 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

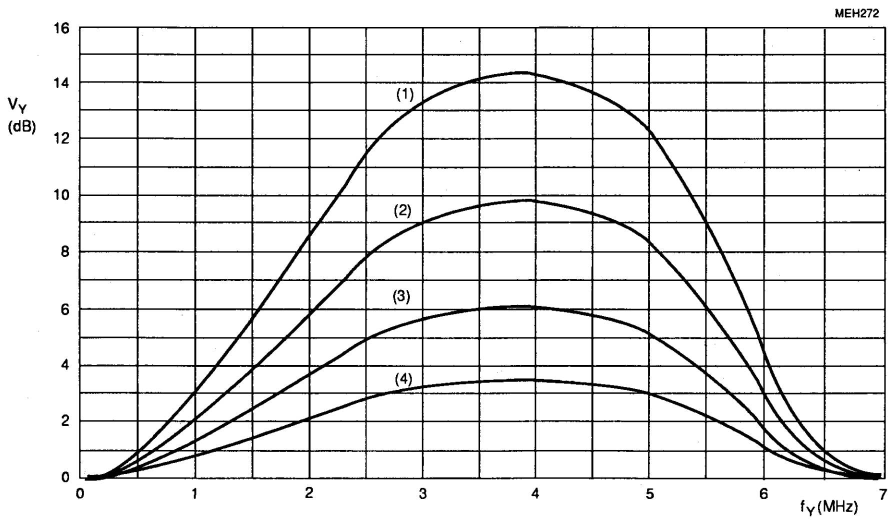


Fig.6 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 1 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

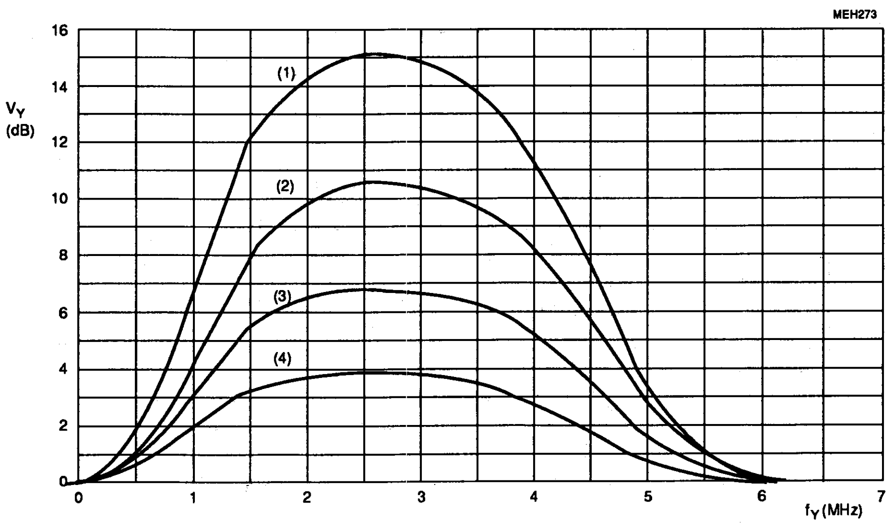


Fig.7 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 0 and BFB = 0:
(1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

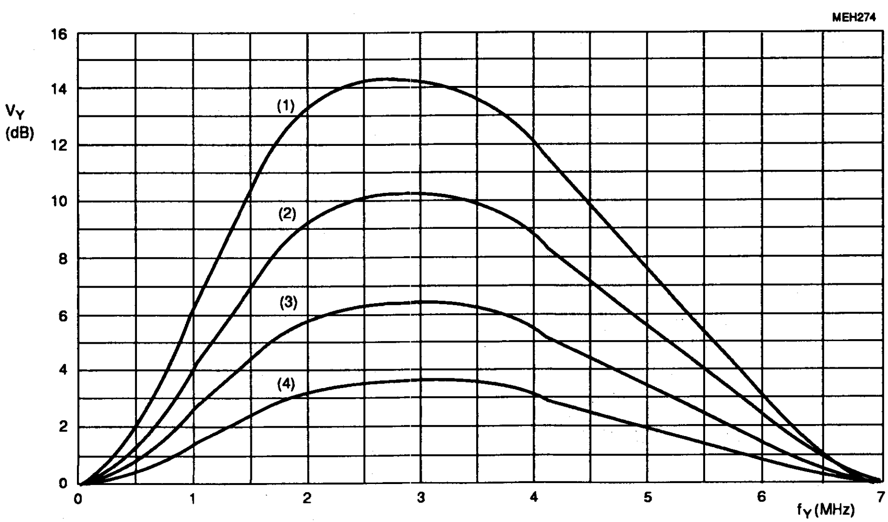


Fig.8 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 1 and BFB = 0:
(1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

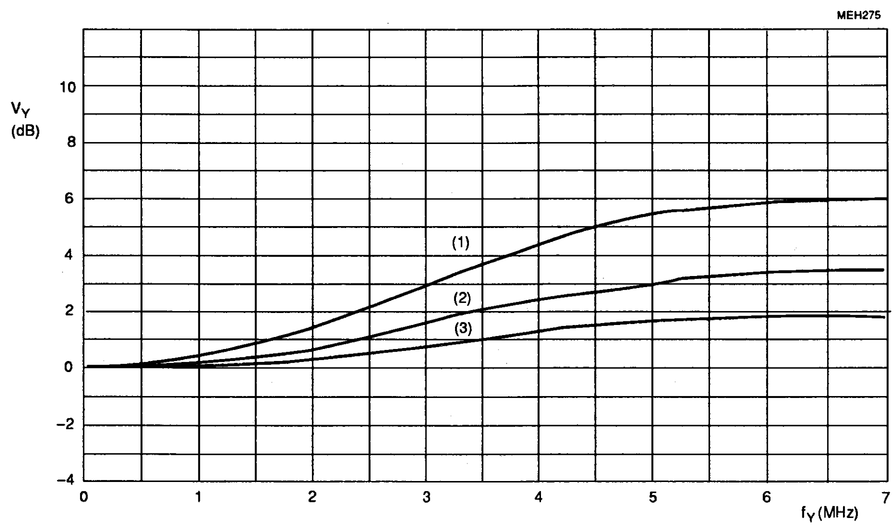


Fig.9 Peaking frequency response with I^2C-bus control bits BP1 = 0; BP0 = 0 and BFB = 1; bandpass filter BF1 bypassed and peaking off; (1) K = 1; (2) K = 1/2; (3) K = 1/4.

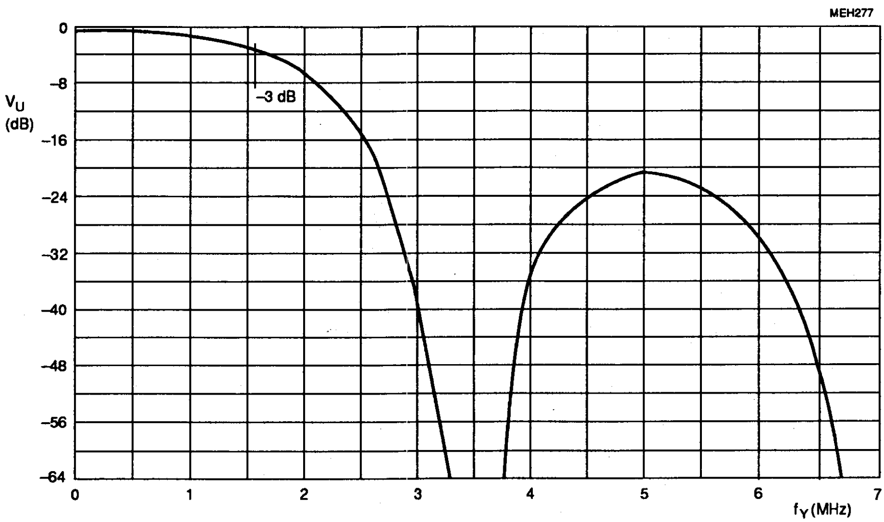


Fig.10 Interpolation filter with I[2]C-bus control bits IFF = 0; IFC = 0 and IFL = 0 in 4:1:1 format, and control bits IFF = 1; IFC = 0 and IFL = 0 in 4:2:2 format; 13.5 MHz data rate.

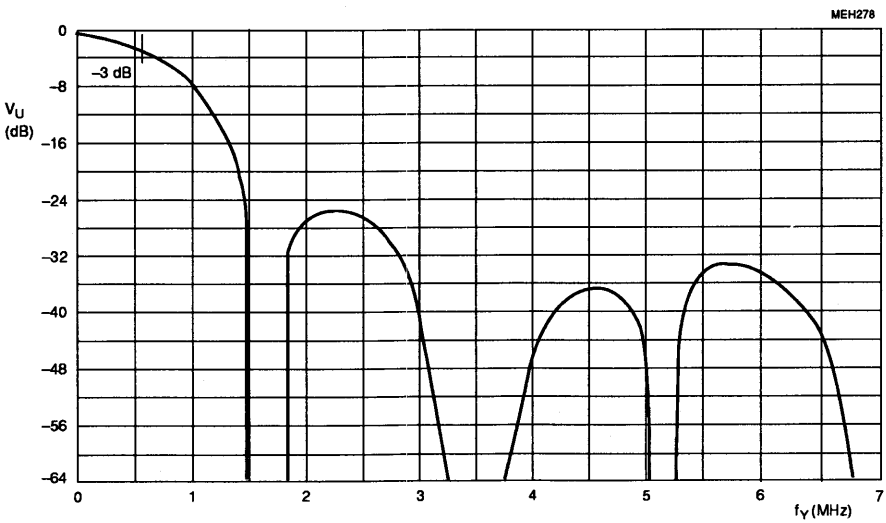


Fig.11 Interpolation filter with I[2]C-bus control bits IFF = 0; IFC = 0 and IFL = 1 in 4:1:1 format, and control bits IFF = 1; IFC = 0 and IFL = 1 in 4:2:2 format; 13.5 MHz data rate.

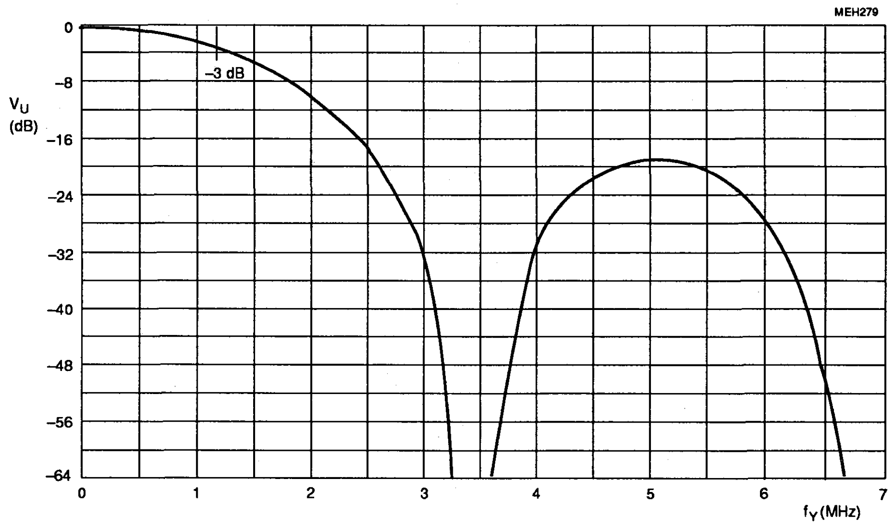


Fig.12 Interpolation filter with I²C-bus control bits IFF = 0; IFC = 1 and IFL = 0 in 4:1:1 format; 13.5 MHz data rate.

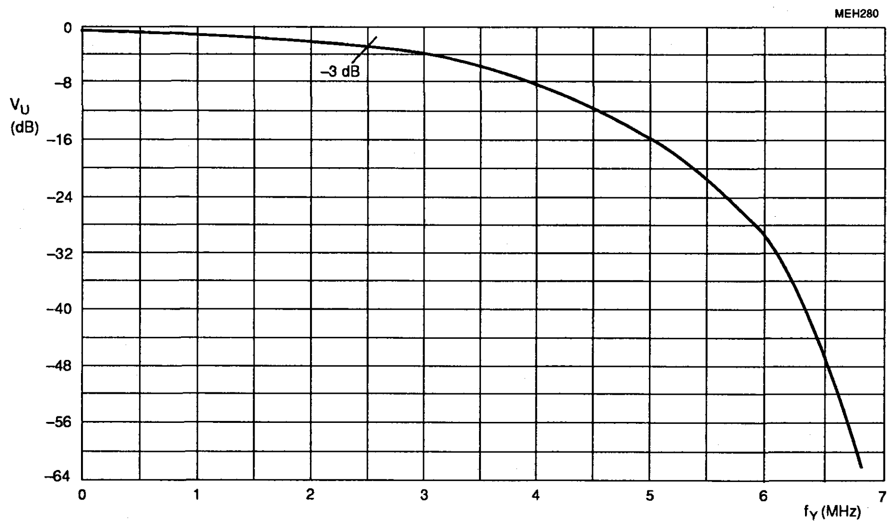


Fig.13 Interpolation filter with I²C-bus control bits IFF = 1; IFC = 1 and IFL = X in 4:2:2 format; 13.5 MHz data rate.

Video enhancement and D/A processor (VEDA2)

SAA7165

FEATURES

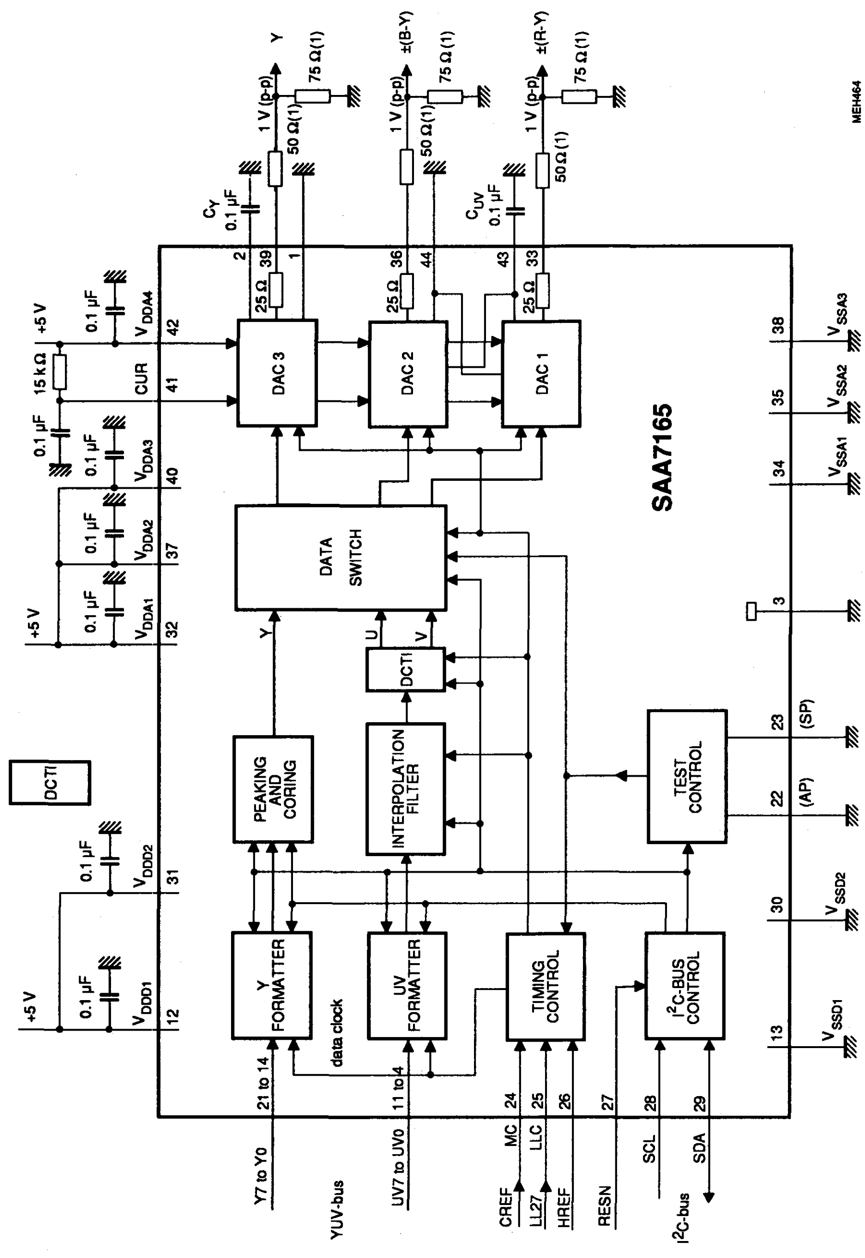
- CMOS circuit to enhance video data and to convert luminance and colour-difference signals from digital-to-analog
- Digital colour transient improvement block DCTI to increase the sharpness of colour transitions. The improved pin-compatible SAA7165 can supercede the SAA9065.
- 16-bit parallel input for 4:1:1 and 4:2:2 YUV data
- Data clock input LLC (line-locked clock) for a data rate up to 32 MHz
- 8-bit luminance and 8-bit multiplexed colour-difference formats (optional 7-bit formats)
- MC input to support various clock and pixel rates
- Formatter for YUV input data; 4:2:2 format, 4:1:1 format and filter characteristics selectable
- HREF input to determine the active line (number of pixels)
- Controllable peaking of luminance signal
- Coring stage with controllable threshold to eliminate noise in luminance signal
- Interpolation filter suitable for both formats to increase the data rate in chrominance path
- Polarity of colour-difference signals selectable
- All functions controlled via I^2C-bus

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage digital part	4.5	5	5.5	V
V_{DDA}	supply voltage analog part	4.75	5	5.25	V
I_{DD}	total supply current	-	tbf	-	mA
V_{IL}	input voltage LOW on YUV-bus	−0.5	-	0.8	V
V_{IH}	input voltage HIGH on YUV-bus	2	-	V_{DDD}+0.5	V
f_{LLC}	input data rate	-	-	32	MHz
$V_{o\ Y,CD}$	output signal Y, ±(R−Y) and ±(B−Y) (peak-to-peak value)	-	2	-	V
$R_{L\ Y,CD}$	output load resistance	125	-	-	Ω
ILE	DC integral linearity error in output signal (8-bit data)	-	-	1	LSB
DLE	DC differential error in output signal (8-bit data)	-	-	0.5	LSB
T_{amb}	operating ambient temperature range	0	-	70	°C

- Separate digital-to-analog converters (9-bit resolution for Y; 8-bit for colour-difference signals)
- 1 V (p-p)/ 75 Ω outputs realized by two resistors
- No external adjustments

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7165	44	PLCC	plastic	SOT187



(1) output amplitude determined by resistors ($R_L > 125\Omega$)

Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
$REFL_Y$	1	low reference of luminance DAC (connected to V_{SSA1})
C_Y	2	capacitor for luminance DAC (high reference)
SUB	3	substrate (connected to V_{SSA1})
UV0	4	UV signal input bits UV7 to UV0 (digital colour-difference signal)
UV1	5	
UV2	6	
UV3	7	
UV4	8	
UV5	9	
UV6	10	
UV7	11	
V_{DDD1}	12	+5 V digital supply voltage 1
V_{SSD1}	13	digital ground 1 (0 V)
Y0	14	Y signal input bits Y7 to Y0 (digital luminance signal)
Y1	15	
Y2	16	
Y3	17	
Y4	18	
Y5	19	
Y6	20	
Y7	21	
AP	22	connected to ground (action pin for testing)
SP	23	connected to ground (shift pin for testing)
MC	24	data clock CREF (13.5 MHz e. g.); at MC = HIGH the LLC divider-by-two is inactive
LLC	25	line-locked clock signal (LL27 = 27 MHz)
HREF	26	data clock for YUV data inputs (for active line 768Y or 640Y long)
RESN	27	reset input (active LOW)
SCL	28	I^2C-bus clock line
SDA	29	I^2C-bus data line
V_{SSD2}	30	digital ground 2 (0 V)
V_{DDD2}	31	+5 V digital supply voltage 2
V_{DDA1}	32	+5 V analog supply voltage for buffer of DAC 1
(R–Y)	33	±(R–Y) output signal (analog signal)
V_{SSA1}	34	analog ground 1 (0 V)

SYMBOL	PIN	DESCRIPTION
V_{SSA2}	35	analog ground 2 (0 V)
(B–Y)	36	±(B–Y) output signal (analog colour-difference signal)
V_{DDA2}	37	+5 V analog supply voltage for buffer of DAC 2
V_{SSA3}	38	analog ground 3 (0 V)
Y	39	Y output signal (analog luminance signal)
V_{DDA3}	40	+5 V analog supply voltage for buffer of DAC 3
CUR	41	current input for analog output buffers
V_{DDA4}	42	supply and reference voltage for the three DACs
C_{UV}	43	capacitor for chrominance DACs (high reference)
$REFL_{UV}$	44	low reference of chrominance DACs (connected to V_{SSA1})

PIN CONFIGURATION

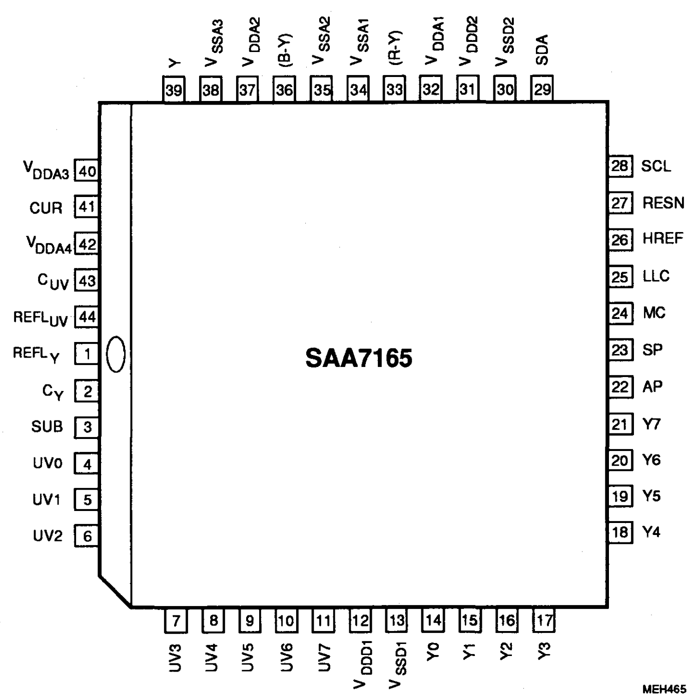


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The CMOS circuit SAA7165 processes digital YUV-bus data up to a data rate of 30 MHz. The data inputs Y7 to Y0 and UV7 to UV0 (Fig.1) are provided with 8-bit data. The data of digital colour-difference signals U and V are in a multiplexed state (serial in 4:2:2 or 4:1:1 format; Tables 2 and 3).

Data is read with the rising edge of LLC (line-locked clock) to achieve a data rate of LLC at MC = HIGH only. If MC is supplied with the frequency CREF (LLC/2 for example), data is read only at every second rising edge (Fig.3). The 7-bit YUV input data are also supported by means of the R78-bit (R78 = 0). Additionally, the luminance data format is converted for internal use into a two´s complement format by inverting MSB. The Y input byte (bits Y7 to Y0) represent luminance information; the UV input byte (bits UV7 to UV0) one of the two digital colour-difference signals in 4:2:2 format (Table 2).

The HREF input signal (HREF = HIGH) determines the start and the end of an active line (Fig.3) the number of pixels respectively . The analog output Y is blanked at HREF = LOW, the ±(B–Y) and ±(R–Y) outputs are in a colourless state. The blanking level can be set by the BLV-bit. The SAA7165 is controllable via the I^2C-bus

Y and UV formatters

The input data formats are formatted into the internally used processing formats (separate for 4:2:2 and 4:1:1 formats). The IFF, IFC and IFL bits control the input data format and determine the right interpolation filter (Figures 10 to 13).

Peaking and coring

Peaking is applied to the Y signal to compensate several bandwidth reductions of the external pre-processing. Y signals can be improved to obtain a better sharpness.

There are the two switchable bandpass filters BF1 and BF 2 controlled via the I^2C-bus by the bits BP1, BP0 and BFB. Thus, a frequency response is achieved in combination with the peaking factor K (Figures 5 to 9; K is determined by the bits BFB, WG1 and WG0).

The coring stage with controllable threshold (4 states controlled by CO1 and CO0 bits) reduces noise disturbances (generated by the bandpass gain) by suppressing the amplitude of small high-frequent signal components. The remaining high-frequent peaking component is available for a weighted addition after coring.

Table 1 LLC and MC configuration modes in DMSD applications

PIN	INPUT SIGNAL	COMMENT
LLC MC	LLC (LL27) CREF	The data rate on YUV-bus is half the clock rate on pin LLC, e. g. in SAA7151B, SAA7191 and SAA7191B single scan operation.
LLC MC	LLC (LL27) MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. in double scan applications.
LLC MC	LLC2/LL3 MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. SAA9051 single scan operation.
Note: YUV data are only latched with the rising edge of LLC at MC = HIGH.		

INPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Interpolation

The chrominance interpolation filter consists of various filter stages, multiplexers and de-multiplexers to increase the data rate of the colour-difference signals by a factor of 2 or 4. The switching of the filters by the bits IFF, IFC and IFL is described previously. Additional signal samples with significant amplitudes between two consecutive signal samples of the low data rate are generated. The time-multiplexed U and V samples are stored in parallel for converting.

Data switch

The digital signals are adapted to the conversation range. U and V data have 8-bit formats again; Y can have 9 bits dependent on peaking. Blanking and switching to colourless level is applied here. Bits can be inverted by INV-bit to change the polarity of colour-difference output signals.

Digital colour transient improvement (DCTI)

The DCTI circuit improves the transition behaviour of the UV colour-difference signals. As the CVBS signal allows for a 4 : 1 : 1 bandwidth representation only, the DCTI improves the transients to the same performance as signals coming from a 4 : 2 : 2 source – or even more.
In order to obtain the point of inflection, the second derivative of the signal is calculated. The improved transition is centered with respect to the point of inflection of the original signal. Thus, there is no horizontal shift of the resulting signal.

The transition area length to be improved is controlled via I^2C-bus by the bits LI1 and LI0 (Table 4); the sensitivity of the DCTI block is controlled by the bits GA1 and GA0. The CMO bit controls the colour detail sensitivity. It should be set to 1 (ON) if the video signal contains fine colour details (recommended operation mode).

Digital-to-analog converters

Conversion is separate for Y, U and V. The converters use resistor chains with low-impedance output buffers. The minimum output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V floating. An application for 1 V/ 75 Ω on outputs is shown in Fig.1.

Each digital-to-analog converter has its own supply and ground pins suitable for decoupling. The reference voltage, supplying the resistor chain of all three DACs, is the supply voltage V_{DDA4}. The current into pin 41 is 0.3 mA ; a larger current improves the bandwidth but increases the integral non-linearity.

Table 3 Data format 4 : 1 : 1

INPUT	PIXEL BYTE SEQUENCE							
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

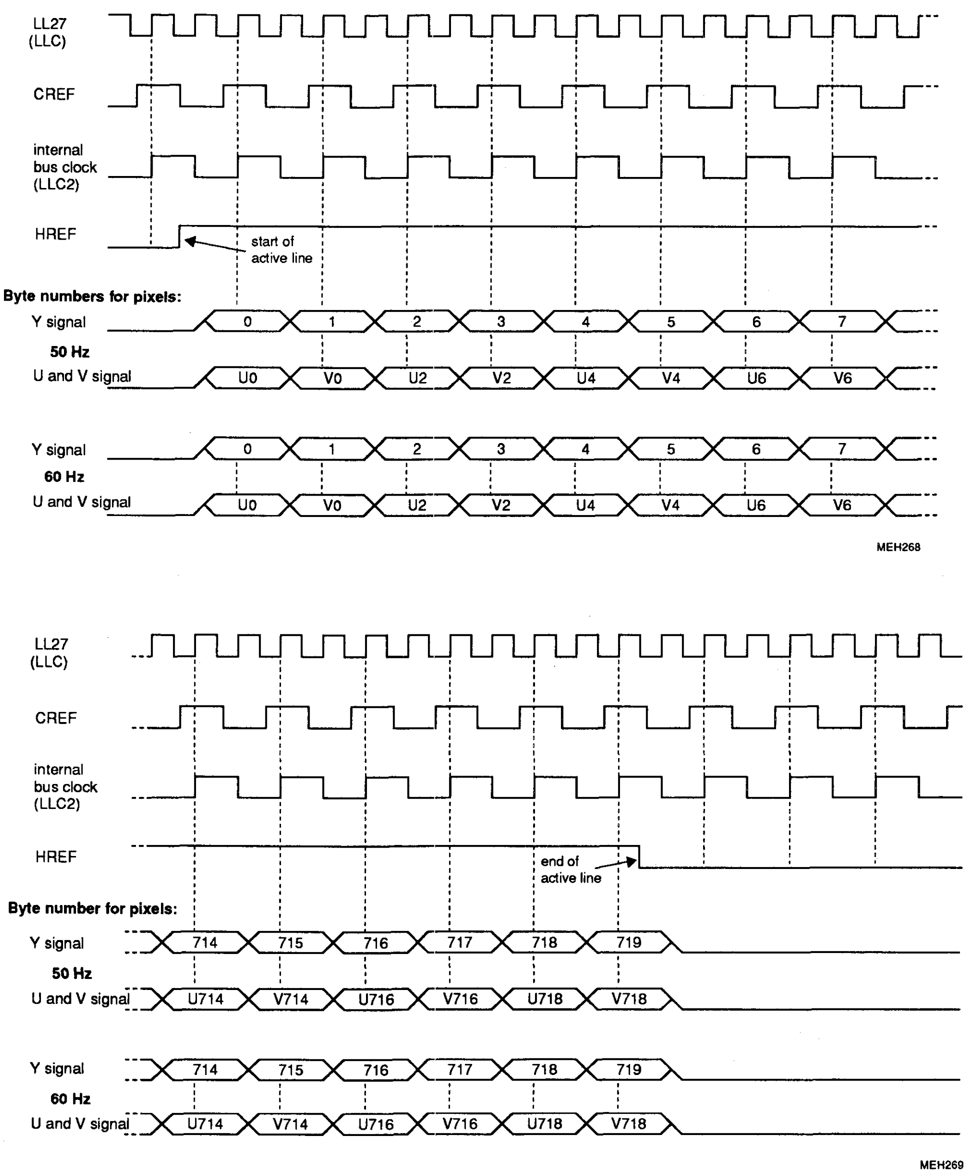


Fig.3 Line control by HREF for 4 : 2 : 2 format, CREF = 13.5 MHz; HREF = 720 pixel; 50 Hz and 60 Hz field.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	−0.3	7	V
V_{DDD2}	supply voltage range (pin 31)	−0.3	7	V
V_{DDA1}	supply voltage range (pin 32)	−0.3	7	V
V_{DDA2}	supply voltage range (pin 37)	−0.3	7	V
V_{DDA3}	supply voltage range (pin 40)	−0.3	7	V
V_{DDA4}	supply voltage range (pin 42)	−0.3	7	V
$V_{diff\ GND}$	difference voltage $V_{SSD} - V_{SSA}$	-	±100	mV
V_n	voltage on all input pins 4 to 11, 14 to 27 and 41	−0.3	V_{DDD}	V
V_n	voltage on analog output pins 33, 36 and 39	−0.3	V_{DDD}	V
P_{tot}	total power dissipation	0	tbf	mW
T_{stg}	storage temperature range	−55	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction-to-ambient in free air	46 K/W

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; LLC = LL27; MC = CREF = 13.5 MHz; T_{amb} = 0 to 70 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	for digital part	4.5	5	5.5	V
V_{DDD2}	supply voltage range (pin 31)	for digital part	4.5	5	5.5	V
V_{DDA1}	supply voltage range (pin 32)	for buffer of DAC 1	4.75	5	5.25	V
V_{DDA2}	supply voltage range (pin 37)	for buffer of DAC 2	4.75	5	5.25	V
V_{DDA3}	supply voltage range (pin 40)	for buffer of DAC 3	4.75	5	5.25	V
V_{DDA4}	supply voltage range (pin 42)	DAC reference voltage	4.75	5	5.25	V
I_{DDD}	supply current (I_{DDD1} + I_{DDD2})	for digital part	-	tbf	tbf	mA
I_{DDA}	supply current (I_{DDA1} to I_{DDA4})	for DACs and buffers	-	tbf	tbf	mA
YUV-bus inputs (pins 4 to 11 and 14 to 21)		Figures 3 and 4				
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	μA
Inputs MS1, MS2, MC, LLC, HREF and RESN (pins 22 to 27)						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	μA
V_{24}	MC input voltage for LL27	27 MHz data rate	2.0	-	V_{DDD}+0.5	V
	CREF signal on MC input	CREF data rate; note 1	-	-	-	V
I^2C-bus SCL and SDA (pins 28 and 29)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3.0	-	V_{DDD}+0.5	V
I_I	input current	V_I = LOW or HIGH	-	-	±10	μA
V_{ACK}	output voltage at acknowledge (pin 29)	I_{29} = 3 mA	-	-	0.4	V
I_{29}	output current	during acknowledge	3	-	-	mA
Digital-to-analog converters (pins 1, 2, 41, 42, 43 and 44)						
V_{DAC}	input reference voltage for internal resistor chains (pin 42)		4.75	5	5.25	V
I_{CUR}	input current (pin 41)	R_{41-42} = 15 kΩ	-	300	-	μA
$V_{1,44}$	reference voltage LOW	pin connected to V_{SSA1}	-	0	-	V
C_L	external blocking capacitor to V_{SSA1} for reference voltage HIGH (pins 2 and 43)		-	0.1	-	μF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LLC}	data conversation rate (clock)	Fig.3	-	-	32	MHz
Res	resolution	luminance DAC	-	9	-	bit
		chrominance DACs	-	8	-	bit
ILE	DC integral linearity error	8-bit data	-	-	1.0	LSB
DLE	DC differential error	8-bit data	-	-	0.5	LSB
Y, ±(R–Y) and ±(B–Y) analog outputs (pins 39, 33 and 36)						
V_o	output signal voltage (peak-to-peak value)	without load	-	2	-	V
$V_{33,36,39}$	output voltage range	without load; note 2	0.2	-	2.2	V
V_{39}	output blanking level	Y output; note 3	-	16	-	LSB
$V_{33,36}$	output no-colour level	±(R–Y), ±(B–Y); note 4	-	128	-	LSB
$R_{33,36,39}$	internal serial output resistance		-	25	-	Ω
$R_{L\ 33,36,39}$	output load resistance	external load	125	-	-	Ω
B	output signal bandwidth	-3 dB	20	-	-	MHz
t_d	signal delay from input to Y output		-	tbf	-	ns
LLC timing (pins 25)		LLC; Fig.3				
t_{LLC}	cycle time		33	37	41	ns
$t_{p\ H}$	pulse width		40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
YUV-bus timing (pins 4 to 11 and 14 to 21)		Fig.5				
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
MC timing (pin24)		Fig.5				
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
RESN timing (pin 27)						
t_{SU}	set-up time after power-on or failure	active LOW; note 5	4 x t_{LLC}	-	-	ns

Notes to the characteristics

1. YUV-bus data is read at MC = HIGH (pin 24) clocked with LLC (Fig.5) . Data is read only with every second rising edge of LLC when CREF = LLC/2 on MC-pin 24.
2. 0.2 to 2.2 V ouput voltage range at 8-bit DAC input data. The data word can increase to 9-bit dependent on peaking factor.
3. The luminance signal is set to the digital black level: 16 LSB for BLV-bit = 0; 0 LSB for BLV-bit = 1.
4. The chrominance amplitudes are set to the digital colourless level of 128 LSB.
5. The circuit is prepared for a new data initialization.

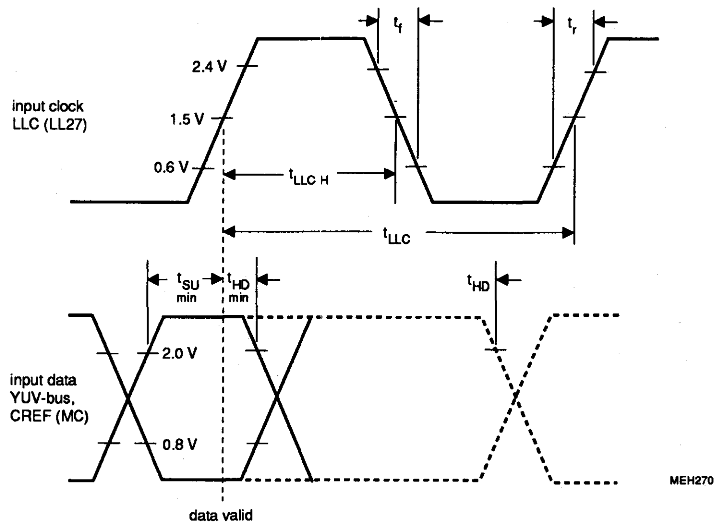


Fig.4 YUV-bus data and CREF timing.

PROCESSING DELAY	LLC CYCLES	REMARKS
YUV digital input to YUV analog output	66 132	at MC = "1" at MC = LLC/2

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A	-----	DATAn	A	P

S = start condition
SLAVE ADDRESS = **1011 111X**
A = acknowledge, generated by the slave
SUBADDRESS* = subadress byte (Table 4)
DATA = data byte (Table 4)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I²C-bus transmission

FUNCTION	SUBADDRESS	DATA D7	D6	D5	D4	D3	D2	D1	D0
Peaking and coring	01	AFB	CO1	CO0	BP1	BP0	BFB	WG1	WG0
Input formats; interpolation	02	IFF	IFC	IFL	CMO	LI1	LI0	GA1	GA0
Input/output setting	03	0	0	DC1	DC0	DRP	BLV	R78	INV

Bit functions in data bytes:

"01"
CO1 and CO0 — Control of coring threshold:

CO1	CO0	
0	0	coring off
0	1	small noise reduction
1	0	medium noise reduction
1	1	high noise reduction

AFB, BP1, BP0, BFB — Bandpass filter selection:

AFB	BP1	BP0	BFB	
X	0	0	0	characteristic Fig.5
X	0	1	0	characteristic Fig.6
X	1	0	0	characteristic Fig.7
X	1	1	0	characteristic Fig.8
0	X	X	1	BF1 filter bypassed Fig.9(a)
1	X	X	1	BF1 filter bypassed Fig.9(b)

BFB, WG1 and WG0	Peaking factor K:	BFB	WG1	WG0	
		0	0	0	K = 1/8; minimum peaking
		0	0	1	K = 1/4
		0	1	0	K = 1/2
		0	1	1	K = 1; maximum peaking
		1	0	0	K = 0; peaking off
		1	0	1	K = 1/4; minimum peaking
		1	1	0	K = 1/2
		1	1	1	K = 1; maximum peaking
"02" IFF, IFC, IFL	Input format and filter control at 13.5 MHz data rate:	IFF	IFC	IFL	
		0	0	0	4 : 1 : 1 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
		0	0	1	4 : 1 : 1 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
		0	1	X	4 : 1 : 1 format; –3 dB attenuation at 1.2 MHz video frequency; Fig.12
		1	0	0	4 : 2 : 2 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
		1	0	1	4 : 2 : 2 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
		1	1	X	4 : 2 : 2 format; –3 dB attenuation at 2.5 MHz video frequency; Fig.13
CMO	Choice modulation:	0 = modulation off; 1 = modulation on			
LI1 and LI0	DCTI timing range:	LI1	LI0		range
		0	0		+4 / –4
		0	1		+6 / –6
		1	0		+8 / –8
		1	1		+12 / –12
GA1 and GA0	DCTI gain factor:	GA1	GA0		factor
		0	0		off
		0	1		1/4
		1	0		1/2
		1	1		1
"03" DC1 and DC0	Delay compensation of luminance signal:	DC1	DC0		delayed clock cycles
		0	0		0
		0	1		+1
		1	0		–2
		1	1		–1

DRP	UV input data code:	0 = two's complement; 1 = offset binary
BLV	Blanking level on Y output:	0 = 16 LSB; 1 = 0 LSB
R78	YUV input data solution:	0 = 7-bit data; 1 = 8-bit data
INV	Polarity of colour-difference output signals:	0 = normal polarity equal to input signal 1 = inverted polarity

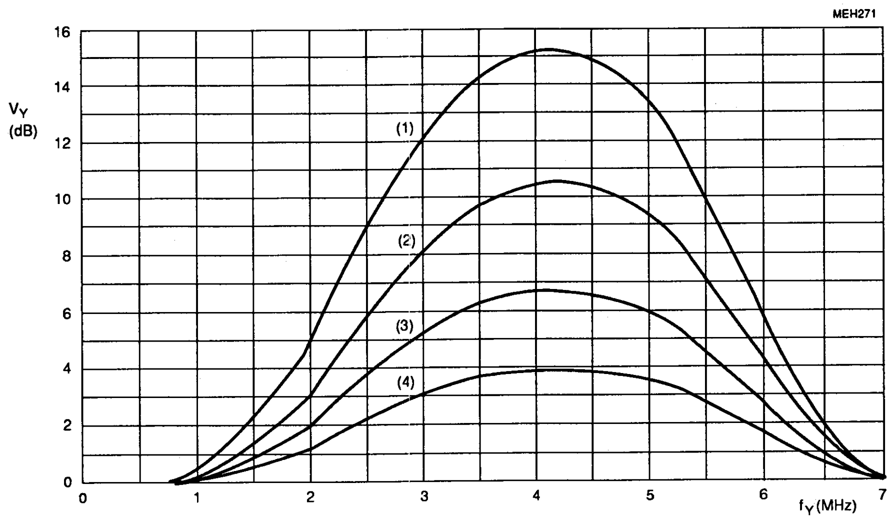


Fig.5 Peaking frequency response with I^{2}C-bus control bits BP1 = 0; BP0 = 0 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

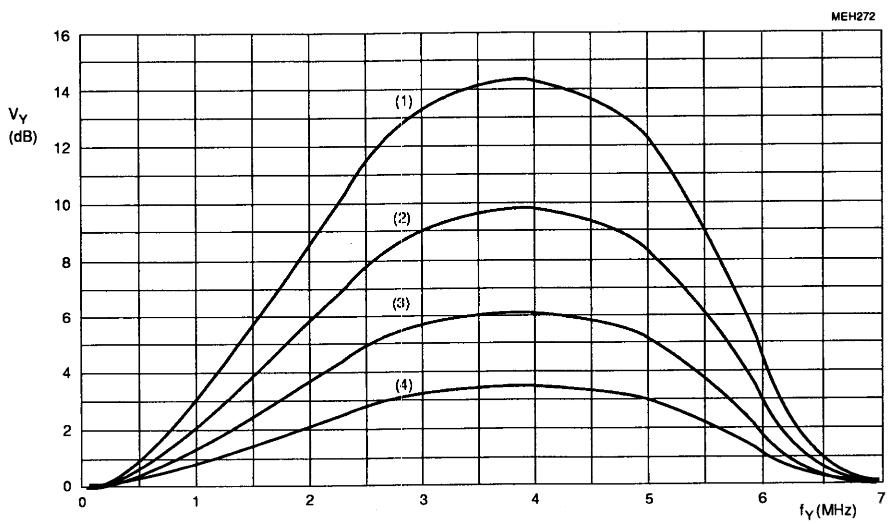


Fig.6 Peaking frequency response with I^{2}C-bus control bits BP1 = 0; BP0 = 1 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

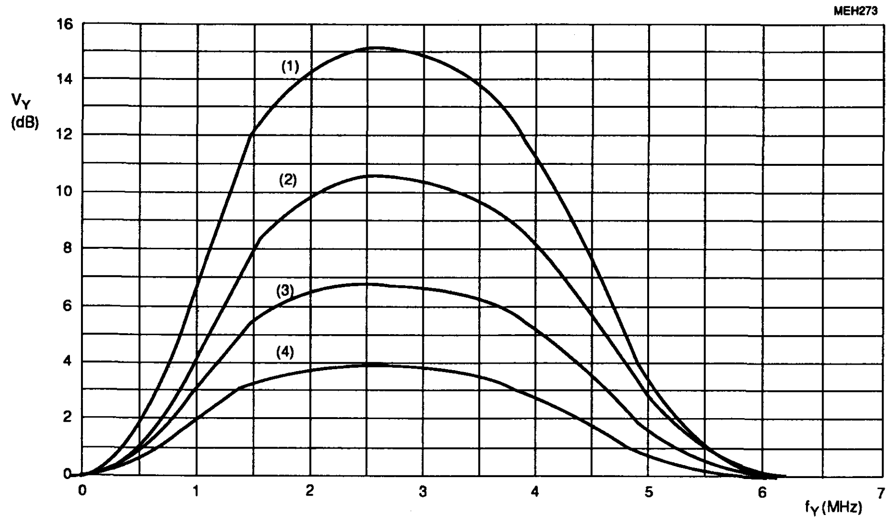


Fig.7 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 0 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

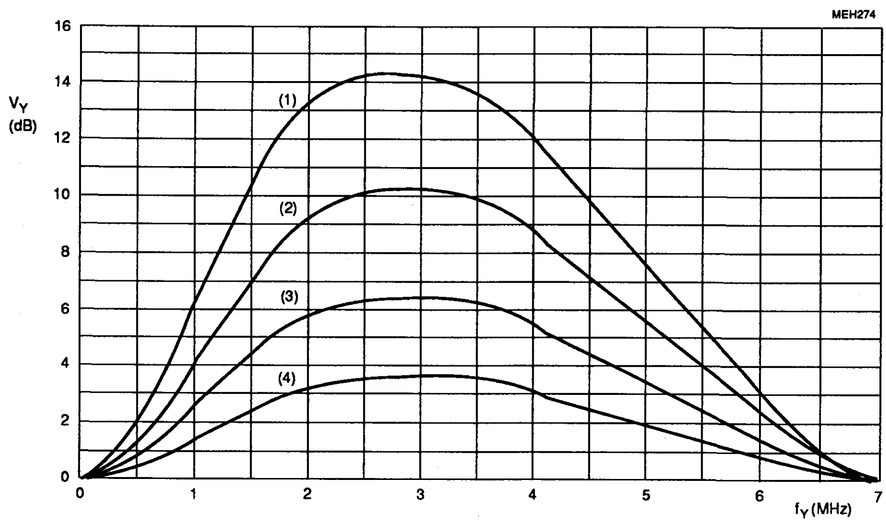


Fig.8 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 1 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

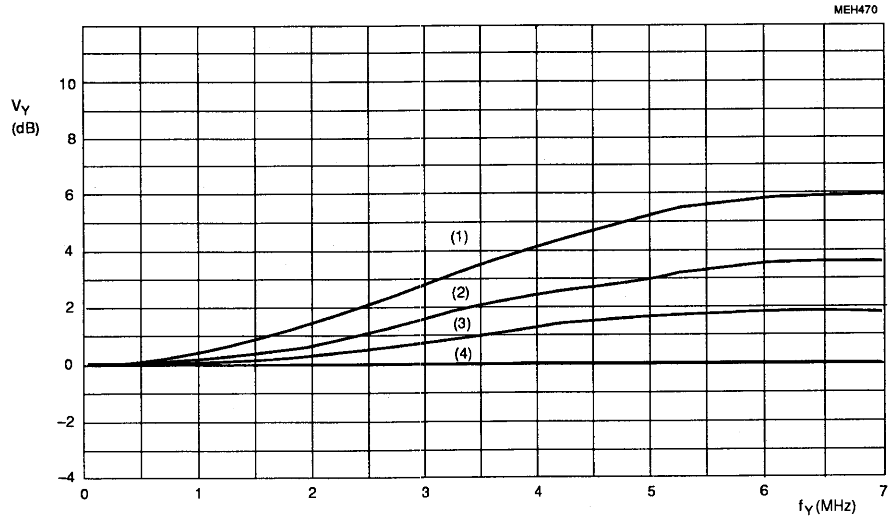


Fig.9(a) Peaking frequency response with I²C-bus control bits AFB = 0, BP1 = 0, BP0 = 0 and BFB = 1; bandpass filter BF1 bypassed and peaking off; (1) K = 1, (2) K = 1/2, (3) K = 1/4 and (4) K = 0

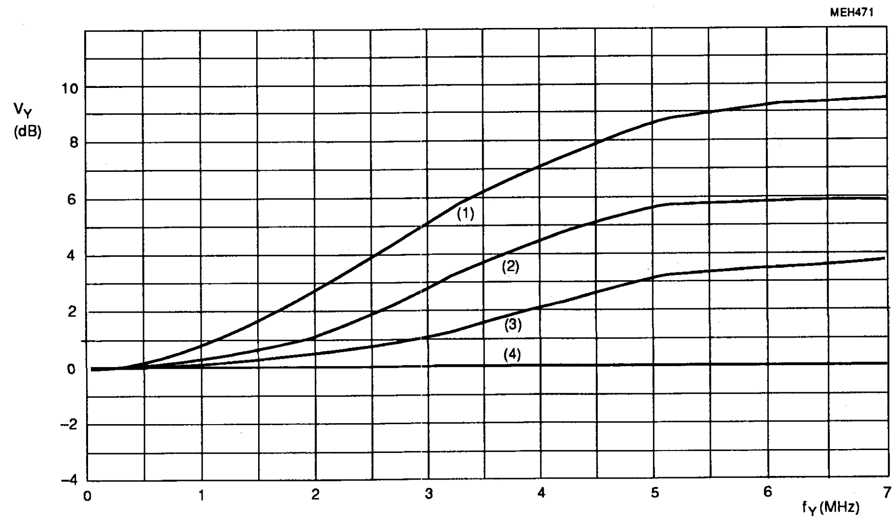


Fig.9(b) Peaking frequency response with I²C-bus control bits AFB = 1, BP1 = 0, BP0 = 0 and BFB = 1; bandpass filter BF1 bypassed and peaking off; (1) K = 1, (2) K = 1/2, (3) K = 1/4 and (4) K = 0.

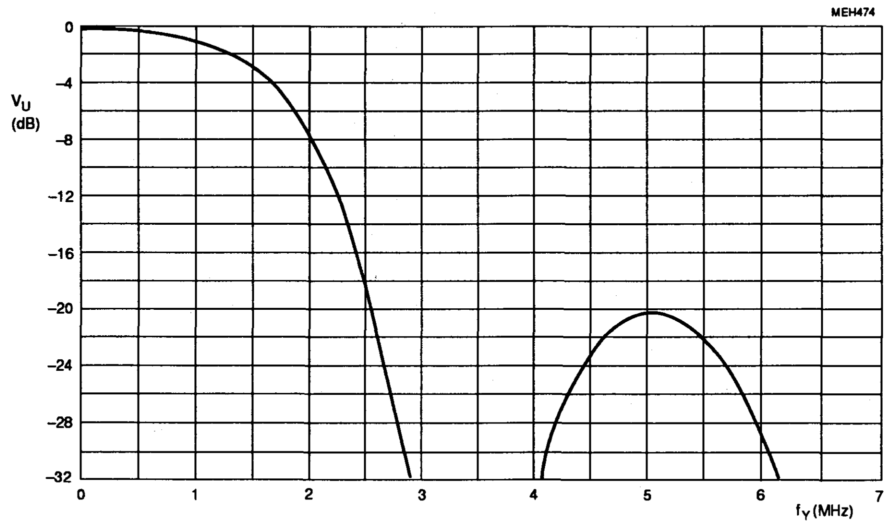


Fig.10 Interpolation filter at DCTI off with I^2C-bus control bits IFF = 0; IFC = 0 and IFL = 0 in 4:1:1 format and control bits IFF = 1; IFC = 0 and IFL = 0 in 4:2:2 format; 13.5 MHz data rate.

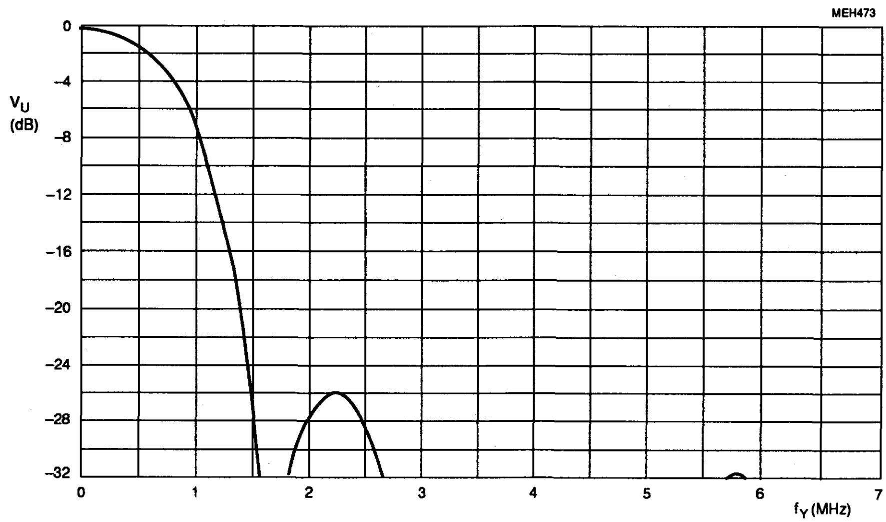


Fig.11 Interpolation filter at DCTI off with I^2C-bus control bits IFF = 0; IFC = 0 and IFL = 1 in 4:1:1 format and control bits IFF = 1; IFC = 0 and IFL = 1 in 4:2:2 format; 13.5 MHz data rate.

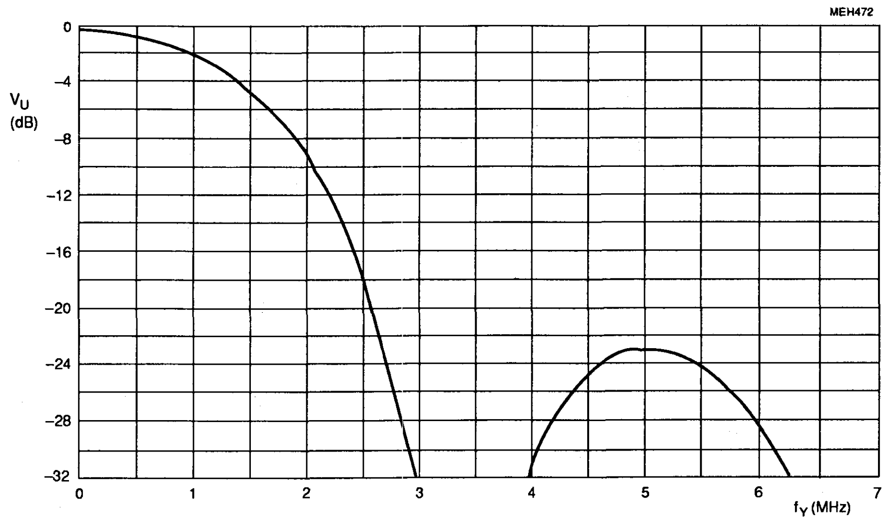


Fig.12 Interpolation filter at DCTI off with I²C-bus control bits IFF = 0; IFC = 1 and IFL = 0 in 4:1:1 format; 13.5 MHz data rate.

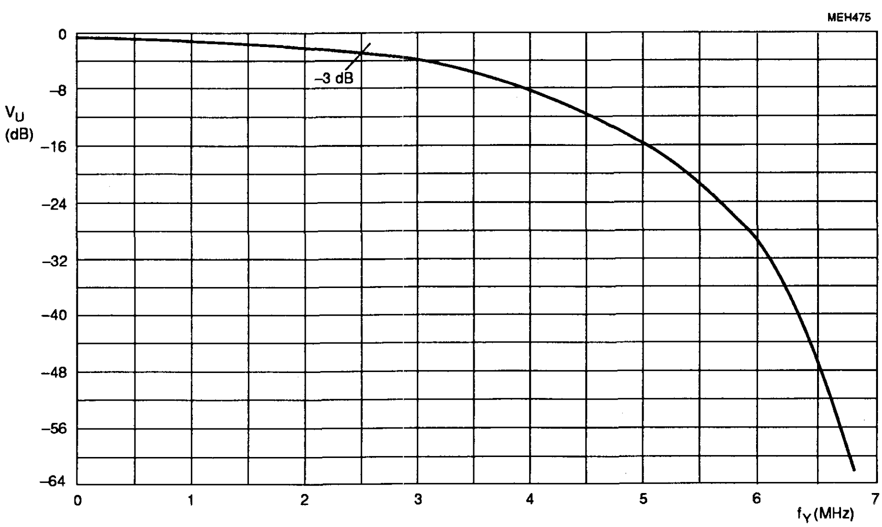


Fig.13 Interpolation filter with I²C-bus control bits IFF = 1; IFC = 1 and IFL = X in 4:2:2 format; 13.5 MHz data rate.

35 MHz triple 9-bit D/A converter for high-speed video

SAA7169

Supercedes data of January 1992

FEATURES

- CMOS circuit to convert high-speed video data from digital to analog
- Three equal 9-bit digital-to-analog converters
- Input signals TTL-compatible
- Input registers for positive edge-triggered data signals
- Clock frequency for a conversion rate up to 35 MHz
- 20 MHz analog bandwidth
- 2 V (p-p) analog output voltage range without load on output (0.2 to 2.2 V DC)
- 1 V / 75 Ω outputs (0.1 to 1.1 V DC); Fig.1
- No de-glitching circuit required
- Typical 225 mW power dissipation

GENERAL DESCRIPTION

The triple high-speed D/A converter can be used in applications for

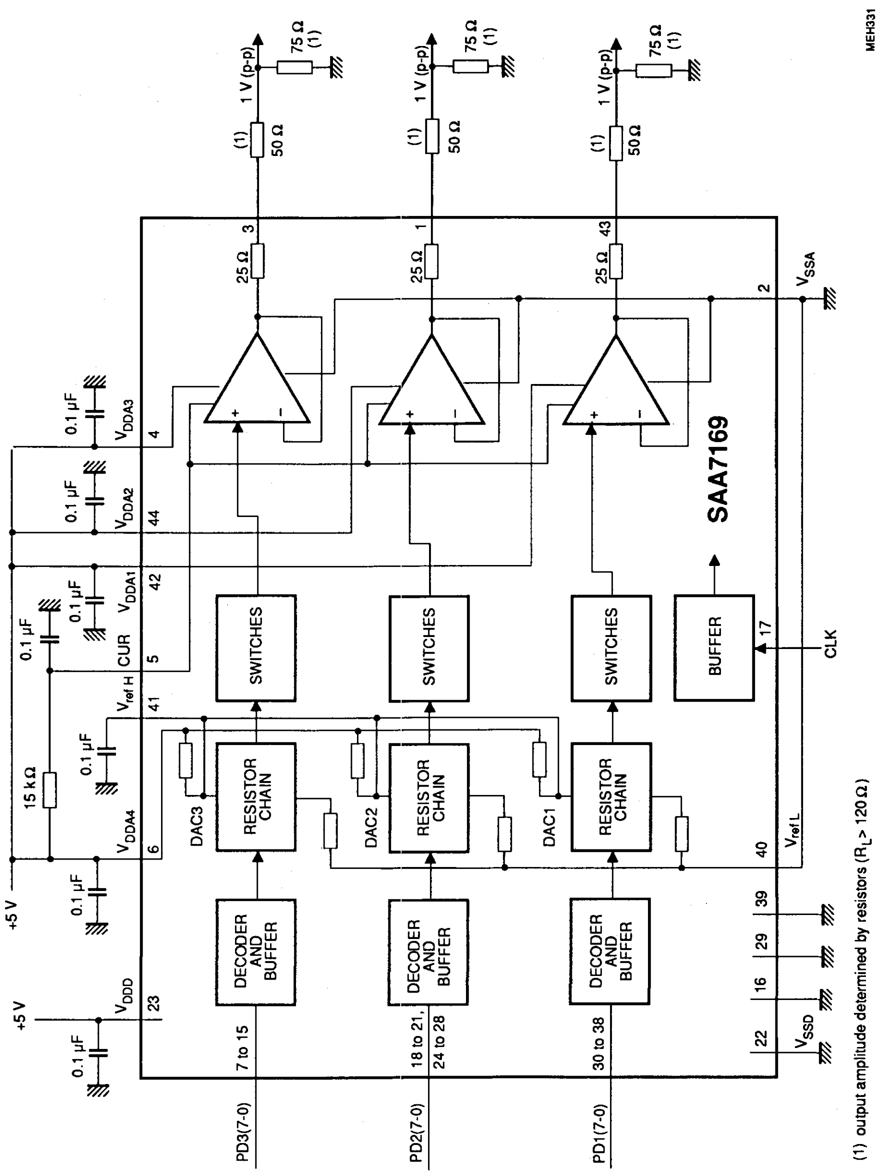
- desktop video processing
- digital television
- graphic displays
- television decoders
- general high frequency conversion

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage digital part	4.5	5	5.5	V
V_{DDA}	supply voltage analog part	4.75	5	5.25	V
$I_{DD\ tot}$	total supply current	-	-	38	mA
V_I	data input levels	TTL-compatible			
f_{CLK}	conversion frequency	1	-	35	MHz
V_o	nominal output amplitude on pins 1, 3, 43 (peak-to-peak value)	-	2	-	V
B	bandwidth (–3 dB)	20	-	-	MHz
DNL	differential non-linearity	-	-	±0.5	LSB
INL	integral non-linearity	-	-	±0.2	%
α_{CR}	crosstalk attenuation	48	-	-	dB
R_o	internal serial output resistance	-	25	-	Ω
R_L	output load resistance	125	-	-	Ω
T_{amb}	operating ambient temperature range	0	-	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7169	44	PLCC	plastic	SOT187



(1) output amplitude determined by resistors ($R_L > 120\,\Omega$)

Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{o\,2}$	1	analog output voltage of channel 2
V_{SSA}	2	analog ground (0 V)
$V_{o\,3}$	3	analog output voltage of channel 3
V_{DDA3}	4	+5 V supply voltage for buffer amplifier of channel 3
CUR	5	current input for analog output buffers, decoupled to V_{SSA}
V_{DDA4}	6	+5 V supply voltage for analog reference part
PD3(8)	7	9-bit data input of channel 3
PD3(7)	8	
PD3(6)	9	
PD3(5)	10	
PD3(4)	11	
PD3(3)	12	
PD3(2)	13	
PD3(1)	14	
PD3(0)	15	
i.c.	16	connect to digital ground (input not used)
CLK	17	clock frequency input
PD2(8)	18	9-bit data input of channel 2 (bits PD2(8-5))
PD2(7)	19	
PD2(6)	20	
PD2(5)	21	
V_{SSD}	22	digital ground (0 V)
V_{DDD}	23	+5 V supply voltage for digital part
PD2(4)	24	9-bit data input of channel 2 (bits PD2(4-0))
PD2(3)	25	
PD2(2)	26	
PD2(1)	27	
PD2(0)	28	
i.c.	29	connect to digital ground (input not used)
PD1(8)	30	9-bit data input of channel 1 (bits PD1(8-4))
PD1(7)	31	
PD1(6)	32	
PD1(5)	33	
PD1(4)	34	

SYMBOL	PIN	DESCRIPTION
PD1(3)	35	9-bit data input of channel 1 (bits PD1(3-0))
PD1(2)	36	
PD1(1)	37	
PD1(0)	38	
i.c.	39	connect to digital ground (input not used)
$V_{ref\ L}$	40	reference voltage LOW; analog ground (V_{SSA})
$V_{ref\ H}$	41	internal generated reference voltage HIGH, decoupled to V_{SSA}
V_{DDA1}	42	+5 V supply voltage for buffer amplifier of channel 1
$V_{o\ 1}$	43	analog output voltage of channel 1
V_{DDA2}	44	+5 V supply voltage for buffer amplifier of channel 2

PIN CONFIGURATION

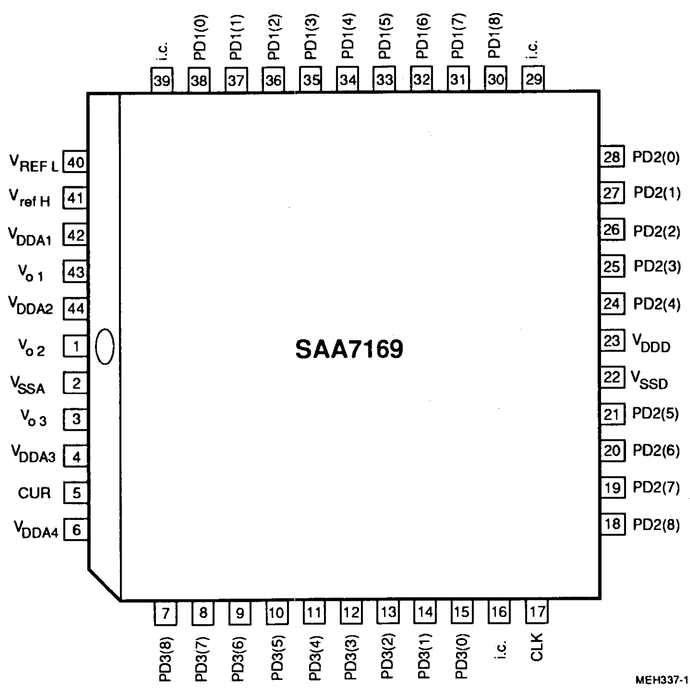


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The integrated monolithic CMOS circuit SAA7169 is a triple 9-bit digital-to-analog converter for high-speed video applications. Its three channels are equal. The maximum conversion rate is 35 MHz.

The converters use a combination of resistor chains with low-impedance output buffers. The bottom output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V. Fig.1 shows the application for 1 V/ 75 Ω outputs, using the serial 25 Ω + 50 Ω resistors.

Each digital-to-analog converter has its own supply pin for purpose of decoupling. V_{DDA4} is the supply voltage for the resistor chains of the three DACs. The accuracy of this supply voltage influences directly the output amplitudes.
The current CUR into pin 5 is 0.3 mA (V_{DDA4} = 5 V, $R_{5\text{-}6}$ = 15 kΩ); a larger current improves the bandwidth but increases the integral non-linearity.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage range (pin 23)	−0.3	7	V
V_{DDA1}	analog supply voltage range (pin 42)	−0.3	7	V
V_{DDA2}	analog supply voltage range (pin 44)	−0.3	7	V
V_{DDA3}	analog supply voltage range (pin 4)	−0.3	7	V
V_{DDA4}	analog supply voltage range (pin 6)	−0.3	7	V
$V_{diff\ GND}$	difference voltage $V_{SSD} - V_{SSA(1\ to\ 4)}$	-	±100	mV
V_n	voltage on all input pins 7 to 15, 18 to 21 and 24 to 40	−0.3	V_{DDD}	V
P_{tot}	total power dissipation	0	tbf	mW
T_{amb}	operating ambient temperature range	0	70	°C
T_{stg}	storage temperature range	−65	150	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; CLK = 35 MHz; f_{DATA} = 17.5 MHz (squarewave, full scale); T_{amb} = 0 to 70 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage range (pin 23)	for digital part	4.5	5	5.5	V
V_{DDA1}	supply voltage range (pin 42)	for buffer of DAC 1	4.75	5	5.25	V
V_{DDA2}	supply voltage range (pin 44)	for buffer of DAC 2	4.75	5	5.25	V
V_{DDA3}	supply voltage range (pin 4)	for buffer of DAC 3	4.75	5	5.25	V
V_{DDA4}	supply voltage range (pin 6)	DAC reference voltage	4.75	5	5.25	V
I_{DDD}	supply current	for digital part; note 1	-	-	20	mA
I_{DDA}	supply current (I_{DDA1} to I_{DDA4})	without load on outputs	-	-	18	mA
9-bit data inputs (pins 7 to 15; 18 to 21, 24 to 28 and 30 to 38)						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance		-	-	10	pF
I_{leak}	input leakage current		-	-	10	µA
t_{SU}	data set-up time	Fig.3	11	-	-	ns
t_{HD}	data hold time		3	-	-	ns
CLK input (pin 17)		Fig.3				
f_{CLK}	frequency range		1	-	35	MHz
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance		-	-	10	pF
I_{leak}	input leakage current		-	-	10	µA
t_{CLK}	cycle time		28.5	-	-	ns
t_{pH}	duty factor	$t_{CLK\,H}$ / t_{CLK}	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
Digital-to-analog converters (pins 5, 6 and 40)						
V_{DDA4}	reference input voltage for internal resistor chains (pin 6)		4.75	5	5.25	V
I_{CUR}	input current (pin 5)	R_{6-5} = 15 kΩ	-	-	400	µA
Analog outputs V_{o1}; V_{o2} and V_{o3} (pins 43, 1 and 3)						
V_o	nominal output signal (peak-to-peak value)	without load	-	2	-	V
$V_{43,1,3}$	minimum output voltage	without load; V_{DDA4} = 5 V	0.16	-	0.24	V
	maximum output voltage	without load; V_{DDA4} = 5 V	2.1	-	2.3	V
DTDM	DAC to DAC matching	between all channels	-	-	|30|	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B	output signal bandwidth	-3 dB	20	-	-	MHz
α_{CR}	crosstalk attenuation	note 2	48	-	-	dB
DNL	differential non-linearity	9-bit data; R_L = 125 Ω	-	-	±0.5	LSB
INL	integral non-linearity	9-bit data; R_L = 125 Ω	-	-	±0.2	%
$R_{43, 1, 3}$	internal serial output resistor		-	25	-	Ω
$R_{L\ 43, 1, 3}$	load resistance on output		125	-	-	Ω

Notes to the characteristics

1. With f_{CLK} = 35 MHz; f_{DATA} = 17.5 MHz (squarewave, full scale)
2. Crosstalk from channel to channel. One DAC with digital 5 MHz (sinusoidal, full scale) input signal, the other input data LOW. Measurements taken on outputs with 5.46 MHz filters (–3 dB at 5.87 MHz and –45 dB at 7.24 MHz).

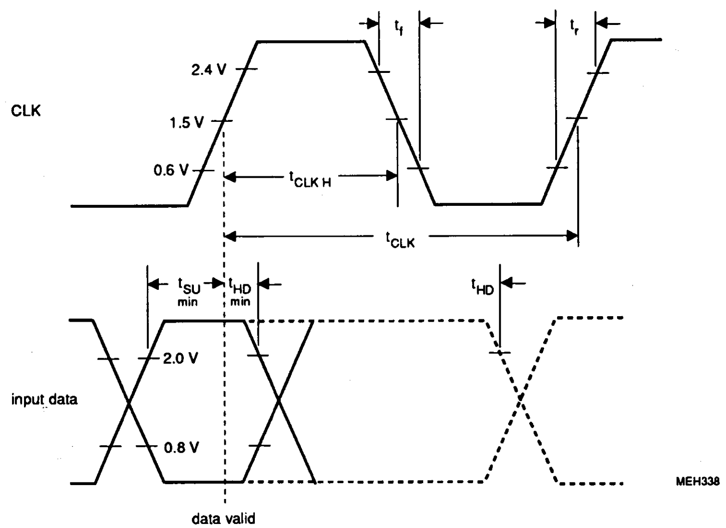


Fig.3 Input data timing.

Digital video scaler

SAA7186

1. FEATURES

- Scaling of video picture windows down to randomly sized windows
- Processes maximum 1023 pixels per line and 1023 lines per field
- Two-dimensional data processing for improved signal quality of scaled video data and for compression of video data
- 16-bit YUV input data buffer
- Interlace/non-interlace video data processing and field control
- Line memories in Y path and UV path to store two lines, each with 2 x 768 x 8 bit capacity
- Vertical sync processing by scale control
- Non-scaled mode to get full picture or to gate videotext lines
- UV input and output data binary/two's complement
- Switchable RGB matrix and anti-gamma ROMs
- 16-word FIFO register for 32-bit output data
- Output formats: 5-bit and 8-bit RGB, 8-bit YUV or 8-bit monochrome

2. GENERAL DESCRIPTION

The CMOS circuit SAA7186 scales and filters digital video data to randomly sized picture windows. YUV input data in 4:2:2 format are required (SAA7191B source).

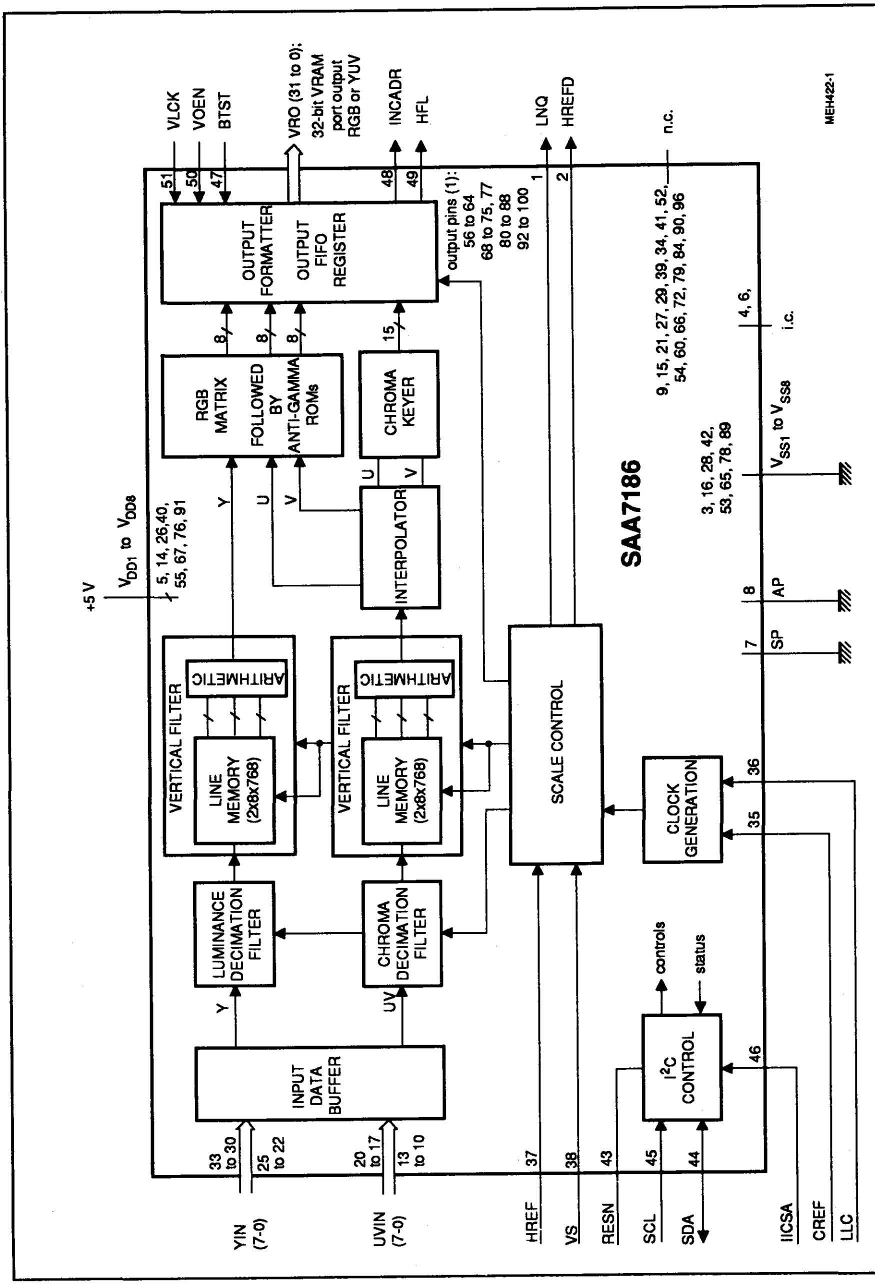
3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5	5.5	V
$I_{DD\ tot}$	total supply current (inputs LOW, without output load)	-	-	180	mA
V_I	data input level	TTL-compatible			
V_O	data output level	TTL-compatible			
LLC	input clock frequency	-	-	32	MHz
T_{amb}	operating ambient temperature range	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7186	100	QFP	plastic	SOT317

5. BLOCK DIAGRAM



(1) without pins 60, 72, 84 and 96, these pins are not connected

Fig.1 Block diagram.

6. PINNING

SYMBOL	PIN	STATUS	DESCRIPTION
LNQ	1	O	line qualifier signal; active polarity defined by QPL-bit in "10" (VCLK strobed)
HREFD	2	O	delay-compensated HREF output signal (VCLK strobed)
V_{SS1}	3	-	GND1 (0 V)
i.c.	4	-	internally connected
V_{DD1}	5	-	+5 V supply voltage 1
i.c.	6	-	internally connected
SP	7	I	connected to ground (shift pin for testing)
AP	8	I	connected to ground (action pin for testing)
n.c.	9	-	not connected
UVIN0 UVIN1 UVIN2 UVIN3	10 11 12 13	I I I I	time-multiplexed colour-difference input data (bits 0 to 3)
V_{DD2}	14	-	+5 V supply voltage 2
n.c.	15	-	not connected
V_{SS2}	16	-	GND2 (0 V)
UVIN4 UVIN5 UVIN6 UVIN7	17 18 19 20	I I I I	time- multiplexed colour-difference input data (bits 4 to 7)
n.c.	21	-	not connected
YIN0 YIN1 YIN2 YIN3	22 23 24 25	I I I I	luminance input data (bits 0 to 3)
V_{DD3}	26	-	+5 V supply voltage 3
n.c.	27	-	not connected
V_{SS3}	28	-	GND3 (0 V)
n.c.	29	-	not connected
YIN4 YIN5 YIN6 YIN7	30 31 32 33	I I I I	luminance input data (bits 4 to 7)
n.c.	34	-	not connected

SYMBOL	PIN	STATUS	DESCRIPTION
CREF	35	I	clock reference, external sync signal
LLC	36	I	line-locked system clock input signal (twice of pixel rate)
HREF	37	I	horizontal reference, pixel data clock signal (also present during vertical blanking)
VS	38	I	vertical sync input signal (approximately 6 lines long)
n.c.	39	-	not connected
V_{DD4}	40	-	+5 V supply voltage 4
n.c.	41	-	not connected
V_{SS4}	42	-	GND4 (0 V)
RESN	43	I	reset input (active-LOW for at least 30LLC periods)
SDA	44	I/O	IIC-bus data line
SCL	45	I	IIC-bus clock line
IICSA	46	I	set module address input of IIC-bus (LOW = B8, HIGH = BC)
BTST	47	I	output disable input; HIGH sets all data outputs to high-impedance state
INCADR	48	O	line increment / vertical reset control output line
HFL	49	O	FIFO register half-full flag output
VOEN	50	I	VRAM port output enable input (active-LOW)
VCLK	51	I	FIFO register clock input signal
n.c.	52	-	not connected
V_{SS5}	53	-	GND5 (0 V)
n.c.	54	-	not connected
V_{DD5}	55	-	+5 V supply voltage 5
VRO31 VRO30 VRO29 VRO28	56 57 58 59	O O O O	video output; 32-bit VRAM output port (bits 31 to 28)
n.c.	60	-	not connected
VRO27 VRO26 VRO25 VRO24	61 62 63 64	O O O O	video output; 32-bit VRAM output port (bits 27 to 24)
V_{SS6}	65	-	GND6 (0 V)
n.c.	66	-	not connected
V_{DD6}	67	-	+5 V supply voltage 6
VRO23 VRO22	68 69	O O	video output; 32-bit VRAM output port (bits 23 to 22)

SYMBOL	PIN	STATUS	DESCRIPTION
VRO21	70	O	video output; 32-bit VRAM output port (bits 21 to 20)
VRO20	71	O	
n.c.	72	-	not connected
VRO19	73	O	video output; 32-bit VRAM output port (bits 19 to 17)
VRO18	74	O	
VRO17	75	O	
V_{DD7}	76	-	+5 V supply voltage 7
VRO16	77	O	video output; 32-bit VRAM output port (bit16)
V_{SS7}	78	-	GND7 (0 V)
n.c.	79	-	not connected
VRO15	80	O	video output; 32-bit VRAM output port (bits 15 to 12)
VRO14	81	O	
VRO13	82	O	
VRO12	83	O	
n.c.	84	-	not connected
VRO11	85	O	video output; 32-bit VRAM output port (bits 11 to 8)
VRO10	86	O	
VRO9	87	O	
VRO8	88	O	
V_{SS8}	89	O	GND8 (0 V)
n.c.	90	-	not connected
V_{DD8}	91	-	+5 V supply voltage 8
VRO7	92	O	video output; 32-bit VRAM output port (bits 7 to 4)
VRO6	93	O	
VRO5	94	O	
VRO4	95	O	
n.c.	96	-	not connected
VRO3	97	O	video output; 32-bit VRAM output port (bits 3 to 0)
VRO2	98	O	
VRO1	99	O	
VRO0	100	O	

PIN CONFIGURATION

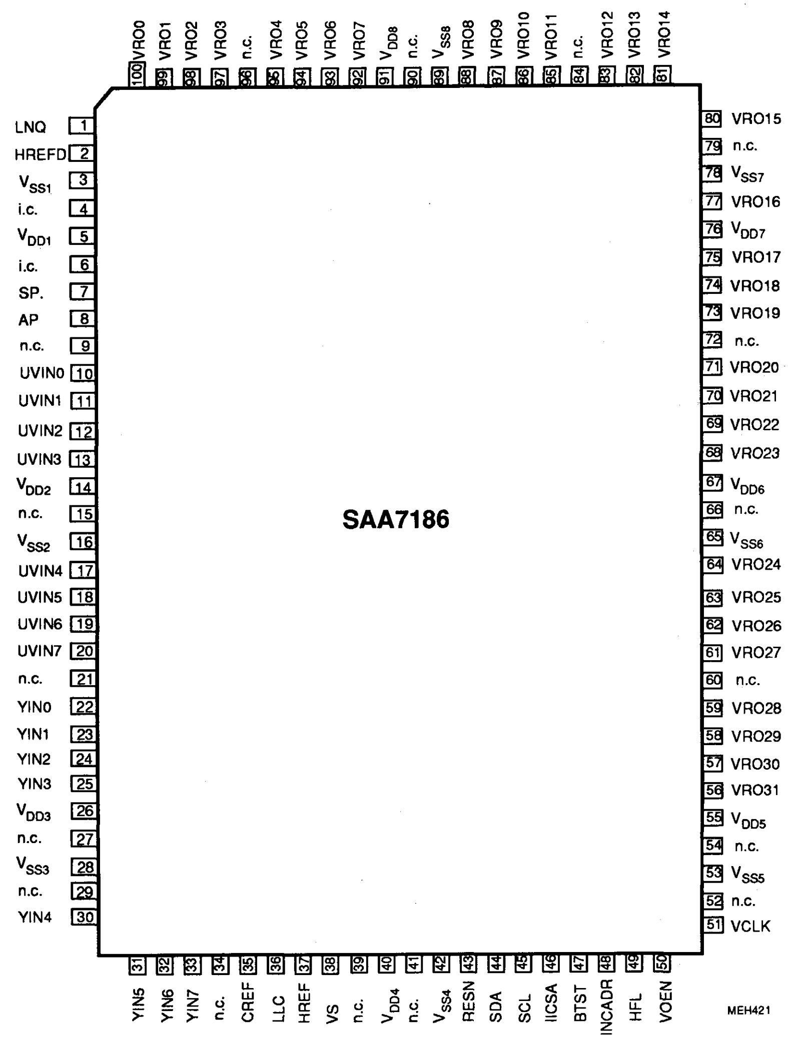


Fig.2 Pin configuration.

7. FUNCTIONAL DESCRIPTION

The input port is output of Philips digital video multistandard decoders (SAA7151B, SAA7191B) or other similar sources.
The SAA7186 input supports the 16-bit YUV 4:2:2 format.
The video data from the input port are converted into a unique internal two's complement data stream and are processed in horizontal direction in two separate decimation filters.Then they are processed in vertical direction by the vertical processing unit (VPU).
Chrominance data are interpolated to a 4:4:4 format; a chroma keying bit is generated.
The 4:4:4 YUV data are then converted from the YUV to the RGB domain in a digital matrix. ROM tables in the RGB data path can be used for anti-gamma correction of gamma-corrected input signals. Uncorrected RGB and YUV signals can be bypassed.
A scale control unit generates reference and gate signals for scaling of the processed video data. After data formatting to the various VRAM port formats, the scaled video data are buffered in the 16 word x 32-bit output FIFO register. The FIFO output is directly connected to the VRAM output bus VRO(31-0). Specific reference signals support an easy memory interfacing.
All functions of the SAA7186 are controlled via I^{2}C-bus using 17 subaddresses. The external microcontroller can get information by reading the status register.

Video input port

The 16-bit YUV input data in 4:2:2 format (Table 1) consist of 8-bit luminance data Y (pins YIN(7-0)) and 8-bit time-multiplexed colour-difference data UV (pins UVIN(7-0)).
The input data are clocked in by the signals LLC and CREF (Fig.3).
HREF and VS inputs define the video scan pattern (window).

Sequential input data

- are limited to maximum 768 active pixels per line if the vertical filter is active
- UV can be processed in straight binary and two's complement representation (controlled by TCC)

Decimation filters

The decimation filters perform accurate horizontal filtering of the input data stream.
Signal characteristics are matched in front of the pixel decimation stage, thus disturbing artifacts, caused by the pixel dropping, are reduced.
The signal bandwidth can be reduced in steps of:

2-tap filter = –6 dB at 0.325 pixel rate
3-tap filter = –6 dB at 0.25 pixel rate
4-tap filter = –6 dB at 0.21 pixel rate
5-tap filter = –6 dB at 0.125 pixel rate
9-tap filter = –6 dB at 0.075 pixel rate

The different characteristics are choosen dependent on the defined scaling parameters in an adaptive filter mode (AFS-bit = 1).
The filter characteristics can also be selected independently by control bits HF2 to HF0 at AFS-bit = 0.

Vertical filters

Y and UV data are handled in separate filters (Fig.1). Each of the two line memories has a capacity of 2 x 768 x 8-bit. Thus two complete video lines of 4:2:2 YUV data can be stored. The VPU is split into two memory banks and one arithmetic unit. The available processing modes, respectively transfer functions, are selectable by the bits VP1 and VP0 if AFS = 0.
An adaptive mode is selected by AFS = 1. Disturbing artifacts, generated by line dropping, are reduced.

Adaptive filter selection (AFS = 1):

scaling ratio	filter function (refer to I^{2}C section)
XD/XS	horizontal
≤1	bypassed
≤14/15	filter 1
≤11/15	filter 6
≤7/15	filter 3
≤3/15	filter 4
YD/YS	vertical
≤1	bypassed
≤13/15	filter 1
≤4/15	filter 2

RGB matrix

Y data and UV data are converted after interpolation into RGB data according to CCIR601 recommendation. Data are bypassed in YUV or monochrome modes.

Table 1 4 : 2 : 2 format (pixels per line). The time frames are controlled by the HREF signal.

INPUT	PIXEL BYTE SEQUENCE				
YIN7	Ye7	Yo7	Ye7	Yo7	Ye7
YIN6	Ye6	Yo6	Ye6	Yo6	Ye6
YIN5	Ye5	Yo5	Ye5	Yo5	Ye5
YIN4	Ye4	Yo4	Ye4	Yo4	Ye4
YIN3	Ye3	Yo3	Ye3	Yo3	Ye3
YIN2	Ye2	Yo2	Ye2	Yo2	Ye2
YIN1	Ye1	Yo1	Ye1	Yo1	Ye1
YIN0	Ye0	Yo0	Ye0	Yo0	Ye0
UVIN7	Ue7	Ve7	Ue7	Ve7	Ue7
UVIN6	Ue6	Ve6	Ue6	Ve6	Ue6
UVIN5	Ue5	Ve5	Ue5	Ve5	Ue5
UVIN4	Ue4	Ve4	Ue4	Ve4	Ue4
UVIN3	Ue3	Ve3	Ue3	Ve3	Ue3
UVIN2	Ue2	Ve2	Ue2	Ve2	Ue2
UVIN1	Ue1	Ve1	Ue1	Ve1	Ue1
UVIN0	Ue0	Ve0	Ue0	Ve0	Ue0
Y frame	0	1	2	3	4
UV frame	0		2		4

e = even pixel; o = odd pixel

The matrix equations are these considering the digital quantization:

$$R = Y + 1.375\,V$$
$$G = Y - 0.703125\,V - 0.34375\,U$$
$$B = Y + 1.734375\,U.$$

Anti-gamma ROM tables:
ROM tables are implemented at the matrix output to provide anti-gamma correction of the RGB data. A curve for a gamma of 1.4 is implemented

The tables can be used (RTB-bit = 0) to compensate gamma correction for linear data representation of RGB output data.

Chrominance signal keyer

The keyer generates an alpha signal to achieve a 5-5-5 +α RGB alpha output signal. Therefore, the processed UV data amplitudes are compared with thresholds set via I^2C-bus (subaddresses "0C to 0F").
A logical "1" signal is generated if the amplitude is inside the specified amplitude range, otherwise a logical "0" is generated.
Keying can be switched off by setting the lower limit higher than the upper limit ("0C or 0E" and "0D or 0F").

Scale control and vertical regions

The scale control block SC includes vertical address/sequence counters to define the current position in the input field and to address the internal VPU memories.
To perform scaling, XD of XS pixel selection in horizontal direction and YD of YS line selection in vertical direction are applied. The pixel and line dropping are controlled at the input of the FIFO register.
To control the decimation filter function and the vertical data processing in the adaptive mode

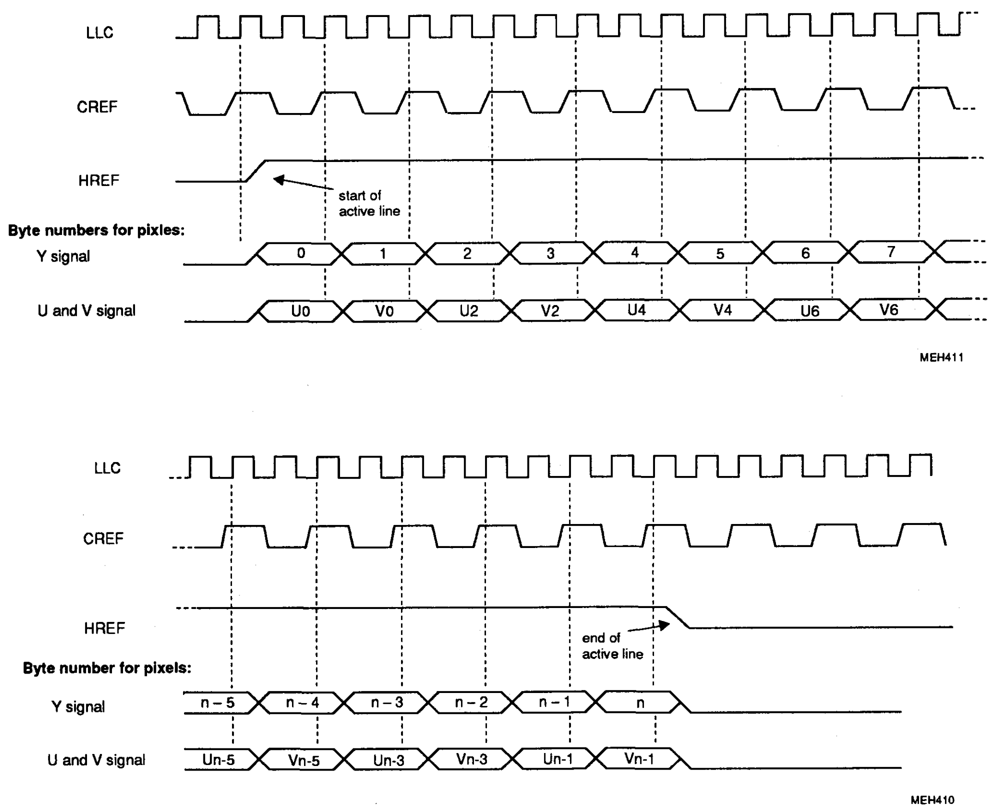


Fig.3 Horizontal and data multiplex timing.

(AFS = 1), the scaling ratio in horizontal and vertical direction is estimated in the SC block.

The input field can be divided into two vertical regions – the bypass region and the scaling region, which are defined via I²C-bus by the parameters VS, VC, YO and YS.

Vertical bypass region:

Data are not scaled and independent of I²C-bits FS1, FS0 the output format is always 8-bit grayscale (monochrome). The SAA7186 outputs all active pixels of a line, defined by the HREF input signal if the vertical bypass region is active. This can be used, for example, to store videotext information in the field memory.

The start line of the bypass region is defined by VS; the number of lines to be bypassed is defined by VC.

Vertical scaling region:

Data is scaled with start at line YO and the output format is selected when FS1, FS0 are valid.
This is the "normal operation" area.

The input/output screen dimensions in horizontal and vertical direction are defined by the parameters

XO, XS and XD for horizontal

YO, YS and YD for vertical.

The circuit processes XS samples of a line. Remaining pixels are ignored if a line is longer than XS. If a line is shorter than XS, processing is aborted when the falling edge of HREF is detected.

Vertical regions in Fig.4:

- the two regions can be programmed via I²C-bus, whereby regions should not overlap (active region overrides the bypass region).
- the start of a normal active picture depends on video standard and has to be programmed to the correct value.
- the offsets XO and YO have to be set according to the internal processing delays to ensure the complete number of destination pixels and lines (Table 6).
- the scaling parameters can be used to perform a panning function over the video frame/field.

Output data representation and levels

Output data representation of the YUV data can be modified by bit MCT (subaddress 10).
The DC gain is 1 for YUV input data. The corresponding RGB levels are defined by the matrix equations. The luminance levels are limited according to CCIR 601

16 (239) = black
235 (20) = white
(..) = grayscale luminance levels
if the YUV or monochrome luminance output formats are selected.

The signal levels of the RGB formats are limited in 8-bit to "0" or "255". For the 5-bit RGB formats a truncation from 8-bit to 5-bit is implemented.

Fill values are inserted dependent on longword position and destination size:

- "0" in RGB formats and for Y two´2 complement U, V
- "128" for U, V (straight binary)
- "255" in 8-bit grayscale format

The unused output values of the YUV and grayscale formats can be used for other purposes.

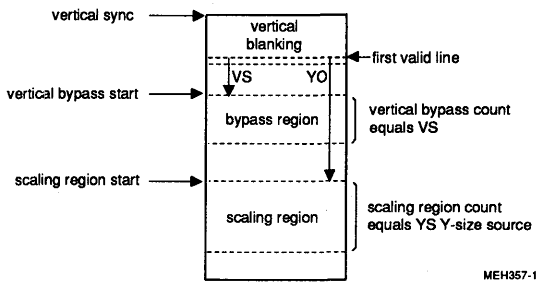


Fig.4 Vertical regions.

Table 2 VRAM port output data formats at EFE-bit = 0 dependend on FS1 and FS0 bits (set via I²C-bus)

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB 5-5-5 + 1 32-BIT WORDS			FS1 = 0; FS0 = 1 YUV 4:2:2 32-BIT WORDS			FS1 = 1; FS0 = 0 YUV 4:2:2 TEST 16-BIT WORDS			FS1 = 1; FS0 = 1 8-bit monochrome 32-BIT WORDS		
PIXEL ORDER	**n**	**n+2**	**n+4**	**n**	**n+2**	**n+4**	**n**	**n+1**	**n+2**	**n n+1**	**n+4 n+5**	**n+8 n+9**
VRO31	α	α	α	Ye7	Ye7	Ye7	Ye7	Yo7	Ye7	Ya7	Ya7	Ya7
VRO30	R4	R4	R4	Ye6	Ye6	Ye6	Ye6	Yo6	Ye6	Ya6	Ya6	Ya6
VRO29	R3	R3	R3	Ye5	Ye5	Ye5	Ye5	Yo5	Ye5	Ya5	Ya5	Ya5
VRO28	R2	R2	R2	Ye4	Ye4	Ye4	Ye4	Yo4	Ye4	Ya4	Ya4	Ya4
VRO27	R1	R1	R1	Ye3	Ye3	Ye3	Ye3	Yo3	Ye3	Ya3	Ya3	Ya3
VRO26	R0	R0	R0	Ye2	Ye2	Ye2	Ye2	Yo2	Ye2	Ya2	Ya2	Ya2
VRO25	G4	G4	G4	Ye1	Ye1	Ye1	Ye1	Yo1	Ye1	Ya1	Ya1	Ya1
VRO24	G3	G3	G3	Ye0	Ye0	Ye0	Ye0	Yo0	Ye0	Ya0	Ya0	Ya0
VRO23	G2	G2	G2	Ue7	Ue7	Ue7	Ue7	Ve7	Ue7	Yb7	Yb7	Yb7
VRO22	G1	G1	G1	Ue6	Ue6	Ue6	Ue6	Ve6	Ue6	Yb6	Yb6	Yb6
VRO21	G0	G0	G0	Ue5	Ue5	Ue5	Ue5	Ve5	Ue5	Yb5	Yb5	Yb5
VRO20	B4	B4	B4	Ue4	Ue4	Ue4	Ue4	Ve4	Ue4	Yb4	Yb4	Yb4
VRO19	B3	B3	B3	Ue3	Ue3	Ue3	Ue3	Ve3	Ue3	Yb3	Yb3	Yb3
VRO18	B2	B2	B2	Ue2	Ue2	Ue2	Ue2	Ve2	Ue2	Yb2	Yb2	Yb2
VRO17	B1	B1	B1	Ue1	Ue1	Ue1	Ue1	Ve1	Ue1	Yb1	Yb1	Yb1
VRO16	B0	B0	B0	Ue0	Ue0	Ue0	Ue0	Ve0	Ue0	Yb0	Yb0	Yb0
PIXEL ORDER	**n+1**	**n+3**	**n+5**	**n+1**	**n+3**	**n+5**	**OUTPUTS NOT USED**			**n+2 n+3**	**n+6 n+7**	**n+10 n+11**
VRO15	α	α	α	Yo7	Yo7	Yo7	X	X	X	Yc7	Yc7	Yc7
VRO14	R4	R4	R4	Yo6	Yo6	Yo6	X	X	X	Yc6	Yc6	Yc6
VRO13	R3	R3	R3	Yo5	Yo5	Yo5	X	X	X	Yc5	Yc5	Yc5
VRO12	R2	R2	R2	Yo4	Yo4	Yo4	X	X	X	Yc4	Yc4	Yc4
VRO11	R1	R1	R1	Yo3	Yo3	Yo3	X	X	X	Yc3	Yc3	Yc3
VRO10	R0	R0	R0	Yo2	Yo2	Yo2	X	X	X	Yc2	Yc2	Yc2
VRO9	G4	G4	G4	Yo1	Yo1	Yo1	X	X	X	Yc1	Yc1	Yc1
VRO8	G3	G3	G3	Yo0	Yo0	Yo0	X	X	X	Yc0	Yc0	Yc0
VRO7	G2	G2	G2	Ve7	Ve7	Ve7	X	X	X	Yd7	Yd7	Yd7
VRO6	G1	G1	G1	Ve6	Ve6	Ve6	X	X	X	Yd6	Yd6	Yd6
VRO5	G0	G0	G0	Ve5	Ve5	Ve5	X	X	X	Yd5	Yd5	Yd5
VRO4	B4	B4	B4	Ve4	Ve4	Ve4	X	X	X	Yd4	Yd4	Yd4
VRO3	B3	B3	B3	Ve3	Ve3	Ve3	X	X	X	Yd3	Yd3	Yd3
VRO2	B2	B2	B2	Ve2	Ve2	Ve2	X	X	X	Yd2	Yd2	Yd2
VRO1	B1	B1	B1	Ve1	Ve1	Ve1	X	X	X	Yd1	Yd1	Yd1
VRO0	B0	B0	B0	Ve0	Ve0	Ve0	X	X	X	Yd0	Yd0	Yd0

α = keying bit; R, G, B, Y. U and V = digital signals; e = even pixel number; o = odd pixel number;
a b c d = consecutive pixels

Table 3 VRAM port output data formats at EFE-bit = 1 dependend on FS1 and FS0 bits (set via I²C-bus)

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB 5-5-5 + 1 16-BIT WORDS			FS1 = 0; FS0 = 1 YUV 4:2:2 16-BIT WORDS			FS1 = 1; FS0 = 0 RGB 8-8-8 24-BIT WORDS			FS1 = 1; FS0 = 1 8-bit monochrome 16-BIT WORDS		
PIXEL ORDER	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n n+1**	**n+2 n+3**	**n+4 n+5**
VRO31	α	α	α	Ye7	Yo7	Ye7	R7	R7	R7	Ya7	Ya7	Ya7
VRO30	R4	R4	R4	Ye6	Yo6	Ye6	R6	R6	R6	Ya6	Ya6	Ya6
VRO29	R3	R3	R3	Ye5	Yo5	Ye5	R5	R5	R5	Ya5	Ya5	Ya5
VRO28	R2	R2	R2	Ye4	Yo4	Ye4	R4	R4	R4	Ya4	Ya4	Ya4
VRO27	R1	R1	R1	Ye3	Yo3	Ye3	R3	R3	R3	Ya3	Ya3	Ya3
VRO26	R0	R0	R0	Ye2	Yo2	Ye2	R2	R2	R2	Ya2	Ya2	Ya2
VRO25	G4	G4	G4	Ye1	Yo1	Ye1	R1	R1	R1	Ya1	Ya1	Ya1
VRO24	G3	G3	G3	Ye0	Yo0	Ye0	R0	R0	R0	Ya0	Ya0	Ya0
VRO23	G2	G2	G2	Ue7	Ve7	Ue7	G7	G7	G7	Yb7	Yb7	Yb7
VRO22	G1	G1	G1	Ue6	Ve6	Ue6	G6	G6	G6	Yb6	Yb6	Yb6
VRO21	G0	G0	G0	Ue5	Ve5	Ue5	G5	G5	G5	Yb5	Yb5	Yb5
VRO20	B4	B4	B4	Ue4	Ve4	Ue4	G4	G4	G4	Yb4	Yb4	Yb4
VRO19	B3	B3	B3	Ue3	Ve3	Ue3	G3	G3	G3	Yb3	Yb3	Yb3
VRO18	B2	B2	B2	Ue2	Ve2	Ue2	G2	G2	G2	Yb2	Yb2	Yb2
VRO17	B1	B1	B1	Ue1	Ve1	Ue1	G1	G1	G1	Yb1	Yb1	Yb1
VRO16	B0	B0	B0	Ue0	Ve0	Ue0	G0	G0	G0	Yb0	Yb0	Yb0
PIXEL ORDER	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n n+1**	**n+2 n+3**	**n+4 n+5**
VRO15	X	X	X	X	X	X	B7	B7	B7	X	X	X
VRO14	X	X	X	X	X	X	B6	B6	B6	X	X	X
VRO13	X	X	X	X	X	X	B5	B5	B5	X	X	X
VRO12	X	X	X	X	X	X	B4	B4	B4	X	X	X
VRO11	X	X	X	X	X	X	B3	B3	B3	X	X	X
VRO10	X	X	X	X	X	X	B2	B2	B2	X	X	X
VRO9	X	X	X	X	X	X	B1	B1	B1	X	X	X
VRO8	X	X	X	X	X	X	B0	B0	B0	X	X	X
VRO7(1)(2)	α	α	α	α	X	α	α	α	α	α	α	α
VRO6 (2)	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E
VRO5 (2)	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT
VRO4 (2)	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT
VRO3	X	X	X	X	X	X	X	X	X	X	X	X
VRO2 (2)	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF
VRO1 (2)	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ
VRO0 (2)	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ

α = keying bit; R, G, B, Y. U and V = digital signals; e = even pixel number; o = odd pixel number; a b c d = consecutive pixels; O/E = odd/even flag

(1) YUV 16-bit format: the keying signal α is defined only for YU time steps. The corresponding YV sample has also to be keyed. The α signal in monochrome mode can be used only in the transparent mode (TTR = 1), in this case Ya = Yb.

(2) Data valid only when transparent mode active (TTR-bit = 1) and VCLK pin connected to LLC/2 clock rate.

Output FIFO register and VRAM output port

The output FIFO register is the buffer between the video data stream and the VRAM data input port. Resized video data are buffered and formatted. 32-, 24- and 16-bit video data modes are supported. The various formats are selected by the bits EFE, FS1 and FS0. VRAM port formats are shown in Tables 2 and 3. The FIFO register capacity is 16 word x 32 bit (for 32-, 24-, or 16-bit video data). The bits LW1 and LW0 can be used to define the position of the first pixel each line in the 32-bit longword formats or to shift the UV sequence to VU in the 16-bit YUV formats (LW1 = 1).

VRAM port inputs are:
VCLK to clock the FIFO register output data and VOEN to enable output data.

VRAM port outputs are:
the HFL flag (half-full flag), the signal INCADR (refer to section "data burst transfer") and the reference signals for pixel and line selection on outputs VRO(7-0) (only for 24- and 16-bit video data formats refer to "transparent data transfer").

VRAM port transfer procedures

Data transfer on the VRAM port can be done asynchroneously controlled by outputs HFL, INCADR and input VCLK (data burst transfer with bit TTR = 0).

Data transfer on the VRAM port can be done synchroneously controlled by output reference signals on outputs VRO(7-0) and a clock rate of LLC/2 on input VCLK (transparent data transfer with bit TTR = 1 and EFE = 1).
The scaling capability of the SAA7186 can be used in various applications.

Data burst transfer mode

Data transfer on the VRAM port is asynchroneously (TTR = 0). This mode can be used for all output formats. Four signals for communication with the external memory are provided.

- HFL flag, the half-full flag of the FIFO output register is raised when the FIFO contains at least 8 data words (HFL = HIGH).
  By setting HFL = 1, the SAA7186 requests a data burst transfer by the external memory controller, that has to start a transfer cycle within the next 32 LLC cycles for 32-bit longword modes (16 LLC cycles for 16- and 24-bit modes).
  If there are pixels in the FIFO at the end of a line, which are not transferred, the circuit fills up the FIFO register with "fill pixels" until it is half-full and sets the HFL flag to request a data burst transfer.
  After transfer is done, HFL is used in combination with INCADR to indicate the line increments (Figures 6 and 7).
- INCADR output signal is used in combination with HFL to control horizontal and vertical address generation for a memory controller. The pulse sequence depends on field formats (interlace/ non-interlace or odd/even fields, Figures 6 and 7) and control bits OF (subaddress 00).

  HFL = 1 at the rising edge of INCADR:
  the end of line is reached, request for line address increment
  HFL = 0 at the rising edge of INCADR:
  the end of field/frame is reached, request for line and pixel addresses reset
  (The distance from the last half-full request HFL to the INCADR pulse may be longer than 64 x LLC. The HFL state is defined for minimum 4 x LLC in front of the rising edge of INCADR and minimum 2 x LLC afterwards.)
- VCLK input signal to clock the FIFO register output data VRO(n). New data are placed on the VRO(n) port with the rising edge of VCLK (Fig.5).
- VOEN input enables output data VRO(n).The outputs are in 3-state mode at VOEN = HIGH.
  VOEN changes only when VCLK is LOW. If VCLK pulses are applied during VOEN = HIGH, the outputs remain inactive, but the FIFO register accepts the pulses.

Transparent data transfer mode

Data transfer on the VRAM port can be achieved synchroneously (TTR =1). With a contineous clock rate of LLC/2 on input VCLK, the SAA7186 delivers a contineously processed data stream. Therefore, the extended formats of the VRAM output port have to be selected (bit EFE = 1; Table 3). The reference and gate signals on outputs VRO(6-1) and the LNQ signal are delivered in each field (means scaled and ignored fields). The PXO signal (also VRO0) is only delivered in active fields.
The output signals VRO(7-0) can be used to buffer qualified pre-processed RGB or YUV video data (notice: the YUV data are only valid in qualified time slots). Control output signals in Table 3 are:

α	keying signal of the chroma keyer
O/E	odd/even field bit according to the internal field processing
VGT	vertical gate signal, "1" marks the scaling window in vertical direction from YO to (YO + YS) lines, cut by VS.
HGT	horizontal gate signal, "1" marks horizontal direction from XO to (XO + XS) lines, cut by HREF.
HRF	delay compensated horizontal reference signal.
LNQ	line qualifier signal, active polarity is defined by QPL bit.
PXQ	pixel qualifier signal, active polarity is defined by QPP bit.

Power-on reset

- the FIFO register contents are undefined
- outputs VRO are set to high-impedance state
- output INCADR = HIGH
- output HFL = LOW until the VPE bit is set to "1"
- subaddress "10" is set to 00h and VPE-bit in subaddress "00" is set to zero (Table 4).

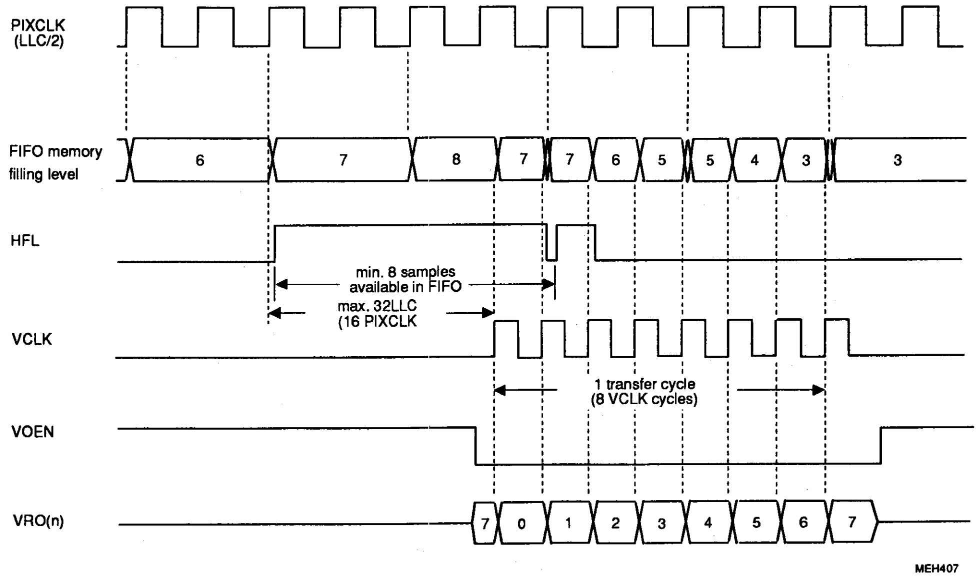


Fig.5 Output port transfer to VRAM at 32-bit data format without scaling. If VCLK cycles occur at VOEN = HIGH, the FIFO register is unchanged, but the outputs VRO(31-0) remain in 3-state position.

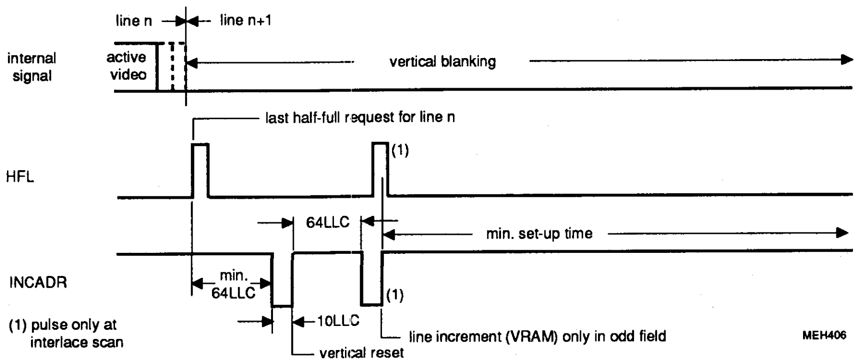


Fig.6 Vertical reset timing to the VRAM.

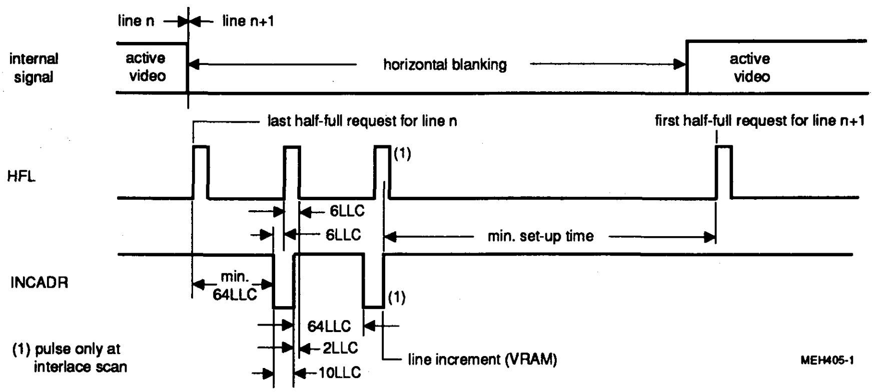


Fig.7 Horizontal increment timing to the VRAM.

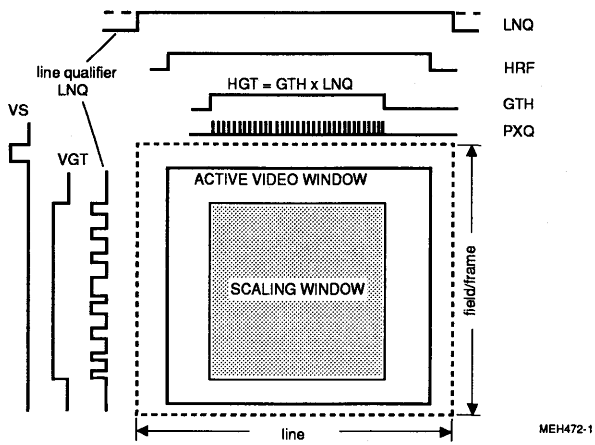


Fig.8 Reference signals for scaling window.

Field processing

The phase of the field sequence (odd/even dependent on inputs HREF and VS) is detected by means of the falling edge of VS. The current field phase is reported in the status byte by the OEF bit (Table 5). OEF bit can be stable 0 or 1 for non-interlaced input frames or non standard input signals VS and/or HREF (nominal condition for VS and HREF – SAA7191 B with active vertical noise limiter). A free-running odd/even flag is generated for internal field processing if the detection reports a stable OEF bit.

The POE bit (subaddress 0B) can be used to change the polarity of the internal flag (in case of non-standard VS and HREF signals) to control the phase of the free-running flag, and to compensate mis-detections. Thus, the SAA7186 can be used under various VS/HREF timing conditions.

The SAA7186 operates on fields. To support progressive displays and to avoid movement blurring and artifacts, the circuit can process both or single fields of interlaced or non-interlaced input data. Therefore the OF bits can be used. The bits OF1 and OF0 (Table 6) determine the INCADR/HFL generation in "data burst transfer mode". One of the fields (odd or even) is ignored when OF1 = 1; then no line increment sequence (INCADR/HFL) is generated, the vertical reset pulse is only generated.

With OF1 = OF0 = 0 the circuit supports correct interlaced data storage. Two INCADR/HFL sequences are generated in each qualified line; additionally an INCADR/HFL sequence after the vertical reset sequence of an odd field is generated. Thereby, the scaled lines are automatically stored in the right sequence.

8. OPERATION CYCLE

The operation is synchronized by the input field. The cycle is specified in the flow chart (Fig.9).
The circuit is inactive after power-on reset, VPO is 0 and the FIFO control is set "empty". The internal control registers are updated with the falling edge of VS signal. The circuit is switched active and waits for a transmission of VS and a vertical reset sequence to the memory controller. Afterwards, the circuit waits for the beginning of a scaling or bypass region. The processing of a current line is finished when a vertical sync pulse appears. The circuit performs a coefficient update and generates a new vertical reset (if it is still active).

Line processing starts when a line is decided to be active, the circuit starts to scale it. Active pixels are loaded into the FIFO register. An HFL flag is generated to initialize a data transfer when eight words are completed.
The line end is reached when the programmed pixel number is processed or when a horizontal sync pulse occurs. If there are pixels in the FIFO register, it is filled up until it is half-full to cause a data transfer. Horizontal increment pulses are transmitted after this data transfer.

Remarks:
The SAA7186 will always wait for the HREF/VS pulse before the line increment/vertical reset sequence is performed.
After each line/field, the FIFO control is set to empty when INCADR/HFL sequence is transmitted.
No additional actions are necessary if the memory controller has ignored the HFL signal. There is no need to handle overflow/underflow of the FIFO register.

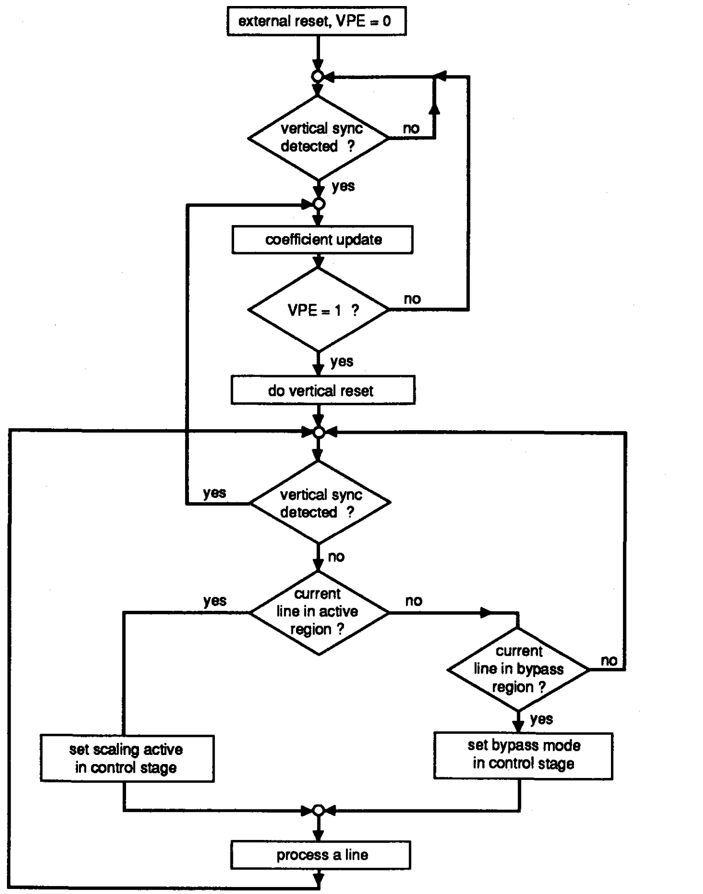


Fig.9 Operation cycle

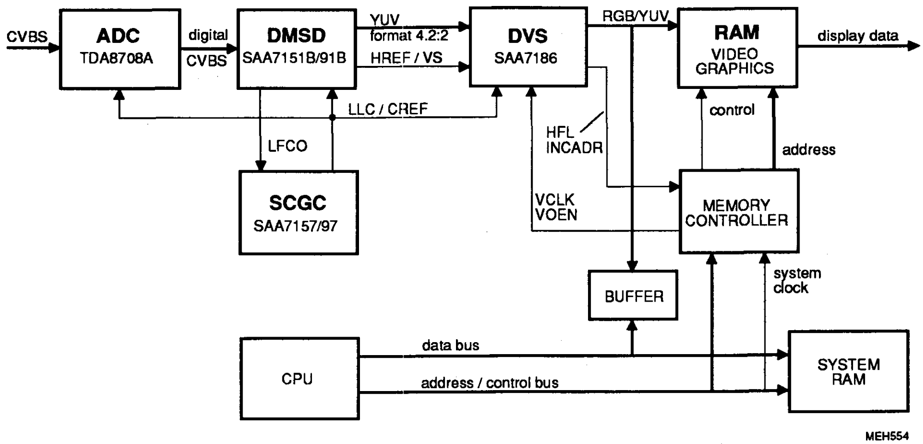


Fig.10 SAA7186 system configuration in Data Burst Transfer Mode
(TTR = , VCLK = continuous).

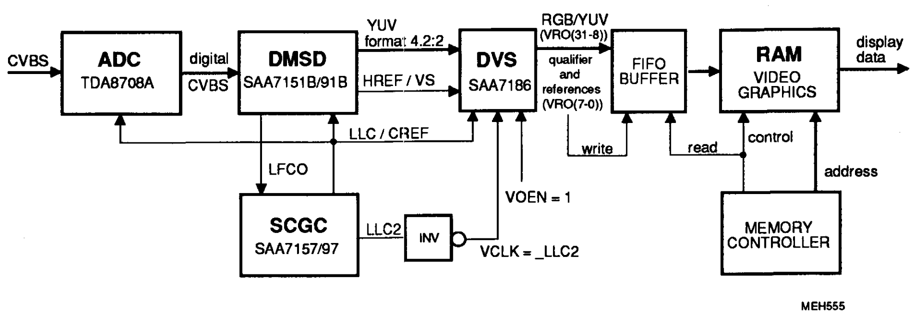


Fig.11 SAA7186 system configuration in Transparent Data Transfer Mode
(TTR = 1, EFE = 1, VCLK = continuous (_LLC2)).

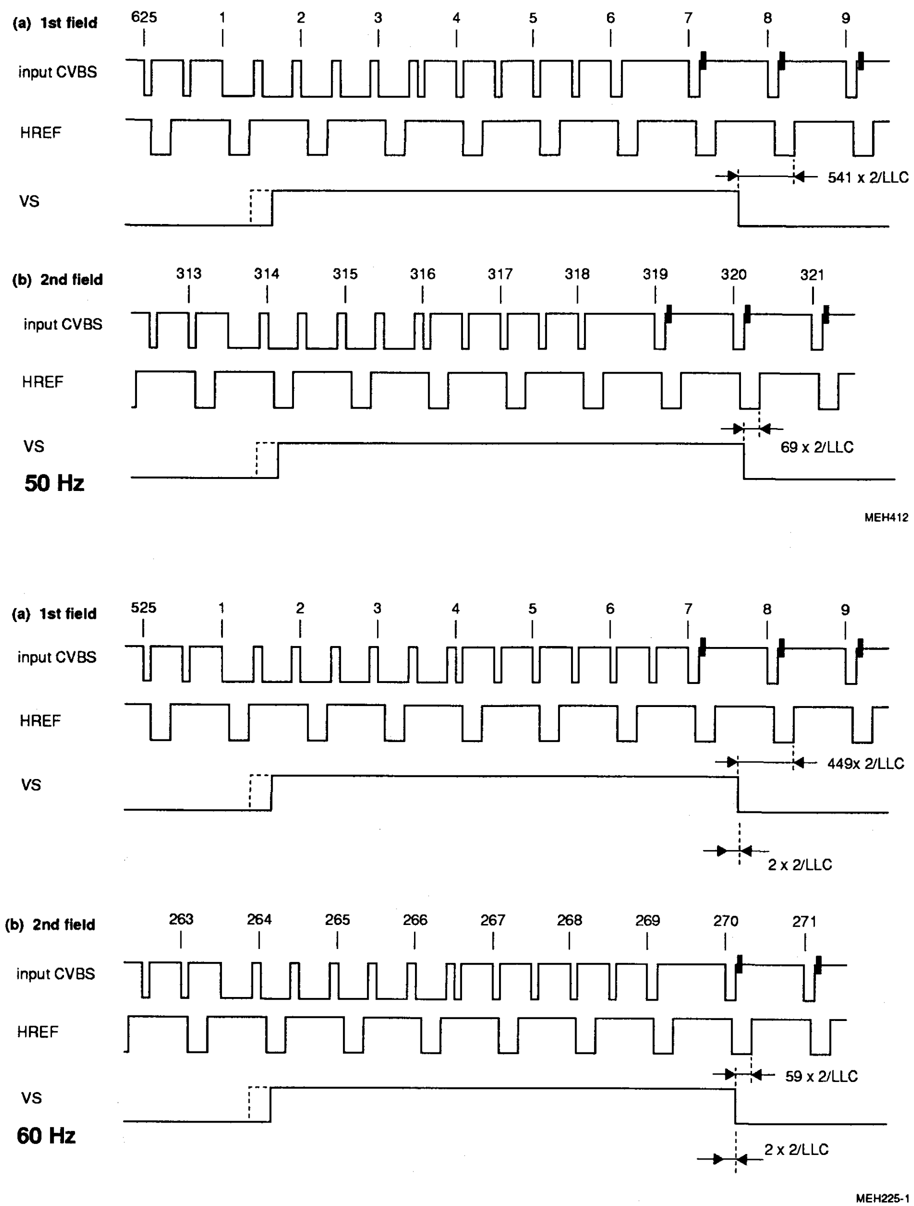


Fig.12 VS timing for video input source SAA7191B.

9. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A	-------	DATAn	A	P

S = start condition
SLAVE ADDRESS = **1011 100X** (IICSA = LOW) **or 1011 110X** (IICSA = HIGH)
A = acknowledge, generated by the slave
SUBADDRESS* = subaddress byte (Table 4)
DATA = data byte (Table 4)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I²C-bus; subaddress and data bytes for writing (X in address byte = 0).

FUNCTION	SUBADDRESS	DATA D7	D6	D5	D4	D3	D2	D1	D0	DF*
Formats and sequence	00	RTB	OF1	OF0	VPE	LW1	LW0	FS1	FS0	tbf
Output data pixel/line	01	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0	
continued in	04							XD9	XD8	
Input data pixel/line	02	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
continued in	04					XS9	XS8			
Horizontal window start	03	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0	
Pixel decimation filter	04	HF2	HF1	HF0	XO8	XS9	XS8	XD9	XD8	
Output data lines/field	05	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0	
continued in	09							YD9	YD8	
Input data lines/field	06	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
continued in	09					YS9	YS8			
Vertical window start	07	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0	
AFS/vertical processing	08	AFS	VP1	VP0	YO8	YS9	YS8	YD9	YD8	
Vertical bypass start	09	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0	
continued in	0B				VS8					
Vertical bypass count	0A	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	
continued in	0B	TCC	0	0	VS8	0	VC8	0	POE	
Chroma keying										
lower limit for V	0C	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	
upper limit for V	0D	VU7	VU6	VU5	VU4	VU3	VU2	VU1	VU0	
lower limit for U	0E	UL7	UL6	UL5	UL4	UL3	UL2	UL1	UL0	
upper limit for U	0F	UU7	UU6	UU5	UU4	UU3	UU2	UU1	UU0	
Byte 10**	10	0	0	0	MCT	QPL	QPP	TTR	EFE	
Unused	11 to 1F									

*) Default register contents fill in by hand
**) Byte 10 is set to 00h after power-on reset.

Table 5 I^2C-bus status byte (X in address byte = 1)

FUNCTION		DATA D7	D6	D5	D4	D3	D2	D1	D0
status byte		ID3	ID2	ID1	ID0	0	0	OEF	SVP

Function of status bits:

ID3 to ID0 — Software version of SAA7186 compatible with

ID3	ID2	ID1	ID0	version
0	0	0	1	1

OEF — Identification of field sequence dependent on inputs HREF and VS: 0 = even field detected; 1 = odd field detected

SVP — State of VRAM port: 0 = inputs HFL and INCADR inactive; 1 = inputs HFL and INCADR active.

Table 6 Function of the register bits of Table 4

"00"

RTB — ROM table bypass switch: 0 = anti-gamma ROM active; 1 = table is bypassed

OF1 to OF0 — Set output field mode:

OF1	OF0	field mode DVS process
0	0	both fields for interlaced storage
0	1	both fields for non-interlaced storage
1	0	odd fields only (even fields ignored) for non-interlaced storage
1	1	even fields only(odd fields ignored) for non-interlaced storage

VPE — VRAM port outputs enable: 0 = HFL and INCADR inactive; VRO outputs in 3-state position (HFL = LOW, INCADR = HIGH)
1 = HFL and INCADR enabled; VRO outputs dependent on VOEN

LW1 to LW0 — First pixel position in VRO data for FS1 = 0; FS0 = 0 (RGB) and FS1 = 0; FS0 = 1(YUV):

LW1	LW0	31 to 24	23 to 16	15 to 8	7 to 0	
0	0	pixel 0	pixel 0	pixel 1	pixel 1	EFE = 0, TRR = 0
0	1	pixel 0	pixel 0	pixel 1	pixel 1	
1	0	black	black	pixel 0	pixel 0	
1	1	black	black	pixel 0	pixel 0	

First pixel position in VRO data for FS1 = 1; FS0 = 1 (monochrome):

LW1	LW0	31 to 24	23 to 16	15 to 8	7 to 0	
0	0	pixel 0	pixel 1	pixel 2	pixel 3	EFE = 0, TRR = 0
0	1	black	pixel 0	pixel 1	pixel 2	
1	0	black	black	pixel 0	pixel 1	
1	1	black	black	black	pixel 0	
0	0	pixel 0	pixel 1	X	X	EFE = 1, TRR = 0; LW only effects the greyscale formar
0	1	black	pixel 0	X	X	
1	0	pixel 0	pixel 1	X	X	
1	1	black	pixel 0	X	X	

FS1 to FS0

FIFO output register format select (EFE- bit see "10"):

EFE	FS1	FS0	output format (Tables 2 and 3)
0	0	0	RGB 5-5-5 + alpa; 2x16-bit/pixel; 32-bit word length; RGB matrix on, VRAM output format
0	0	1	YUV 4:2:2; 2x16-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format
0	1	0	YUV 4:2:2; video test mode; 1x16-bit/pixel;16-bit word length; RGB matrix off, optional output format
0	1	1	monochrome mode; 4x8-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format
1	0	0	RGB 5-5-5 + alpa; 1x16-bit/pixel; 16-bit word length; RGB matrix on, VRAM output + transparent format
1	0	1	YUV 4:2:2 + alpa; 1x16-bit/pixel; 16-bit word length; RGB matrix off, VRAM output + transparent format
1	1	0	RGB 8-8-8 + alpa; 1x24-bit/pixel; 24-bit word length; RGB matrix on, VRAM output + transparent format
1	1	1	monochrome mode; 2x8-bit/pixel; 16-bit word length; RGB matrix off, VRAM output + transparent format

"01 and 04"
XD9 to XD0

Pixel number per line (straight binary) on output (VRO):
00 0000 0000 to 11 1111 1111 (number of XS pixels as a maximum)

"02 and 04"
XS9 to XS0

Pixel number per line (straight binary) on inputs (YIN and UVIN):
00 0000 0000 to 11 1111 1111 (number of input pixels per line as maximum)

"03 and 04"
XO8 to XO0

Horizontal start position (straight binary) of scaling window (take care of active pixel number per line).

start with 1st pixel after HREF rise = 0 0001 0000 to 1 1111 1111 (010 to 1FF)

window start and window end may be cut by internal delay compensated HREF = 0 phase. XO has to be matched to the internal processing delay to get full scaling range

"04"
HF2 to HF0

Horizontal decimation filter (Figures 13 and 14):

HF2	HF1	HF0	taps	filter
0	0	0	2	filter 1 $(1/2\,(1 + z^{-1}))$
0	0	1	3	filter 2 $(1/4\,(1 + 2z^{-1} + z^{-2}))$
0	1	0	5	filter 3 $(1/8\,(1 + 2z^{-1} + 2z^{-2} + 2z^{-3} + z^{-4}))$
0	1	1	9	filter 4 $(1/16\,(1 + 2z^{-1} + 2z^{-2} + 2z^{-3} + 2z^{-4} + 2z^{-5} + 2z^{-6} + 2z^{-7} + z^{-8}))$
1	0	0	1	filter bypassed
1	0	1	1	filter bypassed + delay in Y channel of 1T
1	1	0	8	filter 5 $(1/16\,(1 + 3z^{-1} + 3z^{-2} + z^{-3} + z^{-4} + 3z^{-5} + 3z^{-6} + z^{-7}))$
1	1	1	4	$(1/8\,(1 + 3z^{-1} + 3z^{-2} + z^{-3}))$

"05 and 08"
YD9 to YD0

Line number per output field (straight binary):
00 0000 0000 to 11 1111 1111 (number of YS lines as a maximum)

"06 and 08" YS9 to YS0	Line number per input field (straight binary): 00 0000 0000 0 line 11 1111 1111 1023 lines (maximum = number of lines/field – 3)
"07 and 08" YO8 to YO0	Vertical start of scaling window. "0" equals 3rd line after rising slope of VS input signal. Take care of active line number per field (straight binary). 0 0000 0000 start with 3rd line after the rising slope of VS 0 0000 0011 start with 1st line after the falling slope of nominal VS (SAA7151B/91B) 1 1111 1111 511 + 3 lines after the rising slope of VS (maximum value)
"08" AFS	Adaptive filter switch: 0 = off; use VP1, VP0 and HF2 to HF0 bits 1 = on; filter characteristics are selected by the scaler
VP1 to VP0	Vertical data processing VP1 VP0 | processing 0 0 | bypassed 0 1 | delay of one line $H(z) = z^{-H}$ 1 0 | vertical filter 1: $(H(z) = 1/2\ (1 + z^{-H}))$ 1 1 | vertical filter 2: $(H(z) = 1/4\ (1 + 2z^{-H} + z^{-2H}))$
"09 and 0B" VS8 to VS0	Vertical bypass start, sets begin of the bypass region (straight binary). Scaling region overrides bypass region (YO bits): 0 0000 0000 start with 3rd line after the rising slope of VS 0 0000 0011 start with 1st line after the falling slope of nominal VS (SAA7151B/91B) 1 1111 1111 511 + 3 lines after the rising slope of VS (maximum value)
"0A and 0B" VC8 to VC0	Vertical bypass count, sets length of bypass region (straight binary): 0 0000 0000 0 line length 1 1111 1111 511 lines length (maximum = number of lines/field – 3)
TCC	Two´s complement input data select (U, V): 0 = binary input data 1 = two`complement input data
POE	Polarity, internally detected odd/even flag O/E: 0 = flag unchanged; 1 = flag inverted
"0C" VL7 to VL0	Set lower limit for V colour-difference signal (8 bit; two´s complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"0D" VU7 to VU0	Set upper limit for V colour-difference signal (8 bit; two´s complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level

"0E" UL7 to UL0	Set lower limit for U colour-difference signal (8 bit; two´s complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"0F" UU7 to UU0	Set upper limit for U colour-difference signal (8 bit; two´s complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"10" MCT	Monochrome and two´s complement output data select: 0 = inverse grayscale luminance (if grayscale is selected by FS bits) or straight binary U, V data output 1 = non-inverse monochrome luminance (if grayscale is selected by FS bits) or two`complement U, V data output
QPL	Line qualifier polarity flag : 0 = LNQ is active-LOW (pin 1 and on VRO1, pin 99); 1 = LNQ is active-HIGH
QPP	Pixel qualifier polarity flag : 0 = PXQ is active-LOW (VRO0, pin 100); 1 = PXQ is active-HIGH
TTR	Transparent data transfer: 0 = normal operation (VRAM protocol valid,) 1 = FIFO register transparent (output FIFO in shift register mode)
EFE	Extended formats enable, FS-bits in subaddress "00"

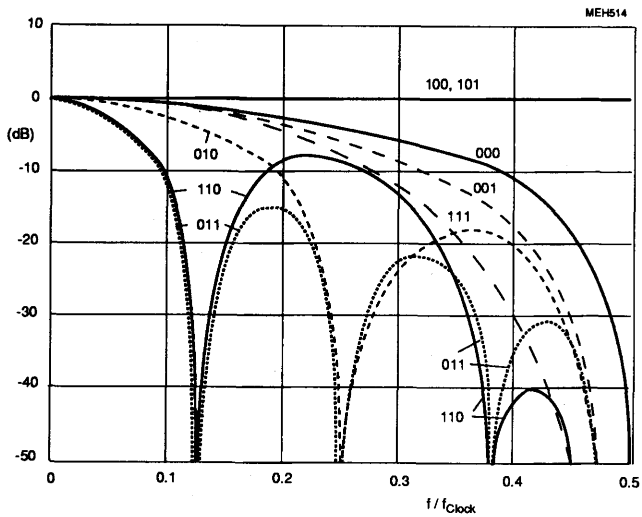


Fig.13 Horizontal frequency characteristic of luminance signal (Y) dependent on HF2 to HF0 bits (subaddress 04).

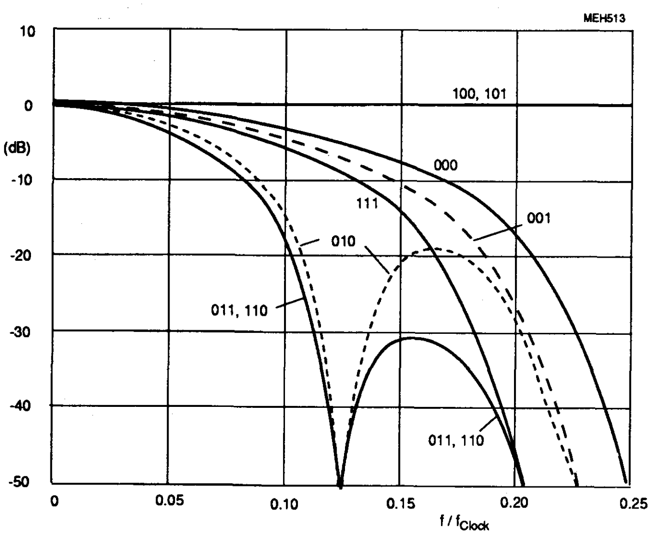


Fig.14 Horizontal frequency characteristic of chrominance signals (UV) without UV interpolation dependent on HF2 to HF0 bits (subaddress 04).

10. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 14, 26, 40, 55, 67, 76 and 91)	−0.5	6.5	V
V_I	DC input voltage on all pins	−0.5	V_{DD}	V
I_{DD}	supply current (pins 5, 14, 26, 40, 55, 67, 76 and 91)	-	70	mA
P_{tot}	total power dissipation	0	1	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±2000	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

11. DC CHARACTERISTICS

V_{DD1} to V_{DD8} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 14, 26, 40, 55, 67, 76 and 91)		4.5	5	5.5	V
I_P	total supply current ($I_{DD1} + I_{DD2} + I_{DD3}$ $I_{DD4} + I_{DD5} + I_{DD6} + I_{DD7} + I_{DD8}$)	inputs LOW and outputs without load	-	80	-	mA
Data and control inputs						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD}+0.5	V
I_{LI}	input leakage current	V_{IL} = 0	-	-	10	µA
C_I	input capacitance	data	-	-	8	pF
		clocks	-	-	10	pF
Data and control outputs						
V_{OL}	output voltage LOW	note 1	-	-	0.6	V
V_{OH}	outputt voltage HIGH	note 1	2.4	-	-	V
3-state outputs						
$I_{O\,off}$	high-impedance output current		-	-	±5	µA
C_O	high-impedance output capacitance		-	-	8	pF
I^2C-bus, SDA and SCL (pins 44 and 45)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3	-	V_{DD}+0.5	V
$I_{44,\,45}$	input current		-	-	±10	µA
I_{ACK}	output current on pin 44	acknowledge	3	-	-	mA
V_{OL}	output voltage at acknowledge	I_{44} = 3 mA	-	-	0.4	V

12. AC CHARACTERISTICS

V_{DD1} to V_{DD8} = 4.5 to 5.5 V; T_{amb} = 0 to 60 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LLC timing (pin 36)		Fig.11				
t_{LLC}	cycle time		31	-	45	ns
t_p	pulse width (duty factor)	$t_{LLC\,H}$ / t_{LLC}	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
Input data and CREF timing		Fig.15				
t_{SU}	setup time		11	-	-	ns
t_{HD}	hold time		3	-	-	ns
VCLK timing (pin 51)		Fig.16				
t_{VCLK}	VRAM port clock cycle time	note 2	50	-	200	ns
$t_{p\,L}$, $t_{p\,H}$	LOW and HIGH times	note 3	17	-	-	ns
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
Output data and reference signal timing		Figures 15 and 16				
C_L	load capacitance	VRO outputs	15	-	40	pF
		other outputs	7.5	-	25	pF
t_{OH}	VRO data hold time	C_L = 10 pF; note 4	0	-	-	ns
t_{OHL}	related to LLC (INCADR, HFL)	C_L = 10 pF; note 5	0		-	ns
t_{OHV}	related to VCLK (HFL)	C_L = 10 pF; note 5	0		-	ns
t_{OD}	VRO data delay time	C_L = 40 pF; note 4	-	-	25	ns
t_{ODL}	related to LLC (INCADR, HFL)	C_L = 25 pF; note 5	-	-	60	ns
t_{ODV}	related to VCLK (HFL)	C_L = 25 pF; note 5	-	-	60	ns
t_D	output disable time to 3-state	C_L = 40 pF; note 6	-	-	40	ns
t_E	output enable time from 3-state	C_L = 40 pF; note 6	-	-	40	ns
$t_{HFL\,VOE}$	HFL maximum response time	VRAM port enabled	-	-	810	ns
$t_{HFL\,VCLK}$	HFL maximum response time	HFL set at beginning of VCLK burst	-	-	840	ns

Notes to the caracteristics

1. Levels are measured with load circuit. VRO outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
2. Maximum t_{VCLK} = 200 ns for test mode only. The applicable maximum cycle time depends on data format, horizontal scaling and input data rate.
3. Measured at 1,5 V level; $t_{p\,L}$ may be unlimited.
4. Timings of VRO refer to the rising edge of VLCK.
5. The timing of INCADR refers to LLC; the rising edge of HFL always refers to LLC. During a VRAM transfer is the falling edge of HFL generated by VCLK. Both edges of HFL refer to LLC during horizontal increment and vertical reset cycles.
6. Asynchronous signals with timing refering to the 1.5 V switching point of VOEN input signal (pin 50).

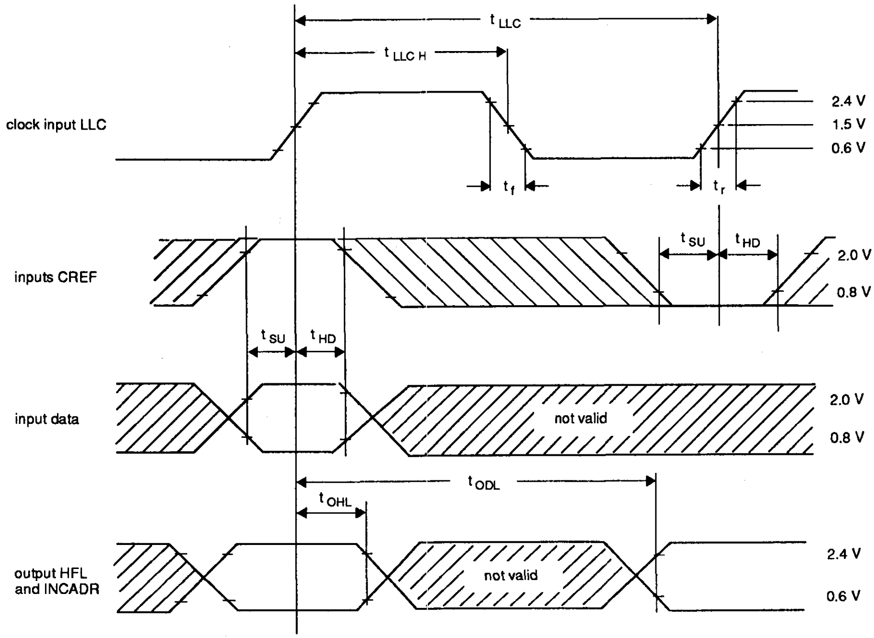


Fig.15 Data input timing (LLC).

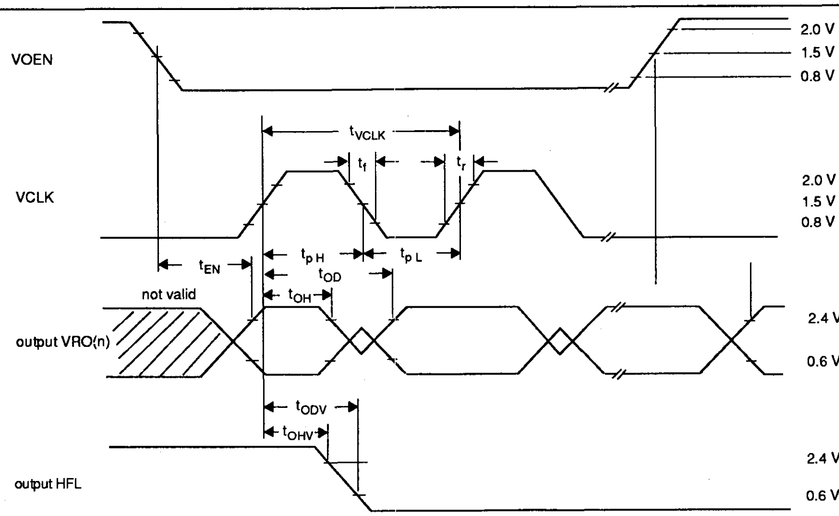


Fig.16 Data output timing (VCLK).

13. PROCESSING DELAYS

PORTS	DELAY IN LLC	REMARKS
YIN to VRO	58	in transparent mode only
UVIN to VRO	58	in transparent mode only
HREF to VRO	58	in transparent mode only

14. PROGRAMMING EXAMPLE

Slave address byte is B8h at pin IICSA = 0 (or BCh at pin IICSA = +5 V).
This example shows the setting via I^2C-bus for the processing of a picture segment at 1:1 horizontal and vertical scale.

Values in brackets [..]:
If no scaling or panning is wanted,
the parameters XD, XS, YD and YS should be set to the maximum value 3FFh.
the parameters XO and YO should be set to the minimum value 000h.
(in this case, HREF and VS from external define the SAA7186 processing window).

SUBADDR. (hex)	BITS	FUNCTION	VALUE (hex)	COMMENT
00	RTB, OF(1:0), VPE, LW(1:0), FS(1:0),	ROM table control and field sequence processing; VRAM port enable; output format select	11	(1)
01	XD(7:0)	LSB´s output pixel/line	80 [FF]	384 pixels out
02	XS(7:0)	LSB´s input pixel/line	80 [FF]	384 pixels in
03	XO(7:0)	LSB´s for horizontal window start	10 [00]	1st pixel after HREF = 1
04	HF(2:0), XO(8), XS(9, 8), XD(9, 8)	horizontal filter select and MSB´s of subaddresses 01, 02, 03	85 [8F]	horizontal filter bypassed
05	YD(7:0)	LSB´s output lines/field	90 [FF]	144 lines out
06	YS(7:0)	LSB´s input lines/field	90 [FF]	144 lines in
07	YO(7:0)	LSB´s vertical window start	03 [00]	1st line after VS = 0; (2)
08	AFS, VP(1:0), YO(8), YS(9, 8), YD(9, 8)	adaptive and vertical filter select; MSB´s of subaddresses 05, 06, 07	00 [FF]	no adaptive select vertical filter bypassed
09	VS(7:0)	LSB´s vertical bypass start position	00	not bypassed
0A	VC(7:0)	LSB´s vertical bypass lines/field	00	region
0B	VS(8), VC(8), TCC, POE	MSB´s of subaddresses 09, 0A; UV input data representation and odd/even polarity switch	00	defined; (3) (4)
0C	VL(7:0)	UV keyer: lower limit V (R-Y)	00	) keying is switched off
0D	VU(7:0)	UV keyer: upper limit V (R-Y)	FF	) by VU < VL
0E	UL(7:0)	UV keyer: lower limit U (B-Y)	00	-
0F	UU(7:0)	UV keyer: upper limit U (B-Y)	00	-
10	MCT, QPP, QPL, TTR, EFE	Y or UV output data representation, output data transfer mode, pixel/ line qualifier polarity.	00	(5)

Notes to the programming examples

(1) RTB = 0 ROM table is active (only for RGB formats)
OF = 00 SAA7186 processes the both fields for interlaced display
VPE = 1 VRAM port is enabled
LW = 00 longword position of first pixel in each output line = 0
FS = 01 16-bit 4:2:2 YUV output format is selected

(2) for nominal VS length of 6 x H-period (input SAA7191B respectively SAA7151B with active VNL)

(3) TTC = 0 straight binary UV input data expected

(4) odd/even polarity unchanged - can be used to change the field sequence if phase relations between HREF and VS are not according to SAA7191B respectively SAA7151B specification

(5) MCT = 0 when EFE, FS = 001h: UV output data are straight binary
QPP = 0 the pixel qualifier PXQ is "0"-active (if TTR, EFE = 1)
QPL = 0 line qualifier LNQ is "0"-active (if TTR, EFE = 1)
TTR = 0 VRAM port is set to data burst transfer
EFE = 0 32-bit longword formats selected.

Digital multistandard colour decoder, square pixel (DMSD-SQP)

SAA7191B

1. FEATURES

- Separate 8-bit luminance (Y or CVBS) and 8-bit chrominance inputs (CVBS or C) from CVBS, Y/C, S-Video (S-VHS or Hi8) sources
- Luminance and chrominance signal processing for standards PAL-B/G, NTSC-M, SECAM
- Horizontal and vertical sync detection for all standards
- Real-time control output RTCO to be used for frequency-locked digital video encoder (SAA7199B). RTCO contains serialized information about actual clock frequency, subcarrier frequency and PAL/SECAM sequence.
- Controls via the I^2C-bus
- User programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Cross-colour reduction by chrominance comb-filtering (NTSC) or by special cross colour cancellation (SECAM)
- 8-bit quantization of input signals
- 768/640 active samples per line equals 50/60 Hz (SQP)
- The YUV bus supports data rates of 780 x f_H equal to 12.2727 MHz for 60 Hz (NTSC-M) and 944 x f_H equal to 14.75 MHz for 50 Hz (PAL–B/G, SECAM) in 4 : 1 : 1 or 4 : 2 : 2 formats (via the I^2C-bus)
- One crystal oscillator of 26.8 MHz

2. GENERAL DESCRIPTION

The SAA7191B is a digital multistandard colour decoder suitable for 8-bit CVBS input signals or for 8-bit luminance and 8-bit chrominance input signals (Y/C).

The SAA7191B is down-compatible with SAA7191. The SAA7191B has additional outputs RTCO, GPSW0 and ODD. These new outputs are in high-impedance state when NFEN-bit = 0.

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage (pins 5, 18, 28, 37 and 52)	4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37 and 52)	-	100	250	mA
V_{IL}	input levels	TTL-compatible			
V_{OL}	output levels	TTL-compatible			
T_{amb}	operating ambient temperature	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7191B	68	PLCC	plastic	SOT188

5. BLOCK DIAGRAM

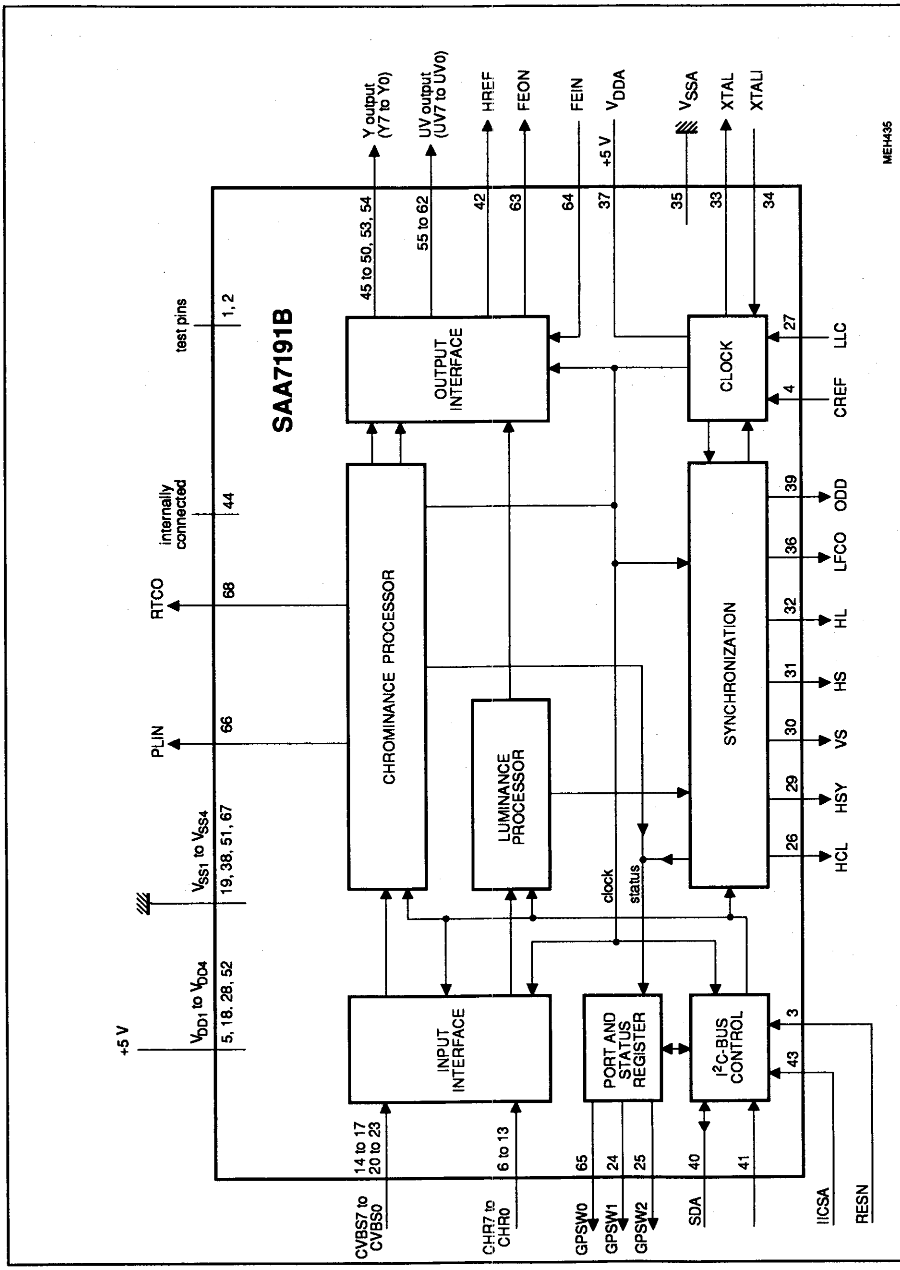


Fig.1 Block diagram.

6. PINNING

SYMBOL	PIN	DESCRIPTION
SP	1	connected to ground (shift pin for testing)
AP	2	connected to ground (action pin for testing)
RESN	3	reset, active LOW
CREF	4	clock reference, sync from external to ensure in-phase signals on the YUV-bus
V_{DD1}	5	+5 V supply input 1
CHR0	6	chrominance input data bits CHR7 to CHR0 from a Y/C (VHS, Hi8) source in two's complement format
CHR1	7	
CHR2	8	
CHR3	9	
CHR4	10	
CHR5	11	
CHR6	12	
CHR7	13	
CVBS0	14	luminance respectively CVBS lower input data bits CVBS3 to CVBS0 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS1	15	
CVBS2	16	
CVBS3	17	
V_{DD2}	18	+5 V supply input 2
V_{SS1}	19	ground 1 (0 V)
CVBS4	20	luminance respectively CVBS upper input data bits CVBS7 to CVBS4 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS5	21	
CVBS6	22	
CVBS7	23	
GPSW1	24	Port 1 output for general purpose (programmable)
GPSW2	25	Port 2 output for general purpose (programmable)
HCL	26	black level clamp pulse (programmable), e.g. for TDA8708 (ADC)
LLC	27	line-locked clock input signal (29.5 MHz for 50 Hz system; 24.5454 MHz for 60 Hz system)
V_{DD3}	28	+5 V supply input 3
HSY	29	horizontal sync indicator output signal (programmable), e.g. for TDA8708 (ADC)
VS	30	vertical sync output signal
HS	31	horizontal sync output signal (programmable)
HL	32	horizontal lock flag, HIGH = PLL locked
XTAL	33	26.8 MHz clock output
XTALI	34	26.8 MHz connection for crystal or external oscillator (TTL compatible squarewave)

SYMBOL	PIN	DESCRIPTION
V_{SSA}	35	analog ground
LFCO	36	line frequency control output signal, multiple of horizontal frequency (7.375 MHz/6.136363 MHz)
V_{DDA}	37	+5 V supply input for analog part
V_{SS2}	38	ground 2 (0 V)
ODD	39	odd/even field identification output (odd = HIGH); active only at NFEN-bit = 1
SDA	40	I^2C-bus data line
SCL	41	I^2C-bus clock line
HREF	42	horizontal reference output for valid YUV data (for active line 768Y or 640Y samples long)
IICSA	43	set module address input (LOW = 1000 101X; HIGH = 1000 111X)
i.c.	44	internally connected
Y7	45	Y signal output bits Y7 to Y2 (luminance), part of the digital YUV-bus
Y6	46	
Y5	47	
Y4	48	
Y3	49	
Y2	50	
V_{SS3}	51	ground 3 (0 V)
V_{DD4}	52	+5 V supply input 4
Y1	53	Y signal output bits Y1 to Y0 (luminance), part of the digital YUV-bus
Y0	54	
UV7	55	UV signal output bits UV7 to UV0 (colour-difference), part of the digital YUV-bus
UV6	56	
UV5	57	
UV4	58	
UV3	59	
UV2	60	
UV1	61	
UV0	62	
FEON	63	output active flag (active LOW when Y and UV data in high-impedance state)
FEIN	64	fast enable input (active LOW to control fast switching due to YUV data)
GPSW0	65	Port 0 output for general purpose (programmable); active only at NFEN-bit = 1
PLIN	66	PAL flag (active LOW at inverted line); SECAM flag (LOW equals DR, HIGH equals DB line)
V_{SS4}	67	ground 4 (0 V)
RTCO	68	real-time control output active at NFEN-bit = 1; Fig.7

Digital multistandard colour decoder, square pixel (DMSD-SQP)

PIN CONFIGURATION

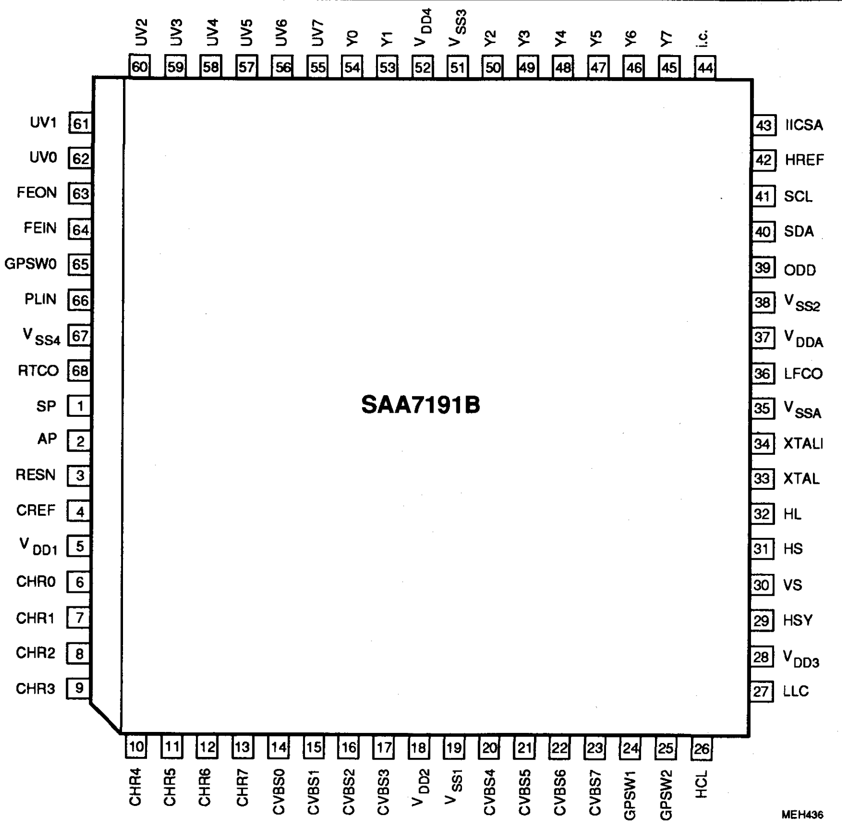


Fig.2 Pin configuration.

7. FUNCTIONAL DESCRIPTION

Chrominance processor

The 8-bit chrominance input signal (CVBS or chrominance format). passes a bandpass filter to eliminate DC components and to decimate the sample rate before it is fed to the two multipliers (quadrature demodulator), Fig.3(a).

Two subcarrier signals from a local oscillator (0 and 90 degree) are fed to the multiplicator inputs of the multipliers. The multipliers operate as a quadrature demodulator for all PAL and NTSC signals; it operates as a frequency down-mixer for SECAM signals.

The two multiplier output signals are converted to a serial data stream and applied to three low-pass filter stages, then to a gain controlled amplifier. A final multiplexed low-pass filter achieves, together with the preceding stages, the required bandwidth performance.

The signals, originated from PAL and NTSC, are applied to a comb-filter.

The signals, originated from SECAM, are fed through a Cloche filter (0 Hz centre frequency), a phase demodulator and a differentiator to obtain frequency-demodulated colour-difference signals.

The SECAM signals are fed after de-emphasis to a cross-over switch, to provide the both serial-transmitted colour-difference signals. These signals are fed finally to the output formatter stages and to the output interface.

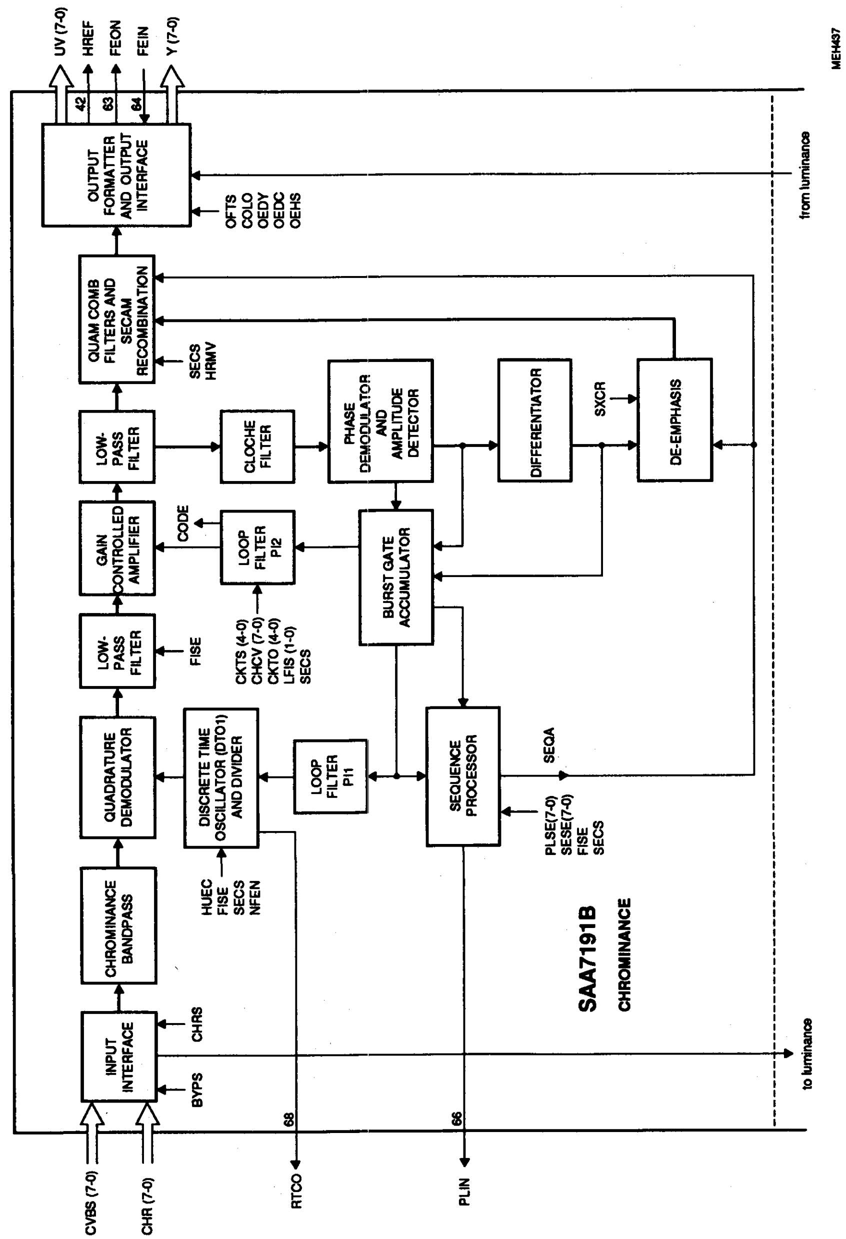


Fig.3(a) Detailed block diagram; continued in Fig.3(b).

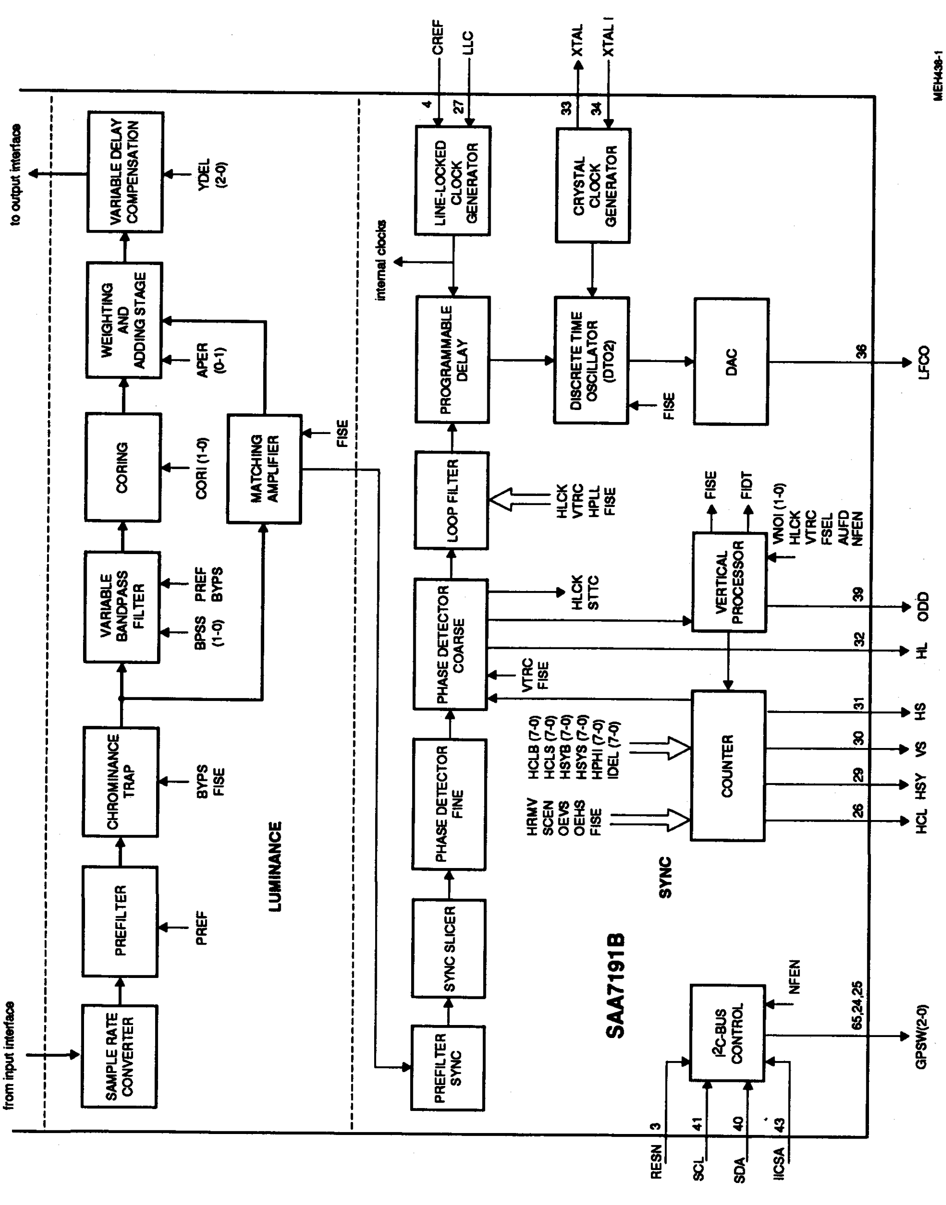


Fig.3(b) Detailed block diagram; continued from Fig.3(a).

Luminance processor

The luminance input signal, a digital CVBS format or an 8-bit luminance format (S-VHS, Hi8), is fed through a sample rate converter to reduce the data rate to 14.75 MHz for PAL and SECAM (12.2727 MHz for NTSC), Fig.3(b).

Sample rate is converted by means of a switchable pre-filter. High frequency components are emphasized to compensate for loss in the following chrominance trap filter. This chrominance trap filter (f_0 = 4.43 MHz or f_0 = 3.58 MHz centre frequency selectable) eliminates most of the colour carrier signal, therefore, it must be by-passed for S-Video (S-VHS and Hi8) signals.
The high frequency components of the luminance signal can be "peaked" (control for sharpness improvement via the I²C-bus) in two bandpass filters with selectable transfer characteristic.
A coring circuit with selectable characteristic improves the signal once more, this signal is then added to the original ("unpeaked") signal. A switchable amplifier achieves a common DC amplification, because the DC gains are different in both chrominance trap modes.
The improved luminance signal is fed to the variable delay compensation.

Processing delay

The delay from input to output is 220 LLC cycles if YDEL is set to 0. The processing delay will be influenced in future enhancements.

Synchronization

The luminance output signal is fed to the synchronization stage. Its bandwidth is reduced to 1 MHz in a low-pass filter. The sync pulses are sliced and fed to the phase detectors to be compared with the sub-divided clock frequency.
The resulting output signal is applied to the loop filter to accumulate all phase deviations. Adjustable output signals (e. g. HCL and HSY) are generated according to peripheral requirements (TDA8708A, TDA8709A). The output signals HS, VS and PLIN are locked to the timing reference signal HREF (Figures 6 and 7).
There is no absolute timing reference guaranteed between the input signal and the HREF signal as further improvements to the circuit may change the total processing delay.
It is therefore not recommended to use them for applications, which ask for absolute timing accuracy to the input signals.
The loop filter signal drives an oscillator to generate the line frequency control output signal LFCO.

Table 1 Clock frequencies in MHz for 50/60 Hz systems

CLOCK	50 Hz	60 Hz
LLC	29.5	24.545454
LLC2	14.75	12.272727
LLC4	7.375	6.136136
LLC8	3.6875	3.068181

Line locked clock frequency

LFCO is required in an external PLL (SAA7197) to generate the line locked clock frequency.

YUV-bus, digital outputs

The 16-bit YUV-bus transfers digital data from the output interfaces to a feature box, or to the digital-to-analog converter (DAC). Outputs are controlled via the I²C-bus in normal selections, or they are controlled by output enable chain (FEIN on pin 64, Fig.4).
The YUV-bus data rate equals LLC2 in Table 1. Timing is achieved by marking each second positive rising edge of the clock LLC in conjunction with CREF (clock reference).

YUV-bus formats 4:2:2 and 4:1:1

The output signals Y7 to Y0 are the bits of the digital luminance signal. The output signals UV7 to UV0 are the bits of the multiplexed colour-difference signals (B–Y) and (R–Y). The frame in the following tables is the time, required to transfer a full set of samples. In case of 4 : 2 : 2 format two luminance samples are transmitted in comparision to one U and one V sample within one frame.

Table 2 4 : 2 : 2 format
(768 pixels per line for 50 Hz system; 640 pixels per line for 60 Hz system)

OUTPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Notes to Table 2

1. Data rate: LLC2
2. Sample frequency:
   Y LLC2
   U LLC4
   V LLC4

The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

Table 3 4 : 1 : 1 format (768 pixels per line for 50 Hz system and 640 pixels per line for 60 Hz system)

OUTPUT	PIXEL BYTE SEQUENCE							
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7 (MSB)	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

Fast enable is achieved by setting input FEIN to LOW. This signal is used to control fast switching on the digital YUV-bus. HIGH on this pin forces the Y and U/V outputs to a high-impedance state. The signal FEON is LOW when the Y and U/V outputs are in this high-impedance state (Fig.4).
The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

Notes to Table 3

Data rate:		LLC2
sample frequency:	Y	LLC2
	U	LLC8
	V	LLC8

Table 4 Digital output control

OEDY	OEDC	FEIN	Y(7:0)	UV(7:0)	FEON
X	X	0	active	active	1
0	0	1	Z	Z	0
0	1	1	Z	active	1
1	0	1	active	Z	1
1	1	X	active	active	1

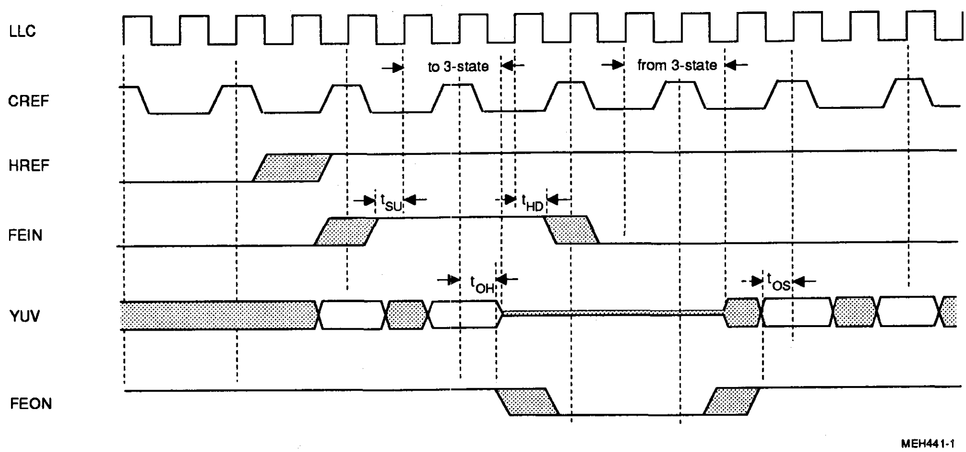


Fig.4 Timing example of fast enable input FEIN.

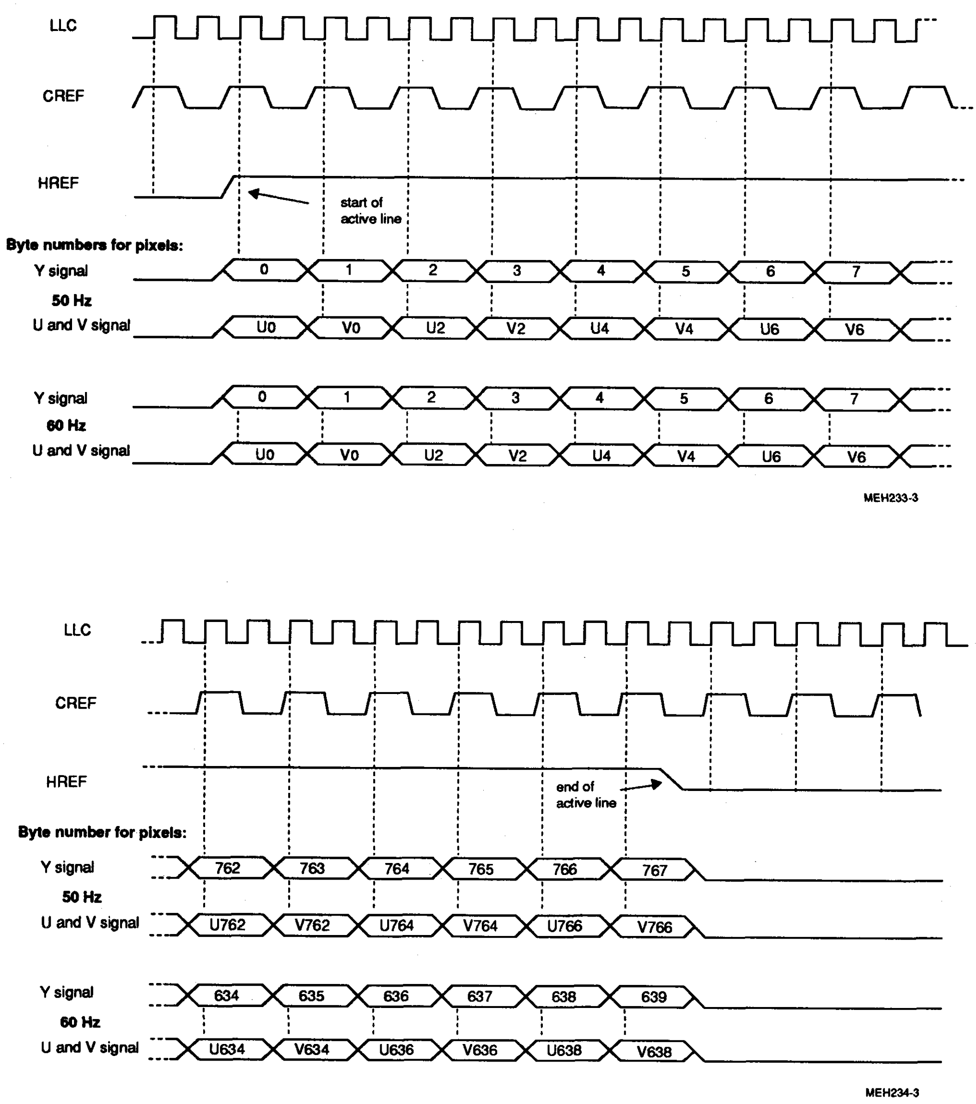


Fig.5 Line control by HREF in 4:2:2 format for 50 Hz and 60 Hz systems.

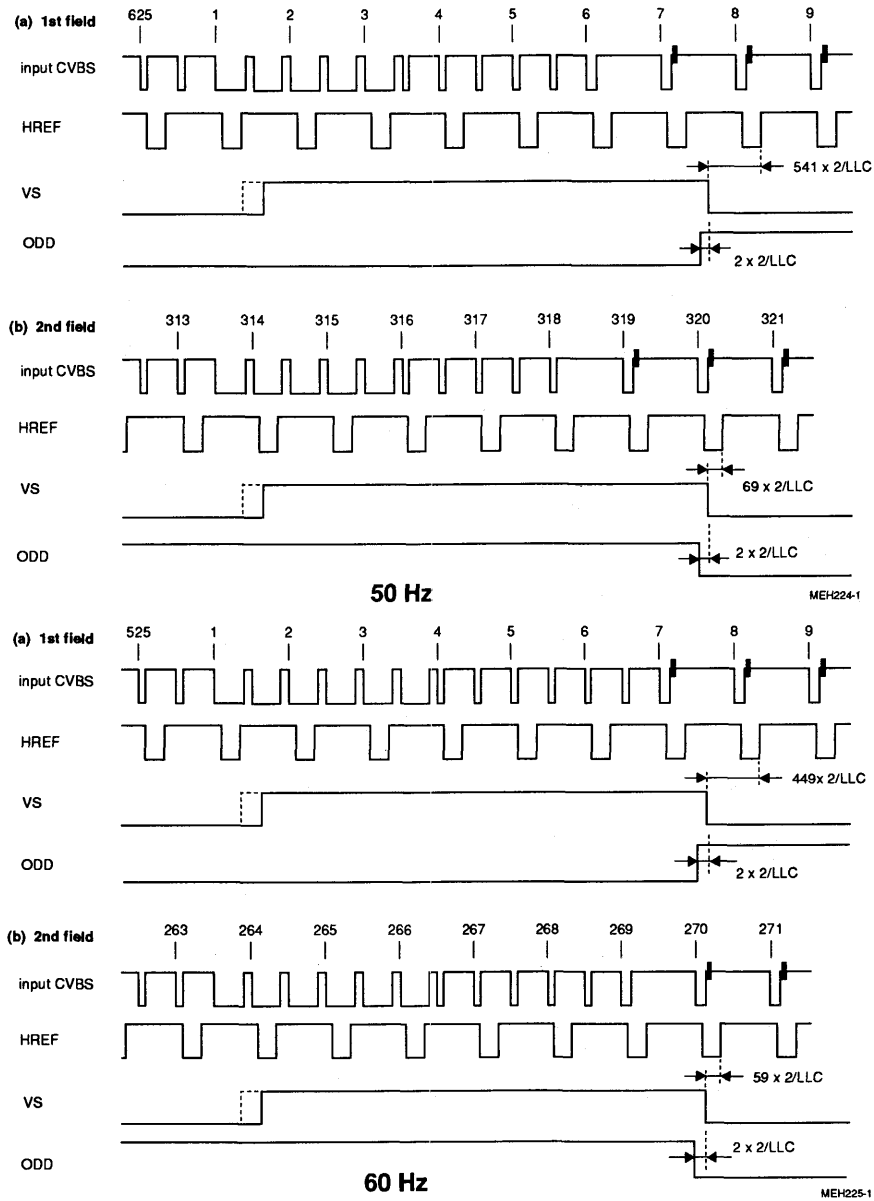
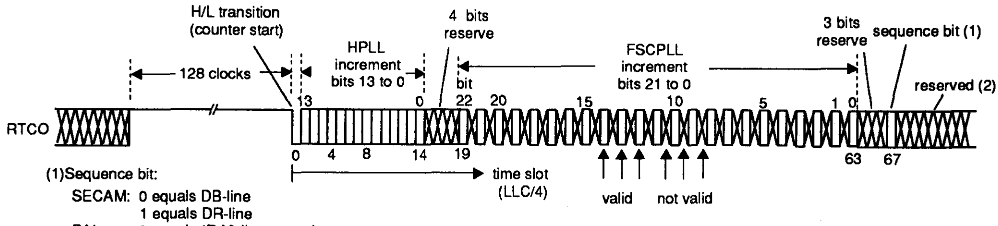


Fig.6 Vertical timing diagram for 50 / 60 Hz.



(1)Sequence bit:
SECAM: 0 equals DB-line
1 equals DR-line
PAL: 0 equals (R-Y) line normal
1 equals (R-Y) line inverted
NTSC: 0 (no change)

(2) Reserve bits: 276 for 50 Hz systems; 188 for 60 Hz systems

Fig.7 RTCO timing.

8. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins 19, 35, 38, 51 and 67 as well as supply pins 5, 18, 28, 37 and 52 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37, 52)	−0.5	7.0	V
$V_{diff\,GND}$	difference voltage $V_{SS\,A} - V_{SS\,(1\,to\,4)}$	-	±100	mV
V_I	voltage on all inputs	−0.5	V_{DD}+0.5	V
V_O	voltage on all outputs ($I_{O\,max}$ = 20 mA)	−0.5	V_{DD}+0.5	V
P_{tot}	total power dissipation	-	2.5	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±2000	V

* Equivalent to discharging a 100 pF capacitor through an 1.5 kΩ series resistor.

9. CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 18, 28, 37, 52)		4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37, 52)	V_{DD} = 5 V; inputs LOW; outputs not connected	-	100	250	mA
I^2C-bus, SDA and SCL (pins 40 and 41)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3	-	V_{DD}+0.5	V
$I_{40,41}$	input current		-	-	±10	μA
I_{ACK}	output current on pin 40	acknowledge	3	-	-	mA
V_{OL}	output voltage at acknowledge	I_{40} = 3 mA	-	-	0.4	V
Data clock and control inputs (pins 3, 4, 6 to 17, 20 to 23, 27, 34, 43 and 64), Fig.10						
V_{IL}	LLC input voltage LOW (pin 27)		−0.5	-	0.6	V
V_{IH}	LLC input voltage HIGH		2.4	-	V_{DD}+0.5	V
V_{IL}	other input voltage LOW		−0.5	-	0.8	V
V_{IH}	other input voltage HIGH		2.0	-	V_{DD}+0.5	V
I_{LI}	input leakage current		-	-	10	μA
C_I	input capacitance	data inputs; note 1	-	-	8	pF
		I/O high-ohmic	-	-	8	pF
		clock inputs	-	-	10	pF
$t_{SU.DAT}$	input data set-up time	Fig.8	11	-	-	ns
$t_{HD.DAT}$	input data hold time		3	-	-	ns
LFCO output (pin 36)						
V_o	output signal (peak-to-peak value)	note 2	1.4	-	2.6	V
V_{36}	output voltage range		1	-	V_{DD}	V
YUV-bus, HREF and VS outputs (pins 30, 42, 45 to 50 and pins 53 to 62)			Figures 11 and 15 to 25			
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitance		15	-	50	pF
Control outputs (pins 24 to 26, 29, 31, 32, 39, 63, 65,66 and 68); Fig.12						
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitance		7.5	-	25	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing of YUV-bus and control outputs		Fig.7				
t_{OH}	output signal hold time	YUV, HREF, VS at C_L = 15 pF	13	-	-	ns
		controls at C_L = 7.5 pF	13	-	-	ns
t_{OS}	output set-up time	YUV, HREF, VS at C_L = 50 pF;	14	-	-	ns
		controls at C_L = 25 pF	14	-	-	ns
t_{SZ}	data output disable transition time	to 3-state condition	16	-	-	ns
t_{ZS}	data output enable transition time	from 3-state condition	14	-	-	ns
t_{RTCO}	RTCO timing			Fig.7		
Chrominance PLL						
f_C	catching range		±400	-	-	Hz
Crystal oscillator		Fig.9				
f_n	nominal frequency	3rd harmonic	-	26.8	-	MHz
$\Delta f / f_n$	permissible deviation f_n		-	-	±50	10^{-6}
	temperature deviation from f_n		-	-	±20	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	-	70	°C
	load capacitance C_L		8	-	-	pF
	series resonance resistance R_S		-	50	80	Ω
	motional capacitance C_1		-	1.1±20%	-	fF
	parallel capacitance C_0		-	3.5±20%	-	pF
	Philips catalogue number		9922 520 30004			
Line locked clock input LLC (pin 27)		Fig.8				
t_{LLC}	cycle time	note 3	31	-	45	ns
t_p	duty factor	t_{LLCH}/t_{LLC}	40	-	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns

Notes to the characteristics

1. Data output signals are Y7 to Y0 and UV7 to UV0. All others are control output signals.
2. Levels are measured with load circuit. YUV-bus, HREF and VS outputs with 1.2 kΩ in parallel to 50 pF at 3 V (TTL load); LFCO output with 10 kΩ in parallel to 15 pF and other outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
3. t_{SU}, t_{HD}, t_{OH} and t_{OD} include t_r and t_f.

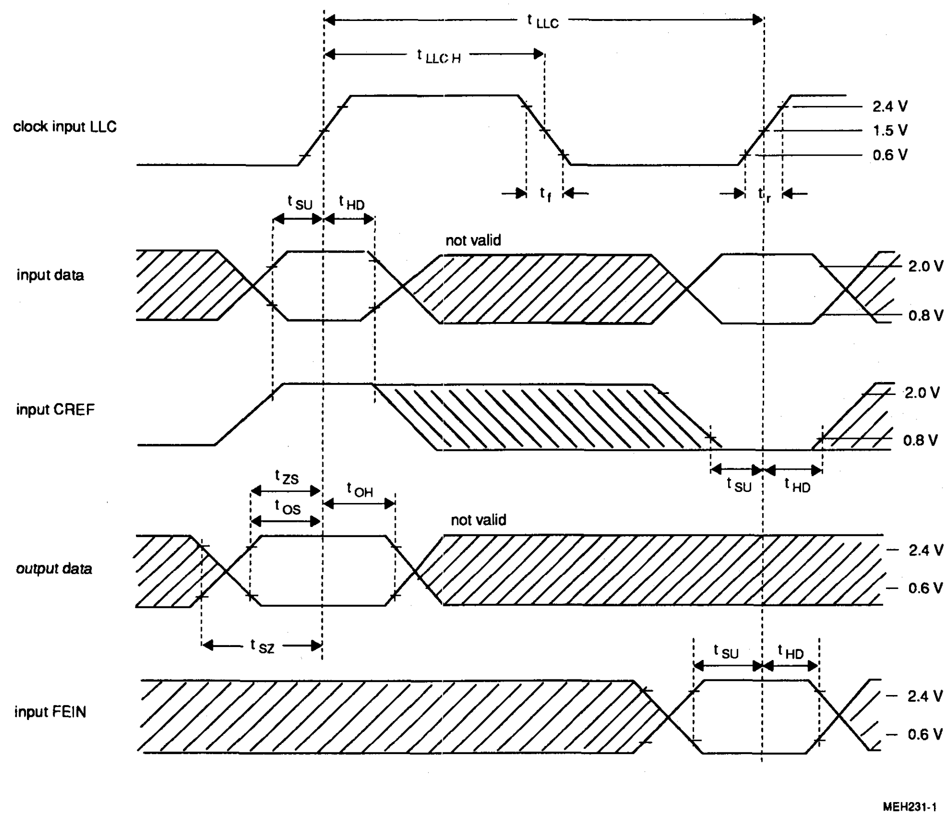


Fig.8 Data input and output timing diagram.

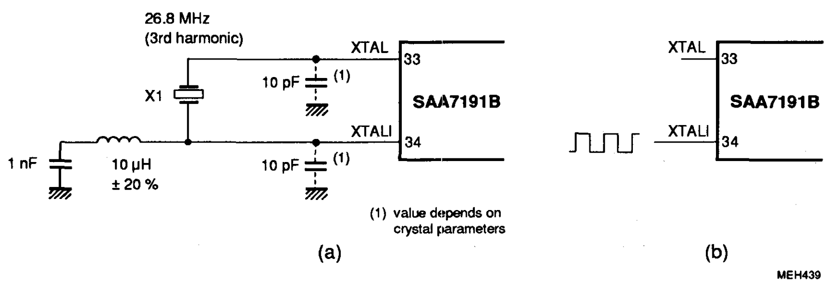
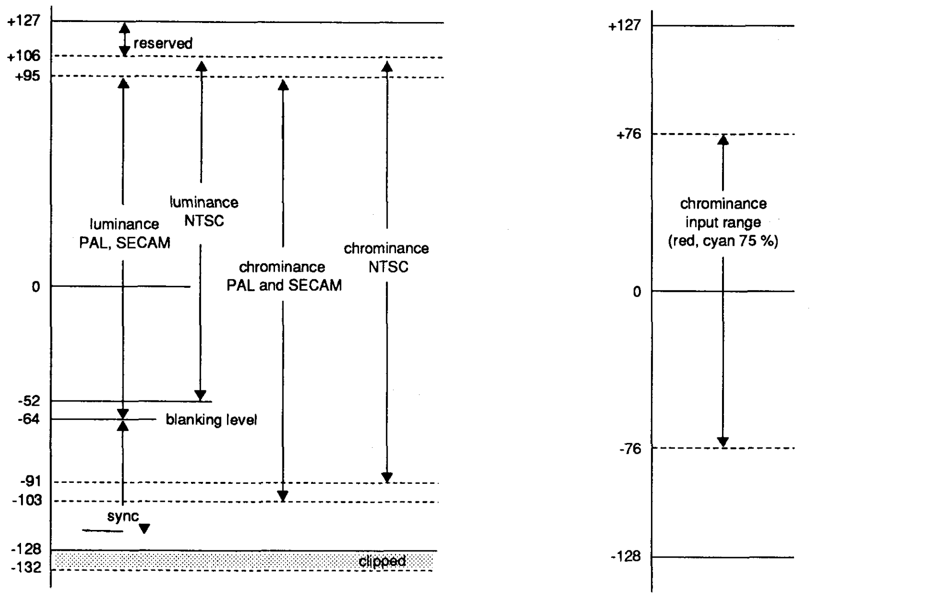
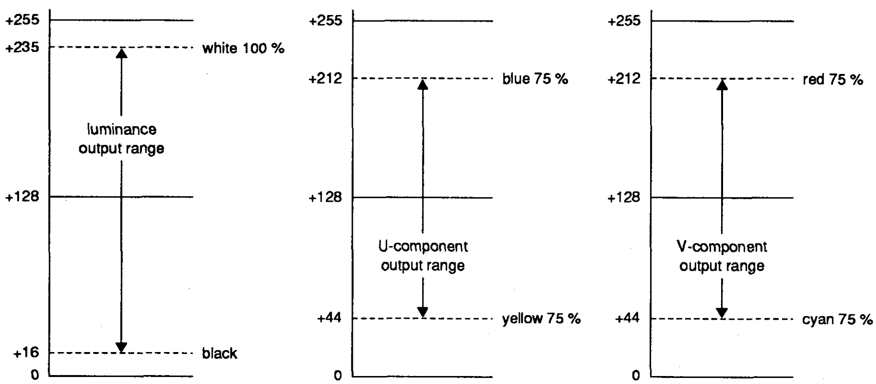


Fig.9 Oscillator application (a) and optional clock from external source (b).



(a) CVBS7 to CVBS0 input signal range.

(b) CHR7 to CHR0 input signal range.



(c) Y output signal range. (d) U output signal range (B-Y). (e) V output signal range (R-Y).

Notes: 1. All levels are related to EBU colour bar.
2. Values in decimal at 100 % luminance and 75 % chrominance amplitude.

MEH254-2

Fig.10 Input and output signal ranges.

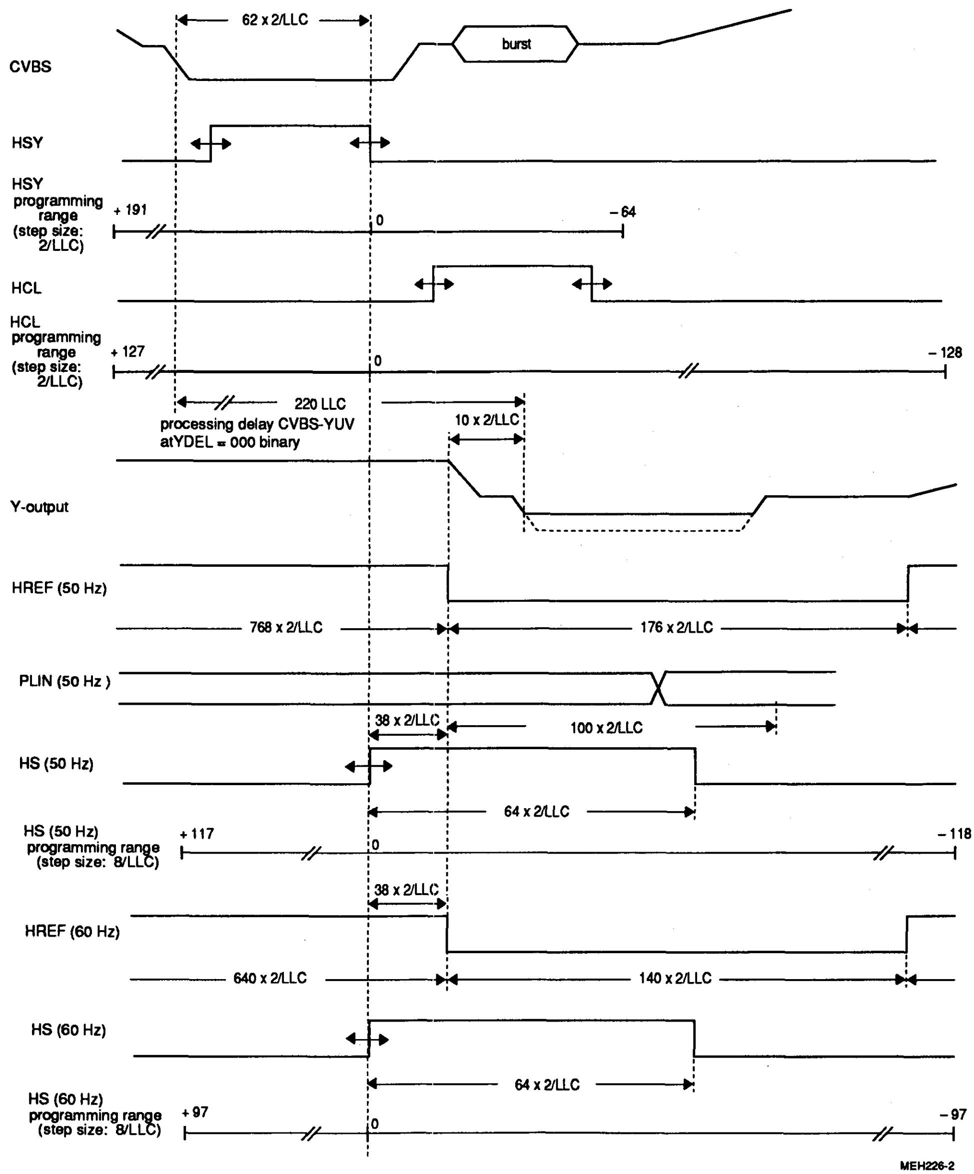


Fig.12 Horizontal sync at HRMV = 0 and HRFS = 0 for 50/60 Hz (signals HSY, HCL, HREF and PLIN).

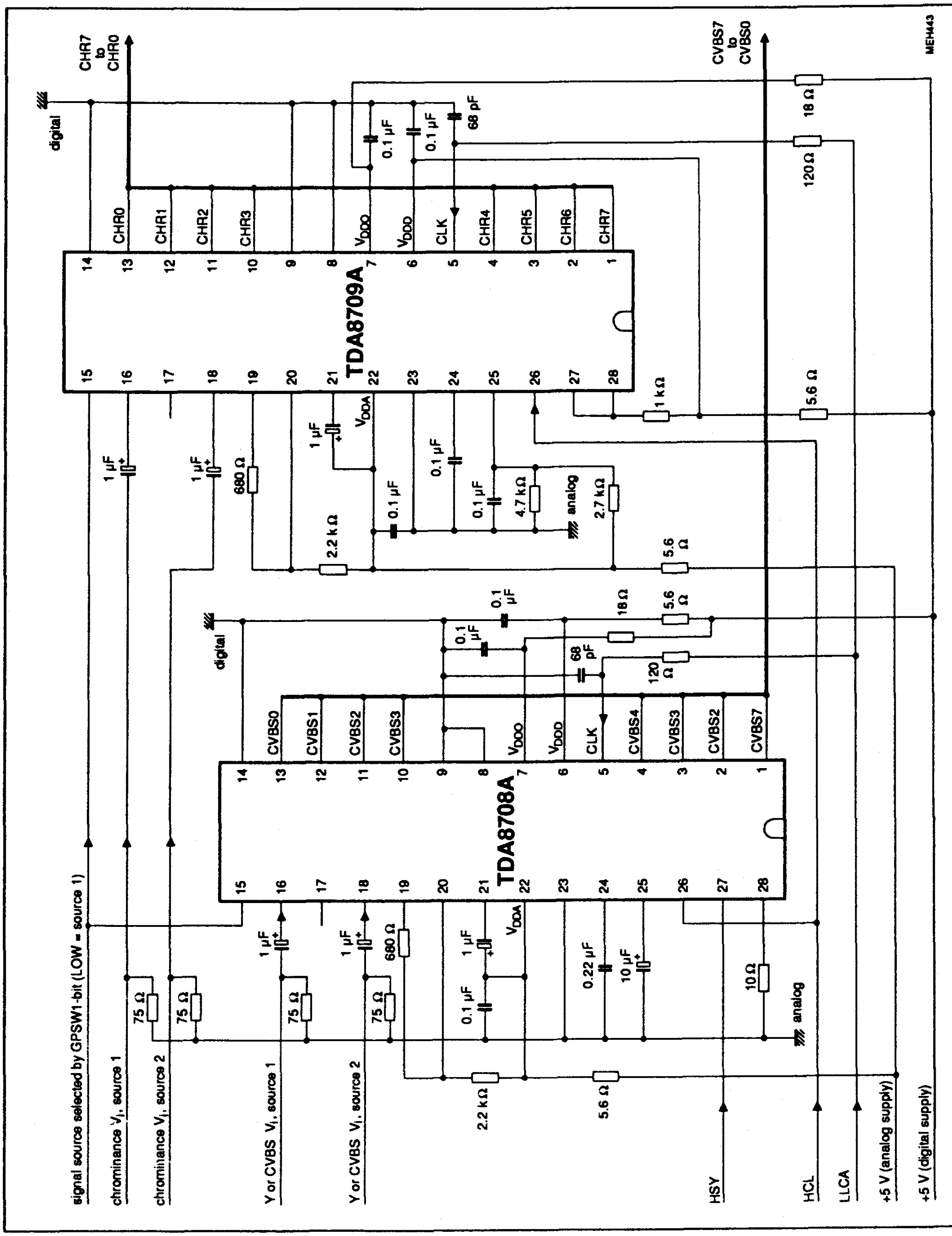


Fig.13 Application circuit for analog-to-digital conversions.

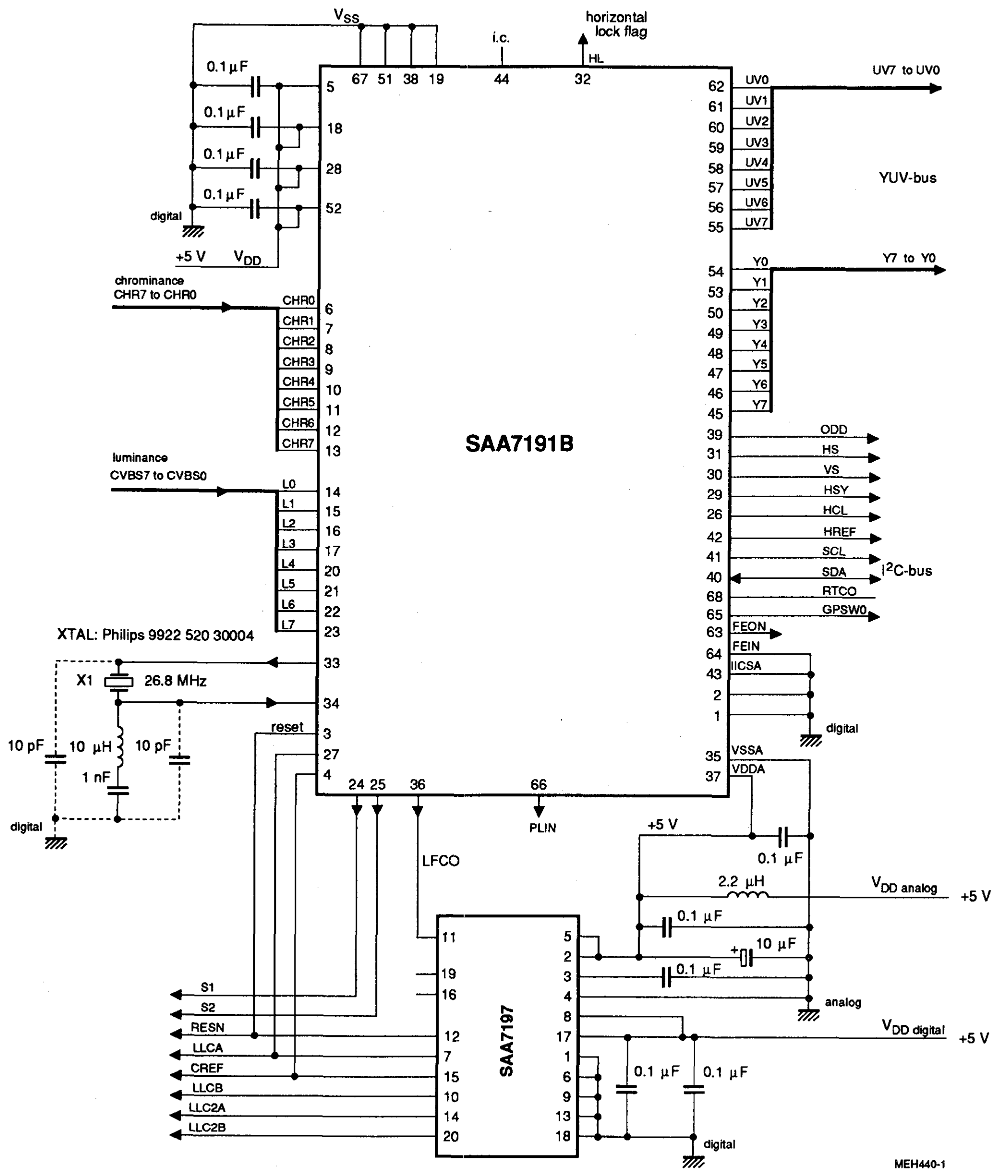


Fig.14 Application circuit for digital multistandard colour decoder.

10. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A	------	DATAn	A	P

S = start condition
SLAVE ADDRESS = **1000 101X** (IICSA = LOW) **or** **1000 111X** (IICSA = HIGH)
A = acknowledge, generated by the slave
SUBADDRESS* = subaddress byte (Table 5)
DATA = data byte (Table 5)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 5 I²C-bus; DATA for status byte (X = 1 in address byte; 8Bh at IICSA = LOW or 8Fh at IICSA = HIGH).

FUNCTION		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
status byte		STTC	HLCK	FIDT	X	X	X	X	CODE

Function of the bits:

STTC Horizontal time constant information for future application with logical combfilter only:
0 = TV time constant (slow);
1 = VCR time constant (fast)

HLCK Horizontal PLL information: 0 = HPLL locked; 1 = HPLL unlocked

FIDT Field information: 0 = 50 Hz system detected; 1 = 60 Hz system detected

CODE Colour information: 0 = no colour detected; 1 = colour detected

Table 6 I²C-bus; subaddress and data bytes for writing (X = 0 in address byte; 8Ah at IICSA = LOW or 8Eh at IICSA = HIGH).

FUNCTION	SUBADDRESS	DATA D7	D6	D5	D4	D3	D2	D1	D0
Increment delay	00	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0
H sync begin, 50 Hz	01	HSYB7	HSYB6	HSYB5	HSYB4	HSYB3	HSYB2	HSYB1	HSYB0
H sync stop, 50 Hz	02	HSYS7	HSYS6	HSYS5	HSYS4	HSYS3	HSYS2	HSYS1	HSYS0
H clamp begin, 50 Hz	03	HCLB7	HCLB6	HCLB5	HCLB4	HCLB3	HCLB2	HCLB1	HCLB0
H clamp stop, 50 Hz	04	HCLS7	HCLS6	HCLS5	HCLS4	HCLS3	HCLS2	HCLS1	HCLS0
H sync after PHI1, 50 Hz	05	HPHI7	HPHI6	HPHI5	HPHI4	HPHI3	HPHI2	HPHI1	HPHI0
Luminance control	06	BYPS	PREF	BPSS1	BPSS0	CORI1	CORI0	APER1	APER0
Hue control	07	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
Colour killer threshold QAM	08	CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0	0	0	0
Colour-killer threshold SECAM	09	CKTS4	CKTS3	CKTS2	CKTS1	CKTS0	0	0	0
PAL switch sensitivity	0A	PLSE7	PLSE6	PLSE5	PLSE4	PLSE3	PLSE2	PLSE1	PLSE0
SECAM switch sensitivity	0B	SESE7	SESE6	SESE5	SESE4	SESE3	SESE2	SESE1	SESE0
Chroma gain control settings	0C	COLO	LFIS1	LFIS0	0	0	0	0	0
Standard/mode control	0D	VTRC	0	0	0	NFEN	HRMV	GPSW0	SECS
I/O and clock control	0E	HPLL	OEDC	OEHS	OEVS	OEDY	CHRS	GPSW2	GPSW1
Control #1	0F	AUFD	FSEL	SXCR	SCEN	OFTS	YDEL2	YDEL1	YDEL0
Control #2	10	0	0	0	0	0	HRFS	VNOI1	VNOI0
Chroma gain reference	11	CHCV7	CHCV6	CHCV5	CHCV4	CHCV3	CHCV2	CHCV1	CHCV0
Not used, is acknowledged	12	0	0	0	0	0	0	0	0
Not used, is acknowledged	13	0	0	0	0	0	0	0	0
H sync begin, 60 Hz	14	HS6B7	HS6B6	HS6B5	HS6B4	HS6B3	HS6B2	HS6B1	HS6B0
H sync stop, 60 Hz	15	HS6S7	HS6S6	HS6S5	HS6S4	HS6S3	HS6S2	HS6S1	HS6S0
H clamp begin, 60 Hz	16	HC6B7	HC6B6	HC6B5	HC6B4	HC6B3	HC6B2	HC6B1	HC6B0
H clamp stop, 60 Hz	17	HC6S7	HC6S6	HC6S5	HC6S4	HC6S3	HC6S2	HC6S1	HC6S0
H sync after PHI1, 60 Hz	18	HP6I7	HP6I6	HP6I5	HP6I4	HP6I3	HP6I2	HP6I1	HP6I0

Note to Table 6

- Default values of register contents to obtain a picture see Table 6.
- All unused control bits must be programmed with "0" (zero) as indicated in Table 5.

Function of the bits of Table 5

IDEL7 to IDEL0 "00"	Increment delay time (dependent on application), step size = 4 / LLC. The delay time is selectable from –4 / LLC (–1 decimal multiplier) to –1024 / LLC (–256 decimal multiplier) equals data FF to 00 (hex). Different processing times in the chrominance channel and the clock generation could result in phase errors in the chrominance processing by transients in clock frequency. An adjustable delay (IDEL) is necessary if the processing time in the clock generation is unknown.
HSYB7 to HSYB0 "01"	Horizontal sync begin for 50 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two's complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.
HSYS7 to HSYS0 "02"	Horizontal sync stop for 50 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two's complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.
HCLB7 to HCLB0 "03"	Horizontal clamp start for 50 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HCLS7 to HCLS0 "04"	Horizontal clamp stop for 50 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HPHI7 to HPHI0 "05"	Horizontal sync after PHI1 for 50 Hz, step size = 8 / LLC. The delay time is selectable from –936 /LLC (+117 decimal multiplier) to +944 /LLC (–118 decimal multiplier) equals data 75 to 8A (hex).
BYPS "06"	input mode select bit: 0 = CVBS mode (chrominance trap active) 1 = S-Video mode (chrominance trap bypassed)
PREF	use of pre-filter: 0 = pre-filter off; 1 = pre-filter on; PREF may be used if chrominance trap is active.
BPSS1 to BPSS0	Aperture bandpass to select different characteristics with maximums (0.2 to 0.3 x LLC / 2): (see table below)
CORI1 to CORI0 "06"	Coring range for high frequency components according to 8-bit luminance, Fig.15. (see table below)

BPSS1	BPSS0	characteristics
0	0	Figures 16 to 25
0	1	Figures 16 to 25
1	0	Figures 16 to 25
1	1	Figures 16 to 25

CORI1	CORI0	coring
0	0	coring off
0	1	±1 LSB
1	0	±2 LSB
1	1	±3 LSB

APER1 to APER0 "06"	Aperture bandpass filter weights high frequency components of luminance signal: APER1 APER0 | factor 0 0 | 0) 0 1 | 0.25) 1 0 | 0.5) Figures 16 to 25 1 1 | 1)
HUE7 to HUE0 "07"	Hue control from +178.6° to –180.0°, equals data bytes 7F to 80 (hex); 0° equals 00.
CKTQ4 to CKTQ0 "08"	Colour-killer threshold QAM from approximately –30 dB to –18 dB, equals data bytes F8 to 07 (hex)
CKTS4 to CKTS0 "09"	Colour-killer threshold SECAM from approximately –30 dB to –18 dB, equals data bytes. F8 to 07 (hex)
PLSE7 to PLSE0 "0A"	PAL switch sensitivity from LOW-to-HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.
SESE7 to SESE0 "0B"	SECAM switch sensitivity from LOW-to-HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.
COLO "0C"	Colour on bit: 0 = automatic colour-killer enabled; 1 = forced colour on.
LFIS1 to LFIS0 "0C"	Chrominance gain control (AGC filter): LFIS1 LFIS0 | loop filter time constant 0 0 = | slow 0 1 = | medium 1 0 = | fast 1 1 = | actual gain, stored for test purposes only
VTRC "0D"	VTR/TV mode bit : 0 = TV mode (slow time constant); 1 = VTR mode (fast time constant)
NFEN	SAA7191B-specified functions enable (RTCO, ODD and GPSW0 outputs) 0 = outputs set to high-impedance (circuit equals SAA7191); 1 = outputs active
HRMV	HREF generation: 0 = like SAA7191; 1 = HREF is 8 x LLC2 clocks earlier
GPSWO	General purpose switch 0: 0 = output pin 65 LOW; 1 = output pin 65 HIGH
SECS	SECAM mode bit : 0 = other standards; 1 = SECAM
HPLL "0E"	Horizontal clock PLL: 0 = PLL closed; 1 = PLL circuit open and horizontal frequency fixed.
OEDC	Colour-difference output enable: 0 = data outputs UV7 to UV0 can be set to high-impedance via FEIN 1 = data outputs UV7 to UV0 active.
OEHS	H-sync output enable (pins 31 and 42): 0 = HS and HREF outputs high-impedance 1 = HS and HREF outputs active.
OEVS	V-sync output enable (pin 30): 0 = VS output high-impedance 1 = VS output active.

OEDY	Luminance output enable: 0 = data outputs Y7 to Y0 can be set to high-impedance via FEIN 1 = data outputs Y7 to Y0 active.
CHRS	S-VHS bit (chrominance from CVBS or from chrominance input): 0 = controlled by BYPS-bit (subaddress 06) 1 = chrominance from chrominance input (CHR7 to CHR0)
GPSW2 to GPSW1 to "0E"	General purpose switches : GPSW2 / GPSW1 / set port output pins 24 (GPSW2) and 25 (GPSW1) 0 0 0 1 1 0 1 1 use is dependent on application
AUFD "0F"	Automatic field detection: 0 = field selection by FSEL-bit; 1 = automatic field detection.
FSEL	Field select (AUFD-bit = 0): 0 = 50 Hz (625 lines); 1 = 60 Hz (525 lines)
SXCR	SECAM cross-colour reduction: 0 = reduction off; 1 = reduction on.
SCEN	Sync and clamping pulse enable: 0 = HCL and HSY outputs HIGH (pins 26 and 29); 1 = HCL and HSY outputs active
OFTS	Select output format: 0 = 4 : 1 : 1 format; 1 = 4 : 2 : 2 format.
YDEL2 to YDEL0	Luminance delay compensation: (see table below)
HRFS "10"	Select HREF position: 0 = normal, HREF is matched to YUV output port; 1 = HREF is matched to CVBS intput port.
VNOI1 to VNOI0	Vertical noise reduction (see table below)

Luminance delay compensation:

YDEL2	YDEL1	YDEL0	figure	
0	0	0	0 x 2 / LLC	
0	0	1	+1 x 2 / LLC	
0	1	0	+2 x 2 / LLC	step size = 2 / LLC =
0	1	1	+3 x 2 / LLC	67.8 ns for 50 Hz
1	0	0	−4 x 2 / LLC	81.5 ns for 60 Hz
1	0	1	−3 x 2 / LLC	
1	1	0	−2 x 2 / LLC	
1	1	1	−1 x 2 / LLC	

Vertical noise reduction

VNOI1	VNOI0	mode
0	0	normal
0	1	searching window
1	0	auto-deflection
1	1	vertical noise reduction bypassed

CHCV7 to CHCV0 UV "11"	Chrominance gain control (nominal values) for QAM-modulated input signals, effects output amplitude (SECAM with fixed gain): D7 D6 D5 D4 D3 D2 D1 D0 | gain 1 1 1 1 1 1 1 1 | maximum gain : : | to) 0 1 0 1 1 0 0 1 | CCIR level for PAL)) default programmed : : | to) values dependend 0 0 1 0 1 1 0 0 | CCIR level for NTSC)) on application : : | to) 0 0 0 0 0 0 0 0 | minimum gain
HS6B7 to HS6B0 "14"	Horizontal sync begin for 60 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two's complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.
HS6S7 to HS6S0 "15"	Horizontal sync stop for 60 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two's complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.
HC6B7 to HC6B0 "16"	Horizontal clamp begin for 60 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HC6S7 to HC6S0 "17"	Horizontal clamp stop for 60 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HP6I7 to HP6I0 "18"	Horizontal sync after PHI1 for 60 Hz, step size = 8 / LLC. The delay time is selectable from –776 /LLC (+97 decimal multiplier) to +776 /LLC (–97 decimal multiplier) equals data 61 to 9F (hex).

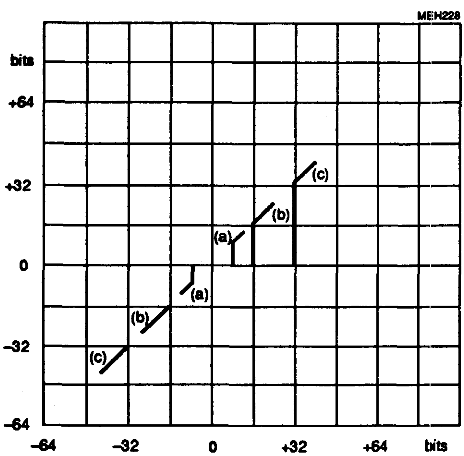


Fig.15 Coring function adjustment by subaddress 06 to affect the bandfilter output signal. The thresholds are related to the 13-bit word width in the luminance processing part and influence the 1LSB to 3LSB (Y0 to Y2) with respect to the 8-bit luminance output

(a) CORI1 = 0; CORI0 = 1

(b) CORI1 = 1; CORI0 = 0

(a) CORI1 = 1; CORI0 = 1

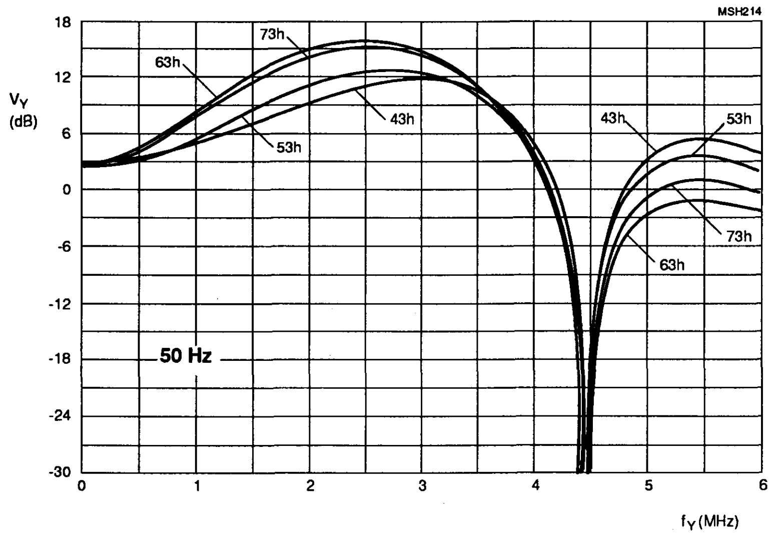


Fig.16 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; maximum aperture bandpass filter characteristic.

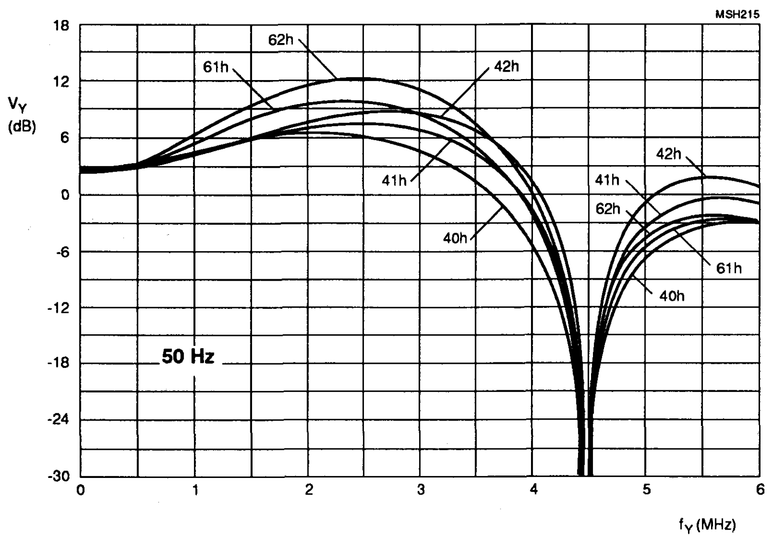


Fig.17 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; other aperture bandpass filter characteristics.

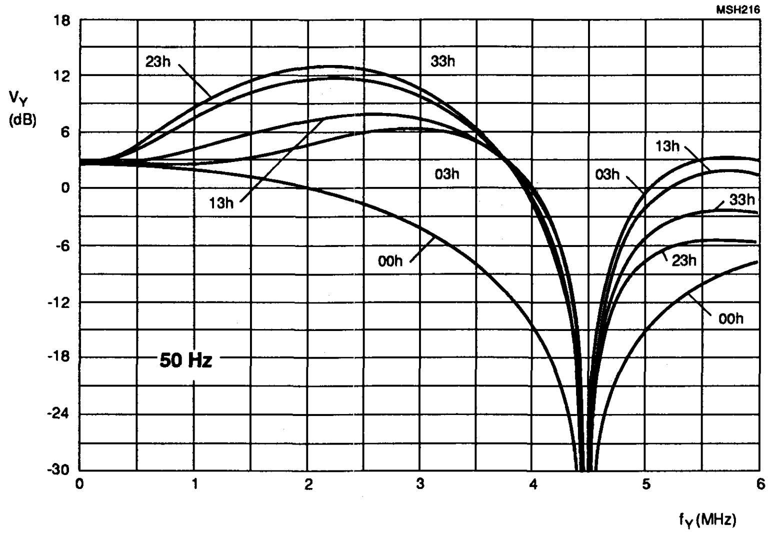


Fig.18 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter off and coring off; maximum aperture bandpass filter characteristic.

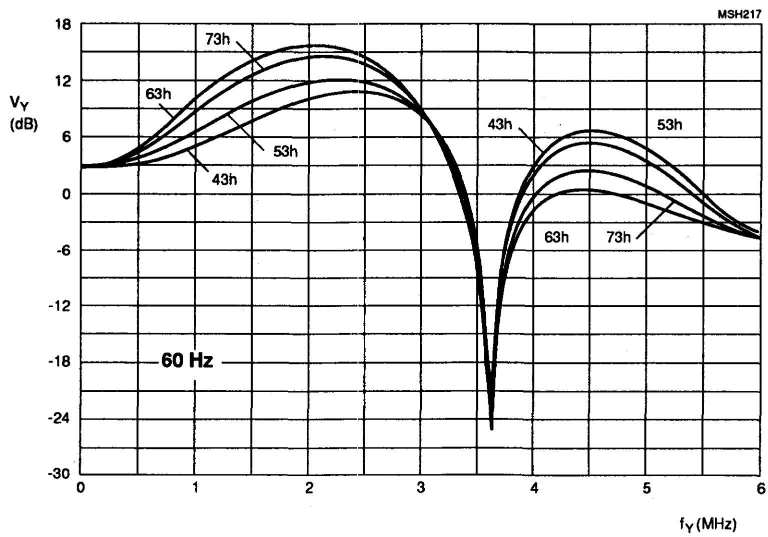


Fig.19 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; maximum aperture bandpass filter characteristic.

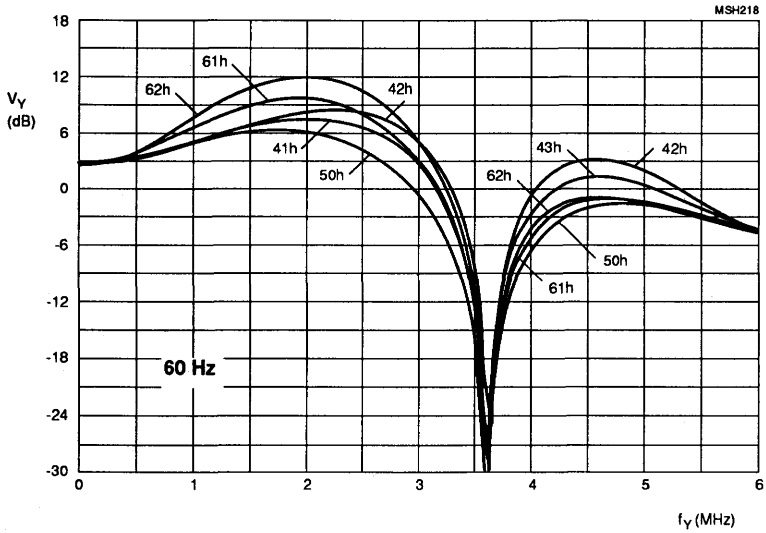


Fig.20 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; other aperture bandpass filter characteristics.

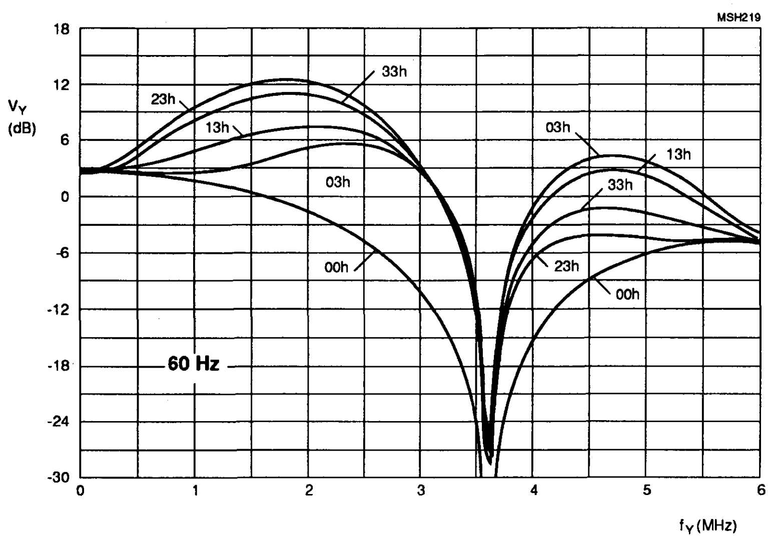


Fig.21 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter off and coring off; maximum and minimum aperture bandpass filter characteristics.

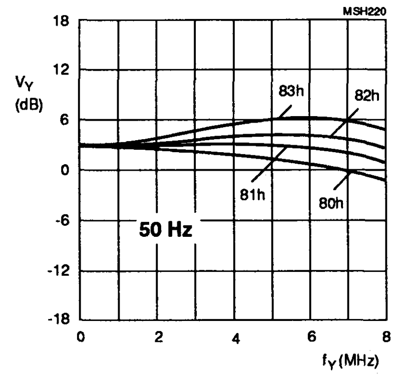


Fig.22 Luminance control in 50 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter off and coring off; different aperture bandpass filter characteristics.

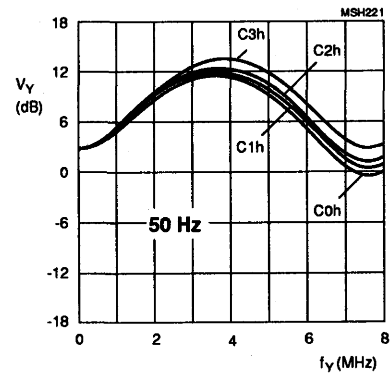


Fig.23 Luminance control in 50 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter on and coring off; different aperture bandpass filter characteristics.

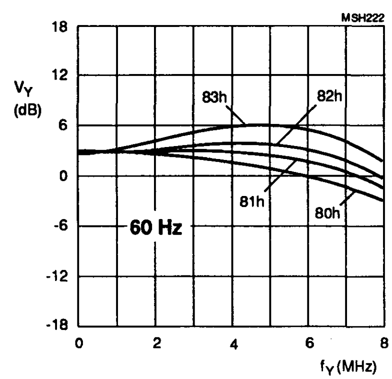


Fig.24 Luminance control in 60 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter off and coring off; different aperture bandpass ffilter characteristics.

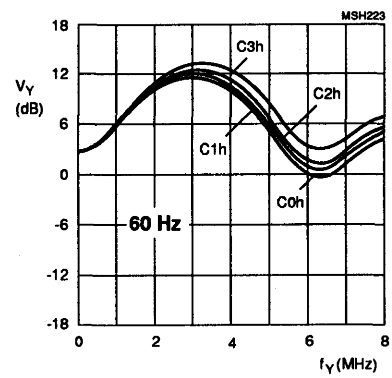


Fig.25 Luminance control in 60 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter on and coring off; different aperture bandpass filter characteristics.

PROGRAMMING EXAMPLE

Coefficients to set operation for application circuits Figures 13 and 14. (All numbers of the Table 6 are hex values). Slave address byte is 8A at pin 43 = 0 V (or 8E at pin 43 = +5 V).

Table 7 Recommended default values

SUBADDRESS	BIT NAME	FUNCTION	VALUE (HEX)
00	IDEL(7-0)	increment delay	50
01	HSYB(7-0)	H sync beginning for 50 Hz	30
02	HSYS(7-0)	H sync stop for 50 Hz	00
03	HCLB(7-0)	H clamping beginning for 50 Hz	E8
04	HCLS(7-0)	H clamping stop for 50 Hz	B6
05	HPHI(7-0)	H sync position for 50 Hz	F4
06	BYPS, PREF, BPSS(1-0) CORI(1-0), APER(1-0)	luminance bandwidth control:	01(1)
07	HUEC(7-0)	hue control (0 degree)	00
08	CKTQ(4-0)	colour-killer threshold QUAM	F8
09	CKTS(4-0)	colour-killer threshold SECAM	F8
0A	PLSE(7-0)	PAL switch sensitivity	90
0B	SESE(7-0)	SECAM switch sensitivity	90
0C	COLO, LFIS(1-0)	chroma gain control settings	00
0D	VTRC, NFEN,HRMV, GPSW0 and SECS	standard/mode control	00(2)(4), 01(3)(4)
0E	HPLL, OEDC, OEHS, OEVS OEDY, CHRS, GPSW(2-1)	I/O and clock control	79, 7E(5)
0F	AUFD, FSEL, SXCR, SCEN, OFTS, YDEL(2-0)	miscellaneous control #1	91(6), 99(7)
10	HRFS, VNOI(1-0)	miscellaneous control #2	00
11	CHCV(7-0)	chrominance gain nominal value	2C(8), 59(9)
12	-	set to zero	00
13	-	set to zero	00
14	HS6B(7-0)	H sync beginning for 60 Hz	34
15	HS6S(7-0)	H sync stop for 60 Hz	0A
16	HC6B(7-0)	H clamping beginning for 60 Hz	F4
17	HC6S(7-0)	H clamping stop for 60 Hz	CE
18	HP6I(7-0)	H sync position for 60 Hz	F4

Notes to Table 7

(1) dependent on application (Figures 16 to 25)
(2) for QUAM standards
(3) for SECAM
(4) HPLL is in TV mode; value for VCR mode is 80 (81 for SECAM VCR mode)
(5) for Y/C mode
(6) 4:1:1 format
(7) 4:2:2 format
(8) nominal value for UV CCIR level with NTSC source
(9) nominal value for UV CCIR level with PAL source

12. UPDATE HISTORY

DATE OF ISSUE	UPDATES COMPARED TO PREVIOUS VERSION PAGE	CHANGES
April 1993	9	signal HS, pin 31 added
	11	Table 4 with output conditions added
	12	Fig.4 with fast enable FEIN added
	14	Fig.6; ODD signals added in vertical timing
	15	LIMITING VALUES: V_{ESD} = ±2000 V must be maximum value
	16, 17	CHARACTERISTICS, notes included: some positions have been changed
	18	Fig.8: CREF changed and FEIN added
	20	Fig.12: some new informations (Fig. 11 and 12 tied together)
	21	Fig.13: Capacitors on pins 24 and 25 of TDA8708A changed.
	22	Fig.14: the 10 kΩ resistor for reset pin 3 is not longer necessary
	25	delay time polarities changed for HSYB, HSYS, HCLB, HCLS and HPHI; data now is 75h and 8Ah.
	26	changes for bits CKTQ, CKTS, COLO, LFIS, VTRC and OEDC
	27	changes for bits OEDY, GPSW, AUFD, SCEN and HRFS
	28	delay time polarities changed for HS6B, HS6S, HC6B, HC6S and HP6I; data now is 61h and 9Fh.
	33	Table 7 and Notes changed.

Digital colour space converter

SAA7192A

FEATURES

- Input formatter with:
  - multiplexer
  - Y-dalay line
  - Cr and Cb interpolating filters
- Conversion matrix (acc. to CCIR 601)
- Video look-up tables (provide gamma correction)
- Pipeline delay line (horizontal reference signal)
- I²C-bus interface

GENERAL DESCRIPTION

The Digital Colour Space Converter (DCSC) is a digital matrix which is used to transform 16/24-bit digital input signals, i.e. Y (luminance), Cr (colour, R-Y) and Cb (colour, B-Y), into an RGB 24-bit format in accordance with the CCIR-601 recommendations.

Accepting inputs from the different formats of the DMSD2 decoder family, the device has a constant propagation delay and a maximum data rate of 16 MHz. A matched pipeline delay line is available to permit the HREF signal to be synchronized with the video data at the output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	Supply voltage	−0.5	7	V
VI	input voltage	−0.5	7	V
VO	output voltage	−0.5	7	V
P_{tot}	total power dissipation	-	1.5	W
T_{stg}	storage temperature range	−65	+150	C
T_{amb}	operating ambient temperature	0	+70	C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7192	68	PLCC	plastic	SOT18-8AA, AGA, CGS

BLOCK DIAGRAM

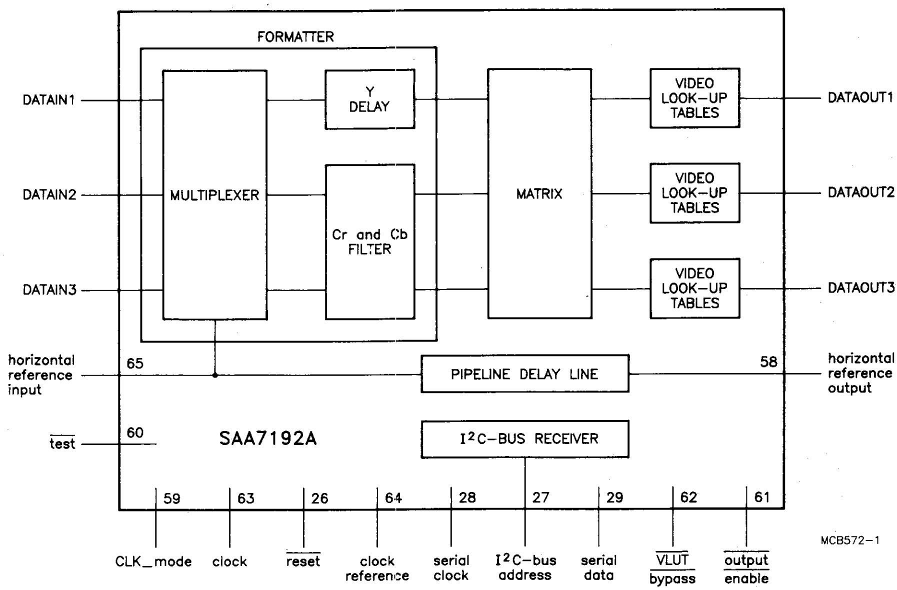


Fig.1 Block diagram.

PIN CONFIGURATION

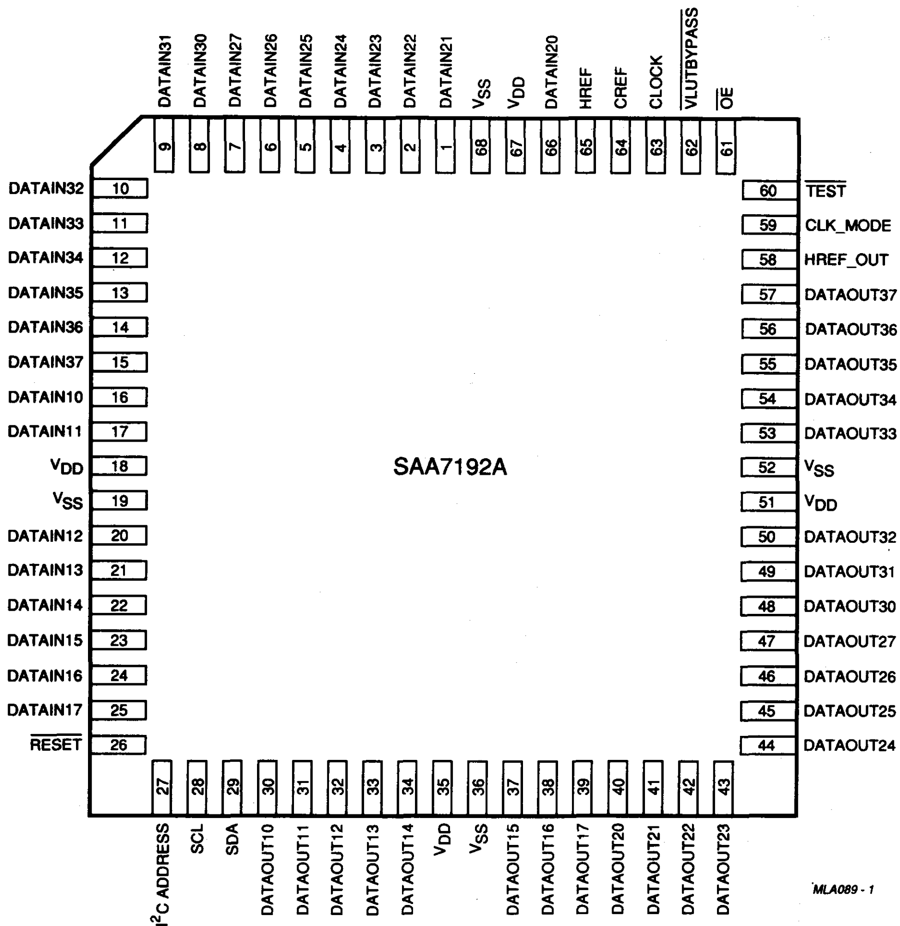


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
DATAIN (10-17)	16-17 and 20-25	luminance signal Y (0-7)
DATAIN (20-27)	1-7 and 66	colour difference signal Cr (0-7)
DATAIN (30-37)	8-15	colour difference signal Cb (0-7) or multiplexed Cb and Cr
DATAOUT (10-17)	30-34 and 37-39	RED (0-7)
DATAOUT (20-27)	40-47	GREEN (0-7)
DATAOUT (30-37)	48-50 and 53-57	BLUE (0-7)
$\overline{\text{RESET}}$	26	initially resets the functions
HREF_OUT	58	delayed horizontal reference signal
CLK_MODE	59	16 MHz or DMSD clock mode selection
$\overline{\text{TEST}}$	60	test mode, usually not connected
$\overline{\text{OE}}$	61	output enable (fast switch)
$\overline{\text{VLUTBYPASS}}$	62	fast switch to operate the VLUTs in bypass
CLOCK	63	system clock
CREF	64	clock reference signal (DMSD mode)
HREF	65	horizontal reference signal
V_{DD}	18, 67	positive supply, voltage core (+ 5 V)
	35, 51	positive supply voltage, output stages (+ 5 V)
V_{SS}	19, 68	negative supply, voltage core (ground)
	36, 52	negative supply, output stages
I^2C-bus ADDRESS	27	I^2C-bus SLAVE ADDRESS selection
SCL	28	I^2C-bus SERIAL CLOCK input
SDA	29	I^2C-bus SERIAL DATA input

Note

All DATAIN and DATAOUT busses count from 0 (LSB) to 7 (MSB).

Functional modes

Table 1 Functional Modes

MODE	FUNCTION
1	4:1:1 filter, no matrix, no VLUT; DATAOUT = upsampled DATAIN
2	4:1:1 filter, matrix, no VLUT; DATAOUT = RGB
3	4:1:1 filter, no matrix, VLUT; DATAOUT = upsampled DATAIN multiplied by the factor loaded into the VLUT
4	4:1:1 filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT
5	4:2:2 filter, no matrix, no VLUT; DATAOUT = upsampled DATAIN
6	4:2:2 filter, matrix, no VLUT; DATAOUT = RGB
7	4:2:2 filter, no matrix, VLUT; DATAOUT = upsampled DATAIN multiplied by the factor loaded into the VLUT
8	4:2:2 filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT
9	no filter, no matrix, no VLUT; DATAOUT = DATAIN "Process Bypass"
10	no filter, matrix, no VLUT; DATAOUT = RGB
11	no filter, no matrix, VLUT; DATAOUT = DATAIN multiplied by the factor loaded into the VLUT.
12	no filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT

Note

Figures 3 to 10 illustrate the various functional modes.

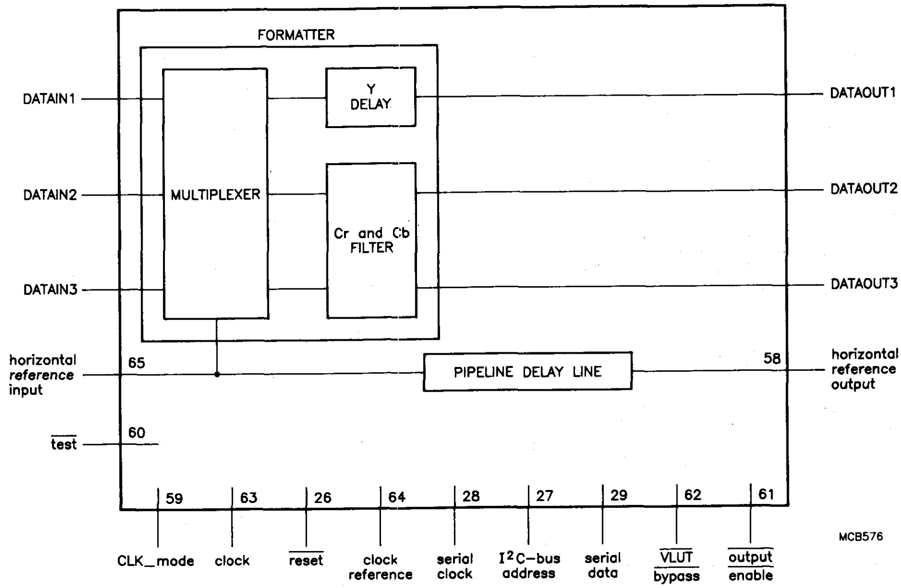


Fig.3 Functional mode 1 and 5.

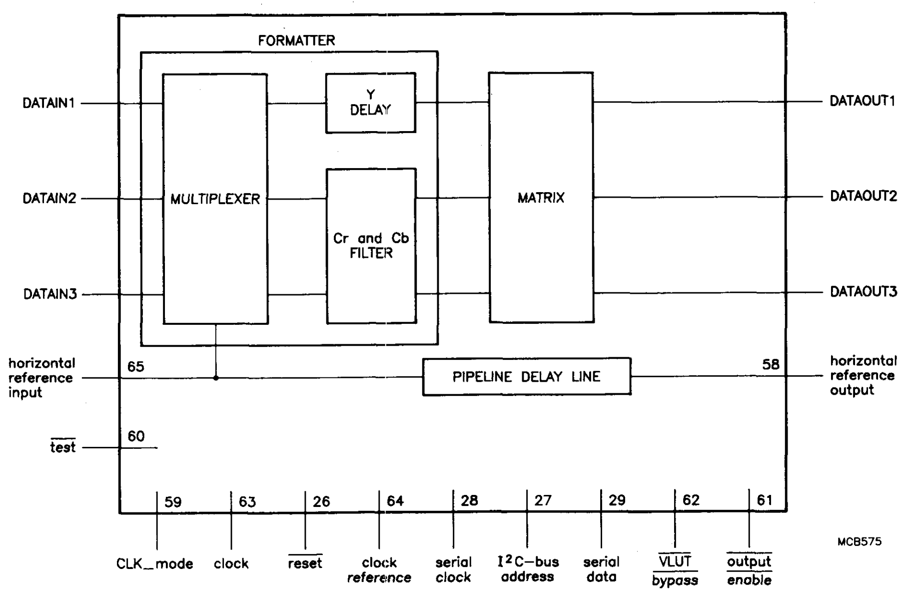


Fig.4 Functional mode 2 and 6.

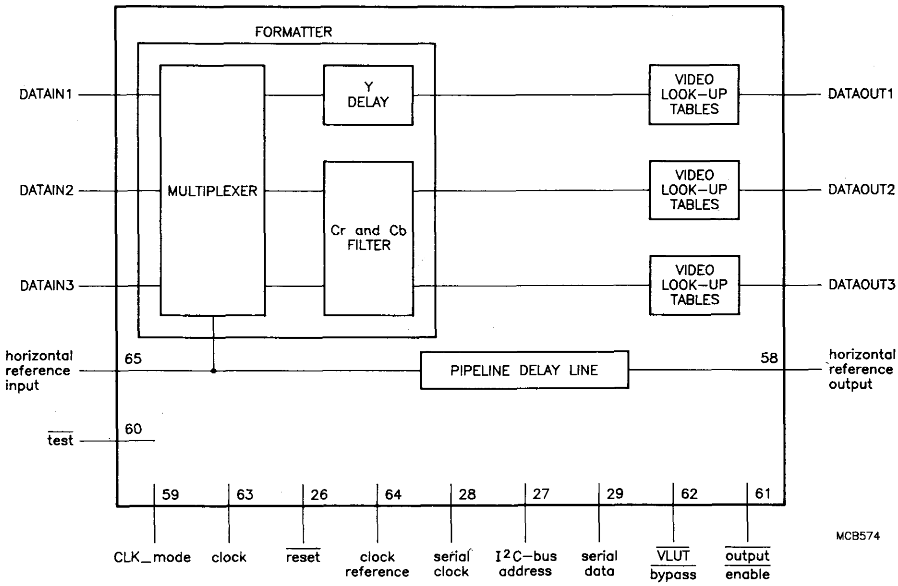


Fig.5 Functional mode 3 and 7.

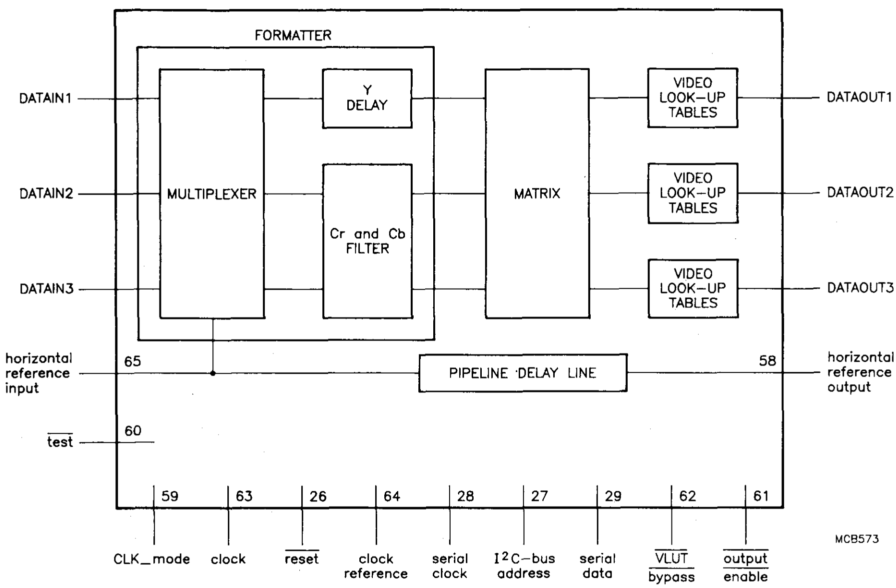


Fig.6 Functional mode 4 and 8.

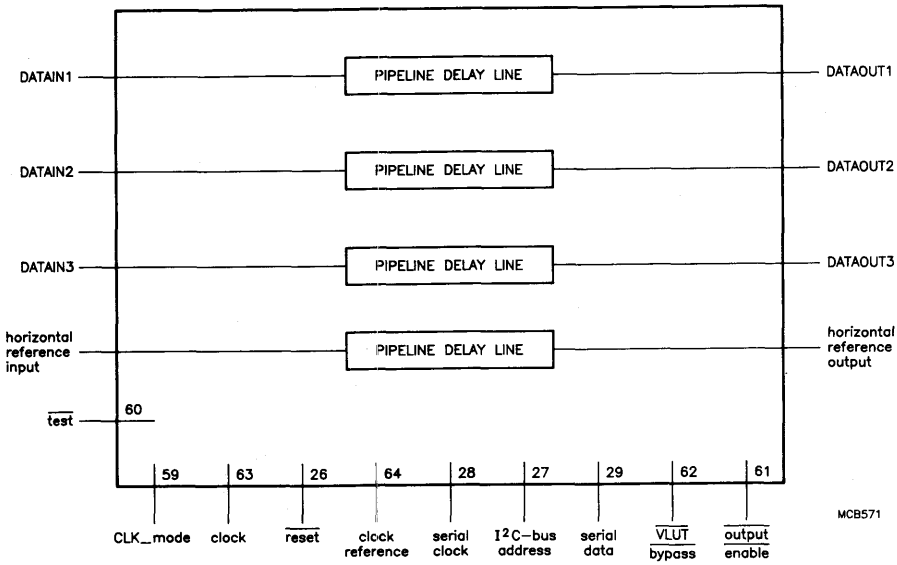


Fig.7 Functional mode 9.

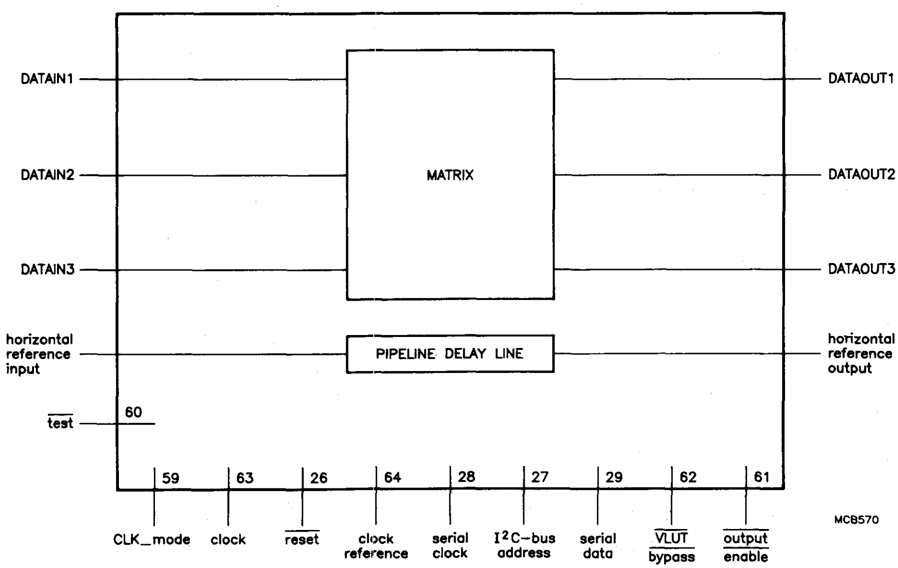


Fig.8 Functional mode 10.

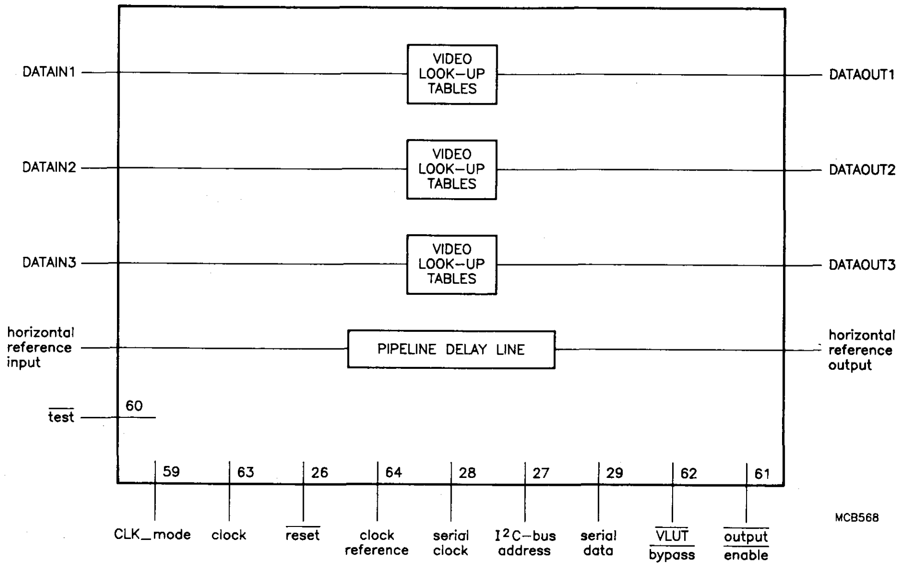


Fig.9 Functional mode 11.

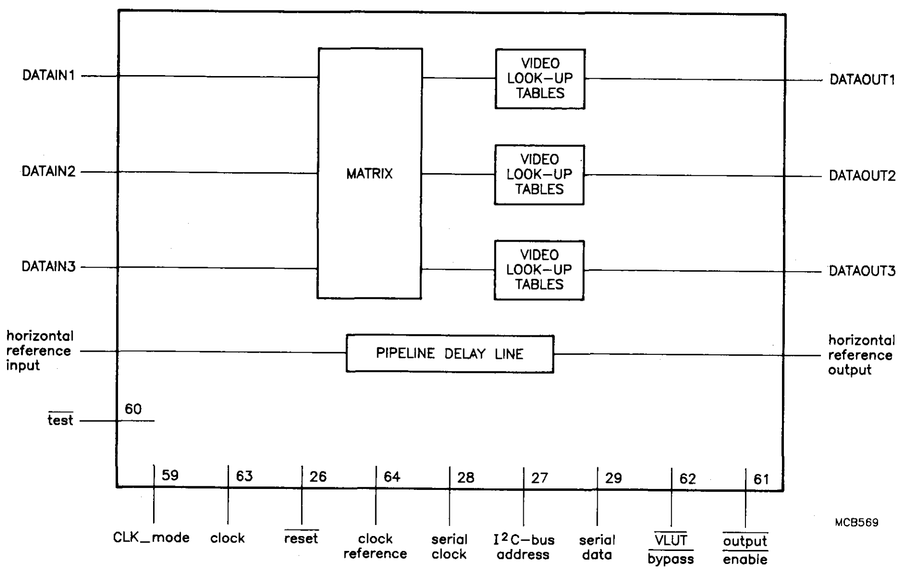


Fig.10 Functional mode 12.

Control facilities

After power-up all device internal control signals are at undefined values. The I^{2}C-bus receiver must, therefore, be reset by using the external RESET signal.

Table 2 I^{2}C-bus control signals (subadd 00H) after an external RESET is received

SYMBOL	BIT	STATUS
IICOE	D5	= 1 ; $\overline{\text{OE}}$ pin 61 enabled
FMTCNTRL	D0-D2	= 4 ; format 4:4:4
$\overline{\text{MATBYPASS}}$	D3	= 0 ; matrix by-passed
$\overline{\text{INRESET}}$	D4	= 0 ; input data set to fixed values

Table 3 Input formats and functional modes

FMTCNTRL	$\overline{\text{MATBYPASS}}$	$\overline{\text{VLUTBYPASS}}$	FUNCTIONS
000	0	0	mode 1, input format 1 (DMSD2 format)
000	1	0	mode 2, input format 1 (DMSD2 format)
001	0	0	mode 1, input format 2
001	1	0	mode 2, input format 2
010	0	0	mode 5, input format 3 (DMSD2 format)
010	1	0	mode 6, input format 3 (DMSD2 format)
011	0	0	mode 5, input format 4 (parallel IN)
011	1	0	mode 6, input format 4 (parallel IN)
100	0	0	mode 9, input format 5 (parallel IN)
100	1	0	mode 10, input format 5 (parallel IN)
x	x	1	each of the above described modes will be multiplied by the factor loaded into the VLUT.

Note

The modes are given in Table 1.

The other control signals are:

$\overline{\text{INRESET}}$	=	logic 1	:	input latches at the formatter are always transparent
	=	logic 0	:	at the end of each active video line the input latches have to be set to fixed values (Y to 16; Cr and Cb to 128; if HREF = 0)
CLK_MODE	=	logic 1	:	DMSD mode (LL27 clock of DMSD feeds the DCSC)
	=	logic 0	:	DCSC is fed by a maximum 16 MHz clock without CREF signal.

Table 4 Output enable control

IICOE	$\overline{\text{OE}}$	CONTROL LINE TO DRIVER STAGES
0	X	1 = DATAOUT in high impedance mode
1	1	1 = DATAOUT in high impedance mode
1	0	0 = DATAOUT working

Notes

IICOE : D5; output enable control of I_2C-bus (enables $\overline{\text{OE}}$)

$\overline{\text{OE}}$: pin 61 ; output enable (fast switch)

SYSTEM I/O INTERFACES

Input signals

Table 5 Format 0 (4:1:1, semi-parallel, DMSD2 decoder family format)

DATAIN1 - Y	luminance signal, 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black, quantization level 16 100 IRE; white, quantization level 235
DATAIN3 - U, V	multiplexed colour difference signals 4-bit; corresponds to UV7 to UV4 of DMSD2
Sampling frequency	1/4 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 6 Timing of Format 0; pin (DATAIN) and bit (U,V) numbers are indicated except clock

Y; 7 to 0	Y	Y	Y	Y	Y	Y	Y
DATAIN 37	U7	U5	U3	U1	U7	U5	U3
DATAIN 36	U6	U4	U2	U0	U6	U4	U2
DATAIN 35	V7	V5	V3	V1	V7	V5	V3
DATAIN 34	V6	V4	V2	V0	V6	V4	V2
Clock A	1	2	3	4	5	6	7

Note

Clock_A is the internal sampling clock of the system. The clock rate of the DMSD and the DCSC is twice that of Clock_A in this mode.

Table 7 Format 1 (4:1:1, semi-parallel, customized format)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cr, Cb	multiplexed colour difference signals, 8-bit
Sampling frequency	1/4 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 8 Timing of Format 1; the indices show the clock (sample) number

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cr, Cb	Cb0		Cr0		Cb4		Cr4
Clock A	0	1	2	3	4	5	6

Note

Clock_A is the internal sampling clock of the system. The external CLOCK may differ from the CLK_MODE.

Table 9 Format 2 (4:2:2, semi-parallel, DMSD2 format)

DATAIN1 Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cr, Cb	multiplexed colour difference signals; corresponds to UV7 to UV0 of DMSD2
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 10 Timing of Format 2

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cr, Cb	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4	Cb6
Clock A	0	1	2	3	4	5	6

Note

Clock_A is the internal sampling clock of the system. The clock of the DMSD (also the CLOCK of the DCSC) is twice that of Clock_A in this mode.

Table 11 Format 3 (4:2:2, Y-Cr-Cb, parallel)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cb	colour difference signal B-Y, 8-bit
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2 - Cr	colour difference signal R-Y, 8-bit
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128

Table 12 Timing of Format 3

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cb	Cb0		Cb2		Cb4		Cb6
Cr	Cr0		Cr2		Cr4		Cr6
Clock A	0	1	2	3	4	5	6

Note

Clock_A is the internal sampling clock of the system. The external CLOCK may differ from the CLK_MODE.

Table 13 Format 4 (4:4:4, Y-Cr-Cb, parallel)

DATAIN2 - Cr	colour difference signal R-Y, 8-bit
Sampling frequency	as the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless, binary 128
DATAIN3 - Cb	colour difference signal B-Y, 8-bit
Sampling frequency	as the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235

VIDEO DATA (DATAIN)

Table 14 Timing of Format 4

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cb	Cb0	Cb1	Cb2	Cb3	Cb4	Cb5	Cb6
Cr	Cr0	Cr1	Cr2	Cr3	Cr4	Cr5	Cr6
Clock A	0	1	2	3	4	5	6

Note

Clock_A is the internal sampling clock of the system. The external CLOCK may differ from CLK_MODE.

CONTROL DATA

Clock

The CLK-Mode signal is used to select the frequency of the system clock (denoted as CLOCK at the DCSC input) and may be chosen from two different Clock Modes.

16 MHz-Mode:

DCSC is used in any environment except that of the DMSD2 decoder family. The clock reference signal (CREF) is internally set HIGH in value.

The maximum CLOCK frequency is 16 MHz.

DMSD-Mode:

DCSC is used in a DMSD environment.

The CLOCK signal (LL27) and the CREF signal are fed by the clock generator circuit (SAA7157/SAA7197) and the line locked clock LL27 (denoted as CLOCK at the DCSC input) is twice the data rate of that specified for the DMSD2 family of decoders. The data rate is denoted as CLOCK_A in Tables 6, 8, 10, 12 and 14.

The data rate on the input (DATAIN) is as follows:

12.2727 MHz; 60 Hz signals (from SAA7191)
13.5 MHz; CCIR signals (from SAA7151)
14.75 MHz; 50 Hz signals (from SAA7191)
16.0 MHz; maximum frequency

TIMING REFERENCE

The timing reference signal from the SAA7151/7191 is used to synchronize the multiplexer and refers to the LL27 clock. Each alternative positive slope, marked by a CREF signal, is used to obtain data.

The horizontal reference signal, HREF, indicates the active part of a line and also synchronizes the multiplexer.

CREF — The clock reference signal is a clock qualifier signal distributed by the clock generator of the DMSD system. The frequency is identical to the sample rates denoted in the input and the output formats (see Video data and Operating conditions).

HREF — Horizontal reference signal is the line reference signal of the YUV-bus. A positive slope marks the beginning of the active part of a line. The length of the active part corresponds to the number of samples (see Operating conditions).

Table 15 Real-time control signals

$\overline{OE}$	pin 61	= 1 :	switches the output to high-z mode
		= 0 :	output enable, output stage in use
$\overline{VLUTBYPASS}$	pin 62	= 1 :	VLUT's in use
		= 0 :	VLUT's bypassed
$\overline{RESET}$	pin 26	= 1 :	device in use
		= 0 :	general reset
CLK_MODE	pin 59	= 1 :	DMSD mode (LL27 clock of DMSD feeds the DCSC)
		= 0 :	DCSC is fed by a clock signal with a maximum data rate of 16 MHz (without CREF signal).

Table 16 I^{2}C-bus controls (sub-add. VLUTDATA)

VLUTDATA FED TO	SUB-ADD
RAM 1 (RED)	01H
RAM 2 (GREEN)	02H
RAM 3 (BLUE)	03H
RAM 1, 2, 3	04H

Note

See also example of VLUT programming Fig. 23.

Table 17 I²C-bus controls (sub-add. 00H)

FMTCNTRL	D0-D2	= 000 :	4:1:1 format, DMSD2 format
		= 001 :	4:1:1 format, customized format
		= 010 :	4:2:2 format, from DMSD2
		= 011 :	4:2:2 format, parallel
		= 100 :	4:4:4 format, parallel
		= 101 :	not used
		= 110 :	not used
		= 111 :	not used
$\overline{\text{MATBYPASS}}$	D3	= 1 :	matrix in use
		= 0 :	matrix bypassed
$\overline{\text{INRESET}}$	D4	= 1 :	input latches at the formatter are always transparent
		= 0 :	at the end of each active video line the input latches have to be set to fixed values (Y to 16; Cr, Cb to 128; if HREF = 0)
IICOE		D5 = 1 :	$\overline{\text{OE}}$ enabled
		= 0 :	switches the output to high impedance mode

OUTPUT SIGNALS

Video data

Table 19 Timing of DATAOUT (R-G-B if matrix in use)

Timing : the indices show the clock sample number							
DATAOUT1 :	R0	R1	R2	R3	R4	R5	R6
DATAOUT2 :	G0	G1	G2	G3	G4	G5	G6
DATAOUT3 :	B0	B1	B2	B3	B4	B5	B6
Clock_A :	0	1	2	3	4	5	6

Notes

Clock_A is the internal sampling clock of the system. The system clock may differ from CLK-MODE.

$\overline{\text{OE}}$ (output enable, fast switch, active LOW) and IICOE (I²C-bus output enable, active HIGH) will switch the DATAOUT lines in high-z or normal mode.

See also Fig. 14.

Auxiliary data

Pipelined external reference signal HREF_OUT (delayed HREF).

The delay line (wordlength 1-bit) has the same duration as the signal processing of the video data lines.

OPERATING CONDITIONS

Electrical Conditions

START-UP CONDITION

No particular function except the external power-on-reset e.g. for I²C-bus interface (RESET) is intended.

OPERATING TIME

As this device will be used in computers, it has been designed to operate continuously.

HANDLING

Inputs and outputs are protected against electrostatic discharge during normal handling. It is desirable, however, to observe normal handling precautions appropriate to MOS devices.

TEMPERATURE RANGE

Refer to the characteristics.

BACKUP

No internal backup capability (standby) is provided.

POWER DOWN MODE

No internal power-down capability is provided.

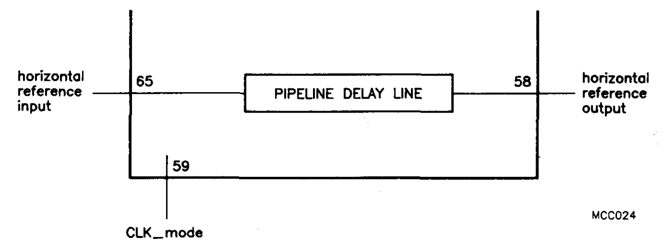


Fig.11 Delayed HREF.

LIMITING VALUES

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.5	7	V
VI	input voltage	–0.5	7	V
VO	output voltage	–0.5	7	V
P_{tot}	total power dissipation	-	1.5	W
T_{stg}	storage temperature range	–65	+150	C
T_{amb}	operating ambient temperature	0	+70	C

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{DD}	supply voltage		4.5	5.5	V
I_{DD}	supply current	note 1	-	150	mA
Inputs					
V_{IL}	input voltage LOW				
	SDA, SCL		–0.5	1.5	V
	any other		–0.5	0.8	V
V_{IH}	input voltage HIGH				
	SDA, SCL		3	V_{DD} +0.5	V
	any other		2	V_{DD} +0.5	V
I_L	input leakage current	note 2	-	10	µA
C_I	input capacitance		-	10	pF
Outputs					
	output voltage				
V_{OH}	HIGH (any)		2.4	V_{DD}	V
V_{OL}	LOW (SDA)		0	0.4	V
	LOW (any other)		0	0.4	V
	output current				
I_{OH}	HIGH (any)		-	4	mA
I_{OL}	LOW (SDA)		-	3	mA
	LOW (any other		-	4	mA
C_{Ld}	output load capacitance		-	40	pF
I_O	output leakage current		-	10	µA

Notes

1 The supply current may vary between 30 and 150 mA depending upon the input data. The minimum may be achieved with $\overline{OE}$ disabled and no clock

2 All inputs except $\overline{TEST}$ (internal pull-up resistor).

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
	propagation delay	note 2	-	26		t_{C16}
	CLOCK (DMSD-mode, LL27) :	note 3				
t_{C27}	cycle time		31	-	45	ns
	duty cycle		40	-	60	%
	CLOCK (16 MHz-mode) :	note 4				
t_{C16}	cycle time		62	-	83	ns
t_{CDL}	duty time LOW		30	-	-	ns
t_{CDH}	duty time HIGH		16	-	-	ns
	CREF					
t_{CS}	set-up time		11	-	-	ns
t_{CH}	hold time		3	-	-	ns
	HREF					
t_{HS}	set-up time		11	-	-	ns
t_{HH}	hold time		3	-	-	ns
t_{RH}	$\overline{\text{RESET}}$ hold time		4 clock periods			
	$\overline{\text{VLUTBYPASS}}$	note 5				
t_{VS}	set-up time		8	-	-	ns
t_{VH}	hold time		0	-	-	ns
	CLK_MODE set-up time		must be set before $\overline{\text{RESET}}$			
	I²C-bus address set-up time		must be set before $\overline{\text{RESET}}$			
	DATAIN					
t_{SU}	set-up time		11	-	-	ns
t_{HD}	hold time		3	-	-	ns
	DATAOUT					
t_{OS}	set-up time		10	-	-	ns
t_{OH}	hold time		10	-	-	ns
	HREF_OUT					
t_{OHS}	set-up time		9	-	-	ns
t_{OHH}	hold time		10	-	-	ns
t_{HZ}	output disable time (to tri-state)		-	10	15	ns
t_{ZH}	output enable time (from tri-state)			15	21	ns

Notes

1 Typical ratings are measured at V_{DD} = 5 V and 25 °C room temperature

2 Denotes the delay in clock periods between DATAIN and DATAOUT

3 DMSD-mode designates that the DCSC will workin a DMSD environment. The CLOCK and the clock reference signal CREF will be fed by the SCGC (SAA7157). This is further explained in the following diagrams.

4 16 MHz-mode indicates that the DCSC will work in any other environment. The CREF signal will be set internally to HIGH, the CLOCK signal can be any clock up to 16 MHz (see also Fig. 15.

5 Must be set one clock period before DATAOUT.

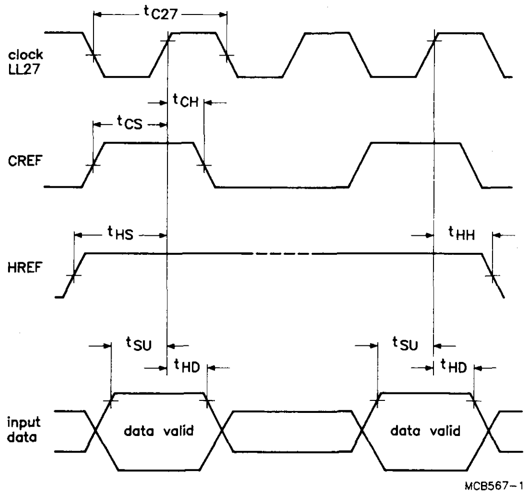


Fig.12 Timing diagram input.

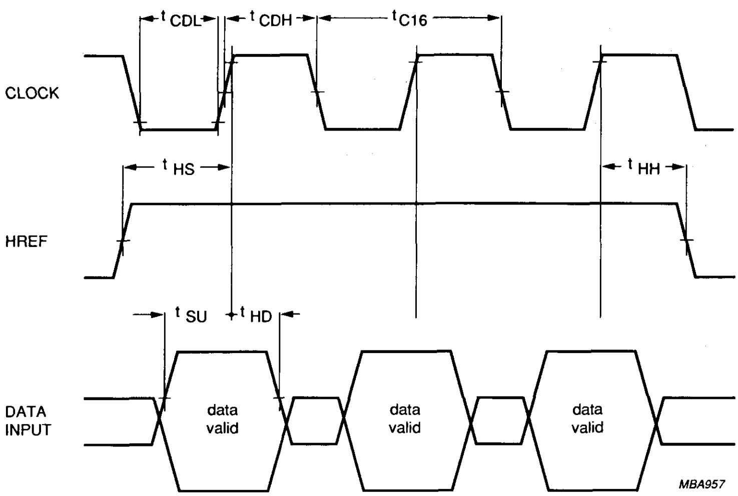
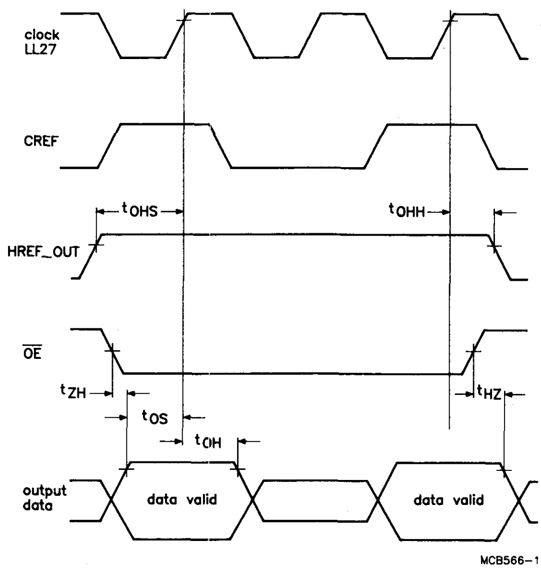


Fig.13 Timing diagram input (16 MHz mode).

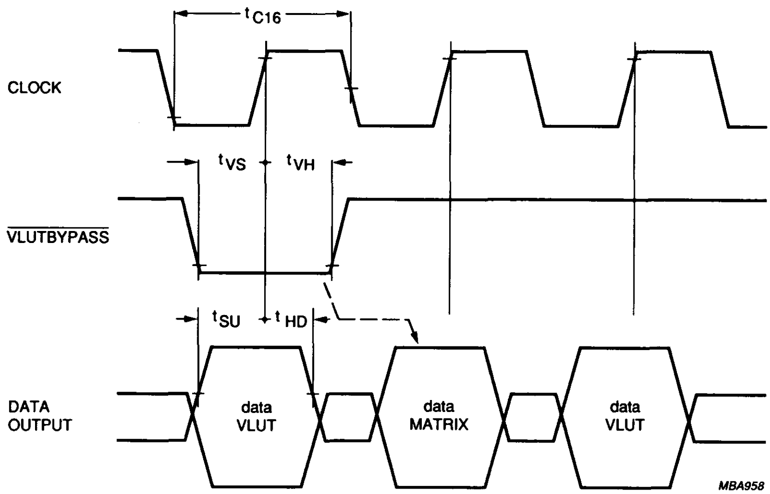


$\overline{OE}$ will also affect HREF_OUT

Fig.14 Timing diagram output.

Error condition

To inhibit unwanted operations, no information signal is available to the peripheral circuits. In the advent of an error the system must be re-started by application of the $\overline{RESET}$ signal.



VLUTBYPASS must be supplied one clock pulse in advance of the desired DATAOUT lines reaction.

Fig.15 Timing diagram VLUTBYPASS

SYSTEM BLOCK DESCRIPTION

Input formatter

The formatter consists of five functional blocks:

- the multiplexer, which decodes the luminance and chrominance input signals
- the filter, which interpolates the samples of the incoming signal to get an upsampled data rate as at DATAIN1
- the luminance delay line
- the timing control which creates the internal reference signals from the various inputs
- the bypass output multiplexer

The data applied at DATAIN1 to DATAIN3 is converted as follows;

FIL1 : Y Luminance
FIL2 : Cr colour-difference signal R-Y
FIL3 : Cb colour-difference signal B-Y

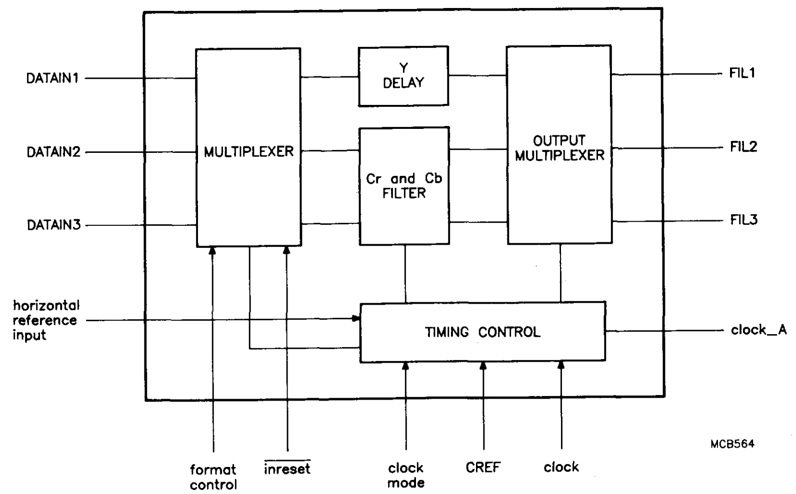


Fig.16 Input formatter.

Filter and delay line

In the various functional modes the signal FMTCNTRL switches in the required filters (FMTCNTRL is described in 'Control data'). In all modes the same propagation delay will be realized, (the reference is Cb0, respective to U7 with format 0).

At all frequencies and in all formats, there is a delay line to compensate for the delay of the signal processing time needed in the chrominance section.

CHROMINANCE FILTER

The filter for the Cr and Cb signal is realized in one filter design.

Format 1, 2 4:1:1

An interpolating filter is inserted to convert the original sampling frequency to the sampling frequency of the luminance signal i.e. four times that of the colour signal. Figure 17 illustrates the frequency response of the chrominance section.

Format 3, 4 4:2:2

An interpolating filter is inserted to convert the original sampling frequency to the sampling frequency of the luminance signal i.e. twice the colour signal. Figure 18 illustrates the frequency response of the chrominance section.

Format 5 4:4:4

A bypass with a specified delay is inserted.

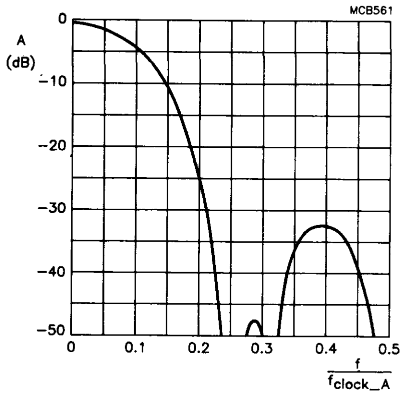


Fig.17 Frequency response of 4:1:1 filter.

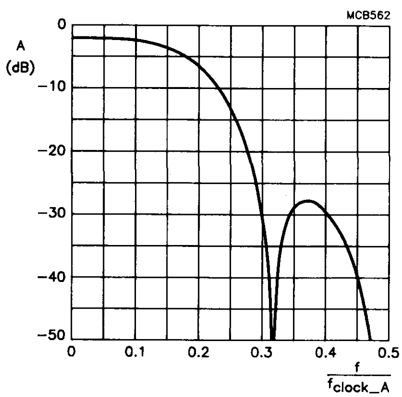


Fig.18 Frequency response of 4:2:2 filter

CONVERSION MATRIX

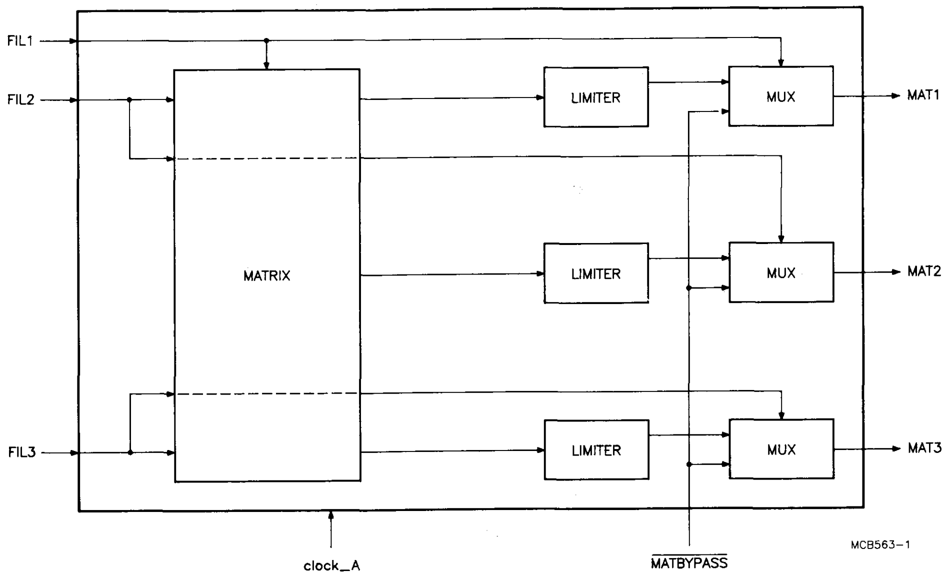


Fig.19 MATRIX block diagram.

The properties of the conversion matrix are as follows:

- the conversion equations are (according to CCIR 601, with respect to the different quantisation on Y, Cb and Cr);

  Red = Y + 1.371 (Cr - 0.5)
  Green = Y - 0.698 (Cr - 0.5) - 0.336 (Cb - 0.5)
  Blue = Y + 1.732 (Cb - 0.5)

- the accuracy of the signal processing is within ± 0.5% of the accuracy of a theoretical conversion.
- the input and output data lines are 8-bit.
- in the advent of non-standard input levels, the limiter reduces the possible output data values to between 0 and 255.
- $\overline{\text{MATBYPASS}}$ switches the matrix in bypass. The bypass has the same propagation delay as the matrix itself.

VIDEO LOOK-UP TABLE AND OUTPUT STAGE

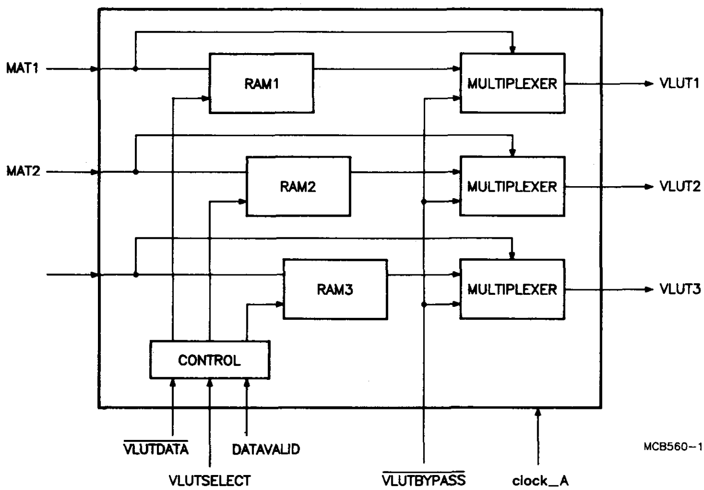


Fig.20 Block diagram video look up table.

Functional description

The $\overline{\text{VLUTLOAD}}$ will be set to the WRITE operation if one of the four addresses are received from the RAMs. $\overline{\text{VLUTLOAD}}$ will be set to the READ operation following reception of the last databyte.

VLUTSELECT provides selection of one VLUT according to the sub-address.

VLUTDATA contains the value for the address counter (VLUT_ADDRESS; the start address of the first byte to be written into the RAM) and the data for the RAMs, validated with DATAVALID.

The databytes will be loaded by an autoincrement function. $\overline{\text{VLUTBYPASS}}$ will bypass the VLUT's in clock period time (real time switch).

In computer applications the VLUT is also known as a Colour Look-Up Table (CLUT).

In the DCSC this table might be used to invert the Gamma-correction of a camera. This correction is applied to compensate for the non-linear relationship between the video voltage applied to the cathode and the light output of the phosphor of a CRT.

The Gamma-correction function (also known as Gradation) is given as;

$Y = X^{Y}$
The VLUT's are realized by 256 x 8-bit RAMs.

I^2C-bus RECEIVER

The DCSC can be switched to different functional modes via the I^2C-bus receiver. The I^2C-bus receiver is also used to feed the VLUT RAMs with data.

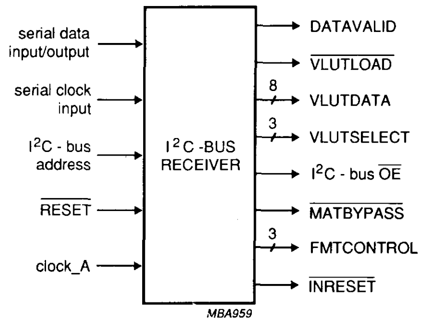


Fig.21 Block diagram of I^2C-bus receiver

I^2C-bus Receiver Functional Description

Following power-up, all internal control signals are at undefined values. The I^2C-bus receiver must be reset by the external $\overline{\text{RESET}}$ signal. Following $\overline{\text{RESET}}$ the control signals are set to:

FMTCNTRL	:=	100	format 4:4:4
$\overline{\text{MATBYPASS}}$	:=	0	matrix bypassed
$\overline{\text{INRESET}}$	:=	0	input data set to fixed values
IICOE	:=	1	$\overline{\text{OE}}$ enabled

RECEIVER ORGANISATION

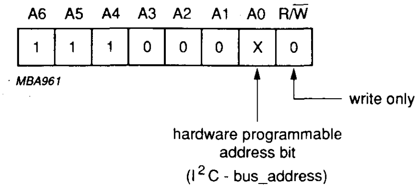


Fig.22 The address for the DCSC

THE CONTROL BYTE

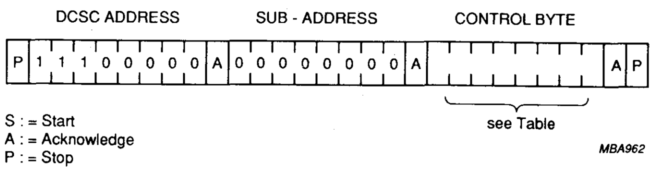


Fig.23 The address of the control byte is 00_{HEX}

In this example the control signals are set to:

FMTCNTRL	:=	2	Format 3	:	4:2:2 DMSD
$\overline{\text{MATBYPASS}}$	:=	1	matrix in use		
$\overline{\text{INRESET}}$	:=	0	input DATA at fixed values during HREF = 0		
IICOE	:=	1	$\overline{\text{OE}}$ enabled		

Table 20 Levels of the colour bar signal

CONDITION	E'_R	E'_G	E'_B	Y	C_R	C_B	R	G	B
White	1.0	1.0	1.0	235	128	128	235	235	235
Black	0	0	0	16	128	128	16	16	16
Red	1.0	0	0	82	240	90	236	17	16
Green	0	1.0	0	145	34	54	16	236	17
Blue	0	0	1.0	41	110	240	16	16	235
Yellow	1.0	1.0	0	210	146	16	235	235	16
Cyan	0	1.0	1.0	170	16	166	16	235	236
Magenta	1.0	0	1.0	106	222	202	235	15	234

Note

The colour bar signal is described in CCIR 601, Rep. 629-2, Table 1. It can be used to check the nominal levels (at least for black and white) between the functional blocks of the DCSC.

Table 21 Control byte formats

D7	D6	D5	D4	D3	D2	D1	D0	Functions
x	x	x	x	x	0	0	0	input formatter at format 0 Filter switched to 4:1:1 filter
x	x	x	x	x	0	0	1	input formatter at format 1 Filter switched to 4:1:1 filter
x	x	x	x	x	0	1	0	input formatter at format 2 Filter switched to 4:2:2 filter
x	x	x	x	x	0	1	1	input formatter at format 3 Filter switched to 4:2:2 filter
x	x	x	x	x	1	0	0	input formatter at format 4 Filter switched to bypass
x	x	x	x	0	x	x	x	matrix bypassed
x	x	x	x	1	x	x	x	matrix in use
x	x	x	0	x	x	x	x	input data at fixed values
x	x	x	1	x	x	x	x	input data to formatter
x	x	0	x	x	x	x	x	output stages tri-state
x	x	1	x	x	x	x	x	OE enabled

D0-D2	FMTCONTROL
D3	$\overline{\text{MATBYPASS}}$
D4	$\overline{\text{INRESET}}$
D5	IICOE
D6	not used
D7	not used

VLUTDATA

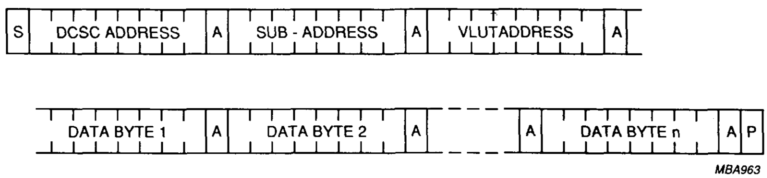
Four sub-addresses are implemented to convey data into the different VLUT RAMs. RAM can be addressed individually or together. The memory of each VLUT RAM can be addressed, e.g. if only parts of the data has to be changed.

Table 22 Sub-addresses VLUTDATA:

SUB-ADDRESS	VLUT-ADDRESS	DATA BYTEs
01	xx	VLUTDATA RAM 1 (RED)
02	xx	VLUTDATA RAM 2 (GREEN)
03	xx	VLUTDATA RAM 3 (BLUE)
04	xx	VLUTDATA RAM 1, 2, 3

Note

(*) addresses in HEX representation



S : = Start
A : = Acknowledge
P : = Stop

Fig.24 Sub-addresses VLUTDATA

I²C-bus receiver timing examples

The exact timing of the signals are described in the I²C-bus specification. The addresses indicated in the FIG. 25 are in HEX representation.

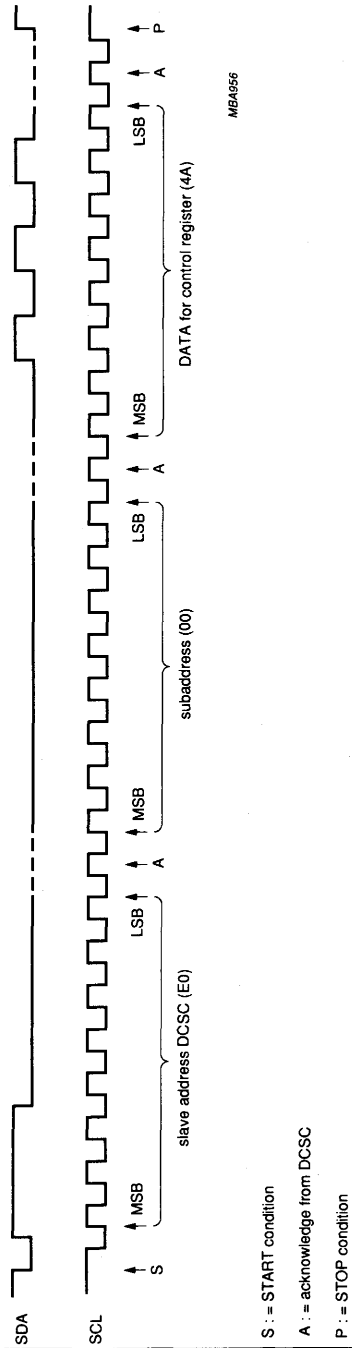
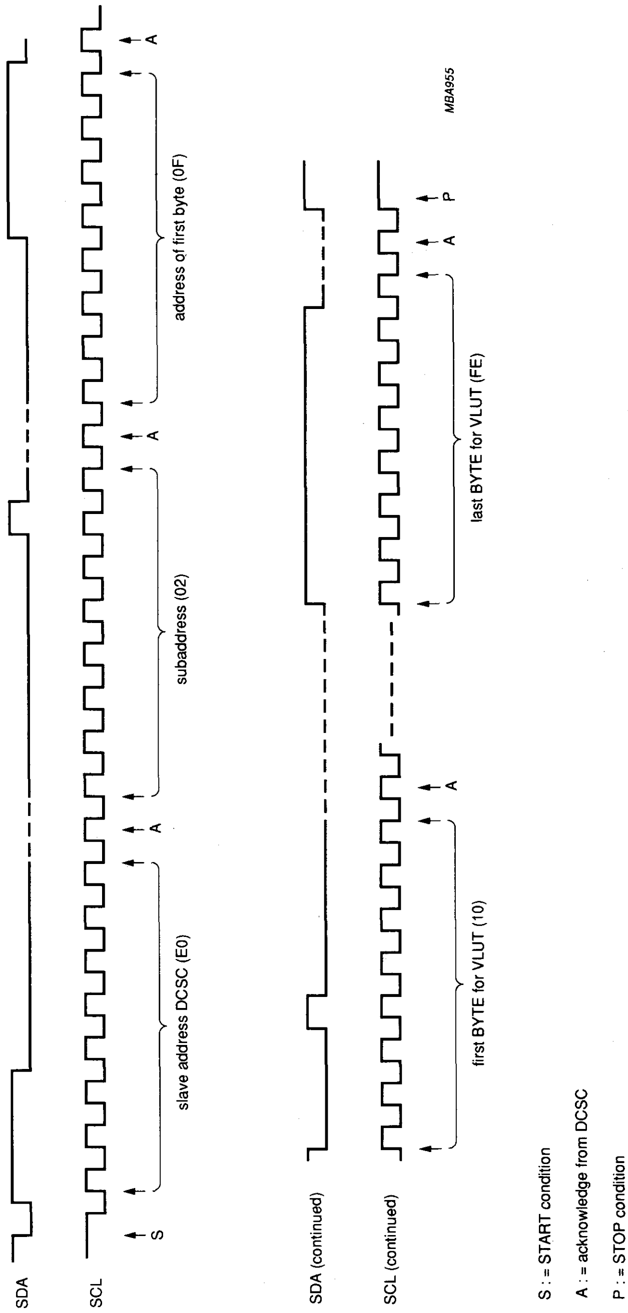


Fig.25 Example of control register loading.



In this example the second RAM (GREEN) receives new data at the start of address OF.
The VLUT addresses are automatically incremented by writing data via the SDA line.

Fig.26 Example of VLUT loading.

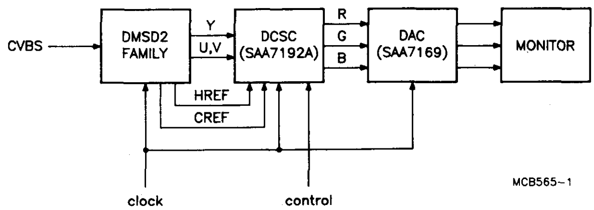


Fig.27 Application with DMSD2.

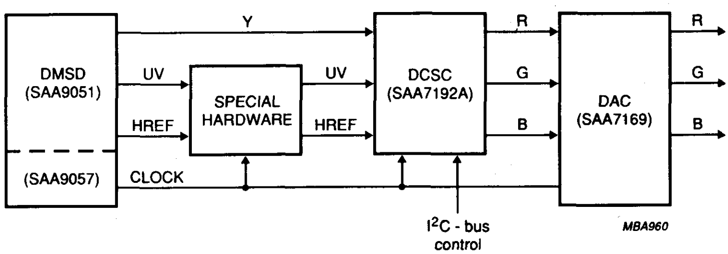


Fig.28 Application with SAA9051.

APPLICATION

The application is simple since the DCSC is designed to operate in conjunction with the DMSD2 decoder family.

Additional hardware is required to convert the level formats to permit the DCSC to be used with the older 7-bit version of the DMSD.

Due to the differing data formats between the SAA9051 and the SAA7192, the colour difference U and V signals must be converted from two's-complement to unipolar representation and the MSBs of the UV data must be inverted. Differing chrominance amplitudes are small and are not taken into account.

Additionally, the DATAIN10 (LSB of the Y-data) should be connected to ground and the DATAIN34 and DATAIN36 (LSBs of the UV data) should be connected to ground via a resistor to avoid noise at the LSBs.

GLOSSARY

B	colour component of a video signal (BLUE)
C	coded colour components of a video signal (TV)
Cb	coded colour difference signal (digital B-Y)
CCIR	Comite Consultatif International de Radiocommunication (International Radio Consultative Committee)
CDS-System	Chip Design System
CGC	Clock Generation Circuit
CLUT	Colour Look Up Table (personal computer graphics)
Cr	coded colour difference signal (digital R-Y)
CREF	Clock Reference Signal; indicates the valid data samples of the DMSD
CVBS	Composite Video Burst Synchron signal (TV)
DCSC	Digital Colour Space Converter; converts the YUV signal to RGB
DIN	Deutsches Institut fuer Normung, Berlin
DMSD	family of Digital Multi-standard Decoders, decodes YUV out of the CVBS signal.
G	colour component of a video signal (GREEN)
HDTV	High Definition Television
HREF	Horizontal Line Reference signal
I^2C-bus	Inter-IC-Bus (Valvo network concept between controllers
IRT	Institut fuer RundfunkTechnik (Muenchen)
IIC-DVP/SE	Philips Components RHW Hamburg, Department Industrial-ICs Video Products System Engineering
MIC-SE	Philips Components RHW Hamburg, Department MOS-ICs System Engineering (now called IIC-DVP-SE)
RGB	components of a video signal (red, green, blue)
R	colour component of a video signal (RED)
SCL	clock line of the I^2C-bus
SDA	data line of the I^2C-bus
SRC	Sample Rate Converter
Semiparallel	Chrominance data (multiplexed colour difference) parallel to luminance data
SERInet	Signetics Elcoma Research ISA Network (Philips computer interconnection network)
VLUT	Video Look Up Table. RAM to multiply video data with a factor
Y	luminance signal (brightness of a video signal)
YUV Bus	Component bus of the DMSD family
U	colour difference signal (coded video signal B-Y)
V	colour difference signal (coded video signal R-Y)

Digital video decoder and scaler circuit (DESC)

SAA7194

CONTENTS

1. FEATURES

- Digital 8-bit luminance input video (Y) or CVBS
- Digital 8-bit chrominance input (CVBS or C from CVBS, Y/C, S-video (S-VHS or Hi8))
- Luminance and chrominance signal processing for main standards PAL, NTSC and SECAM
- Horizontal and vertical sync detection for all standards
- User programmable luminance peaking for aperture correction
- Compatible with memory-based features (line-locked clock, square pixel)
- Cross-colour reduction by chrominance comb filtering for NTSC or special cross-colour cancellation for SECAM
- UV signal delay lines for PAL to correct chrominance phase errors
- Square-pixel format with 768/640 active samples per line
- The bidirectional Expansion Port (YUV-bus) supports data rates of 780 x f_H (NTSC) and 944 x f_H (PAL, SECAM) in 4:2:2 format
- Brightness, contrast, hue and saturation controls for scaled outputs
- Down-scaling of video windows with 1023 active samples per line and 1023 active lines per frame to randomly sized windows
- 2 D data processing for improved signal quality of scaled luminance data, especially for compression applications
- Chroma key (α-generation)
- YUV to RGB conversation including Anti-gamma ROM tables for RGB
- 16-word FIFO register for 32-bit output data
- Output configurable for 32/24/16-bit video data bus
- Scaled 16-bit 4:2:2 YUV output
- Scaled 15-bit RGB (5-5-5+α) and 24-bit (8-8-8+α) output
- Scaled 8-bit monochrome output
- Line increment, field sequence (odd/even, interlace/non-interlace), and vertical reset control for easy memory interfacing
- Output of discontinuous data bursts of scaled video data or continuous data output with corresponding qualifier signals
- Real-time status information
- I²C-bus control
- Only one crystal of 26.8 MHz

2. GENERAL DESCRIPTION

The CMOS circuit SAA7194, digital video decoder and scaler (DESC), is a highly integrated circuit for DeskTop Video applications. It combines the functions of a digital multistandard decoder (SAA7191B) and a digital video scaler (SAA7186).

The decoder is based on the principle of line-locked clock decoding. It runs at square-pixel frequencies to achieve correct aspect ratio.

Monitor controls are provided to ensure best display.

Four data ports are supported:

Ports CVBS(7-0) and CHR(7-0) of the input interface are used in Y/C mode (Fig.1(a)) to decode digitized luminance and chrominance signals (digitized in two external ADCs).

In normal mode, the CVBS(7-0) input is only used, and only one ADC is necessary (Fig.3).

The 32-bit VRAM output port is interface to the video memory; it outputs the down-scaled video data.

Different formats and operation modes are supported by this circuit.

The circuit is I^2C-bus-controlled. The I^2C-bus interface is clocked by LLC to ensure proper control.

The I^2C-bus control is divided into two sections:

- subaddress 00h to 1F for the decoder part (Tables 8 and 9)
- subaddress 20h to 3F for the scaler part (Tables 10 and 11)

The programming of the subaddresses for the scaler part becomes effective at the first vertical sync pulse VS after a transmission.

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5	5.5	V
$I_{DD\ tot}$	total supply current	-	170	250	mA
V_I	data input level	TTL-compatible			
V_O	data output level	TTL-compatible			
LLC	input clock frequency	-	-	32	MHz
T_{amb}	operating ambient temperature range	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7194	120	QFP	plastic	SOT349

5. BLOCK DIAGRAM

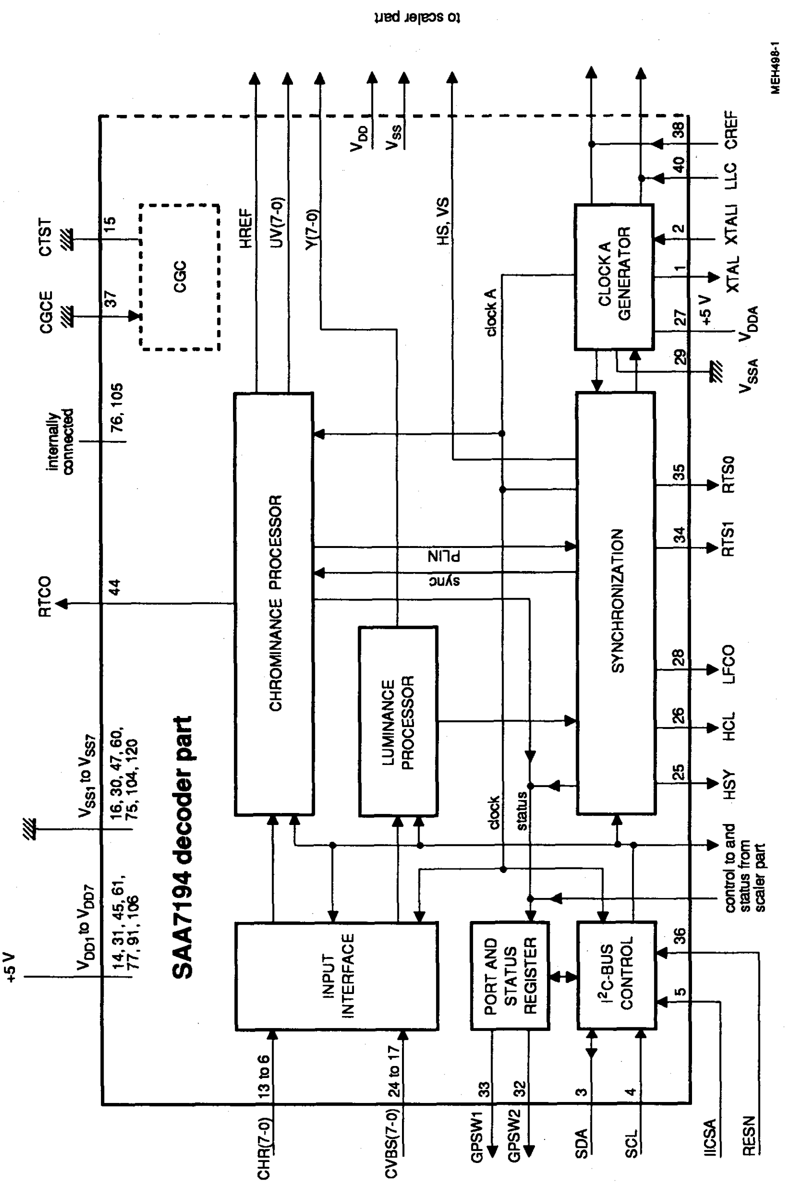


Fig.1(a) Block diagram of decoder part; (continued in Fig.1(b)).

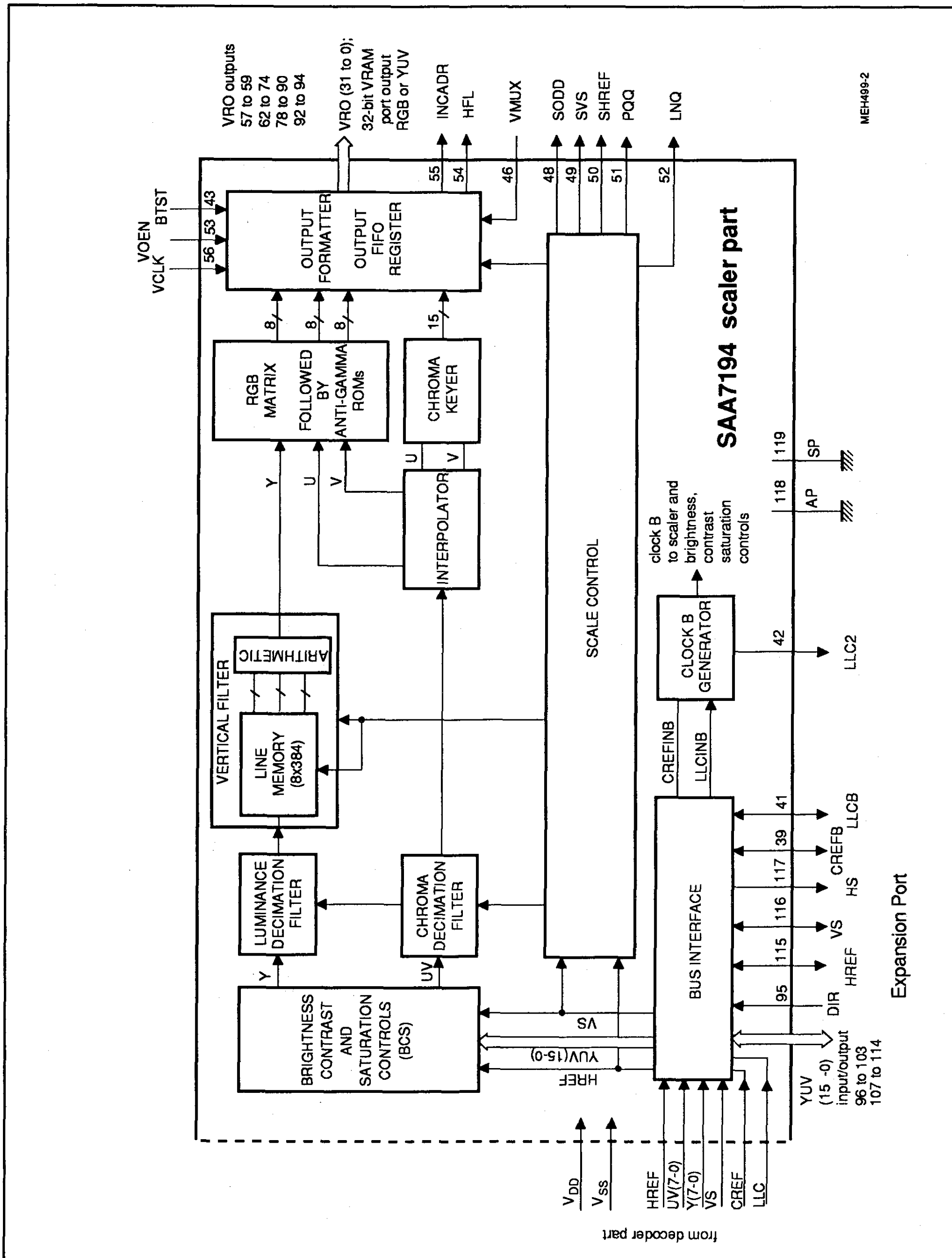


Fig.1(b) Block diagram of brightness, contrast, saturation controls and scaler part; (continued from Fig.1(a)).

6. PINNING

SYMBOL	PIN	STATUS	DESCRIPTION
XTAL	1	O	26.8 MHz crystal oscillator output, not used if TTL clock signal is used
XTALI	2	I	26.8 MHz crystal oscillator input, or external clock input (TTL, squarewave)
SDA	3	I/O	I^2C-bus data line
SCL	4	I	I^2C-bus clock line
IICSA	5	I	I^2C-bus set address
CHR0	6	I	digital chrominance input signal (bits 0 to 7)
CHR1	7	I	
CHR2	8	I	
CHR3	9	I	
CHR4	10	I	
CHR5	11	I	
CHR6	12	I	
CHR7	13	I	
V_{DD1}	14	-	+5 V supply voltage 1
CTST	15	-	connected to ground (clock test pin)
V_{SS1}	16	-	GND1 (0 V)
CVBS0	17	I	digital CVBS input signal (bits 0 to 7)
CVBS1	18	I	
CVBS2	19	I	
CVBS3	20	I	
CVBS4	21	I	
CVBS5	22	I	
CVBS6	23	I	
CVBS7	24	I	
HSY	25	O	horizontal sync indicator output (programmable)
HCL	26	O	horizontal clamping pulse output (programmable)
V_{DDA}	27	-	+5 V analog supply voltage
LFCO	28	O	line frequency control output signal to CGC (multiple of present line frequency)
V_{SSA}	29	-	analog ground (0 V)
V_{SS2}	30	-	GND2 (0 V)

SYMBOL	PIN	STATUS	DESCRIPTION
V_{DD2}	31	-	+5 V supply voltage 2
GPSW2	32	O	general purpose output 2 (settable via I^2C-bus)
GPSW1	33	O	general purpose output 1 (settable via I^2C-bus)
RTS1	34	O	real time status output 1 controlled by RTSE-bit
RTS0	35	O	real time status output 0 controlled by RTSE-bit
RESN	36	I	reset input (active-LOW for at least 30 clock cycles LLC)
CGCE	37	I	enable input for internal CGC (connected to ground)
CREF	38	I	clock qualifier input (HIGH indicates valid input data YUV(15-0) in 4:2:2 format)
CREFB	39	I/O	clock reference qualifier input/output (HIGH indicates valid input data YUV(15-0))
LLC	40	I	line-locked video system clock input, maximum 32 MHz (twice of pixel rate in 4:2:2 format)
LLCB	41	I/O	line-locked clock signal input/output, maximum 32 MHz (twice of pixel rate in 4:2:2 format)
LLC2	42	O	line-locked clock signal output (reserved for future enhancement)
BTST	43	I	connected to ground; BTST = HIGH sets all outputs (except pins 1 and 28) to high-impedance state (testing)
RTCO	44	O	real time control output
V_{DD3}	45	I	+5 V supply voltage 3
VMUX	46	I	VRAM output multiplexing, control input for the 32- to 16-bit multiplexer (Table 3)
V_{SS3}	47	I	GND3 (0 V)
SODD	48	O	odd/even field sequence reference output related to the scaler output (test only)
SVS	49	O	vertical sync signal related to the scaler output (test only)
SHREF	50	O	delayed HREF signal related to the scaler output (test only)
PXQ	51	O	pixel qualifier output signal to mark active pixels of a qualified line (polarity: QPP-bit; test only)
LNQ	52	O	line qualifier output signal to mark active video phase (polarity: QPP-bit; test only)
VOEN	53	I	enable input of VRAM output
HFL	54	O	FIFO half-full flag output signal
INCADR	55	O	line increment / vertical reset control output
VCLK	56	I	clock input signal of FIFO output
VRO31	57	O	32-bit digital VRAM output port (bits 31 to 29)
VRO30	58	O	
VRO29	59	O	
V_{SS4}	60	-	GND4 (0 V)

SYMBOL	PIN	STATUS	DESCRIPTION
V_{DD4}	61	-	+5 V supply voltage 4
VRO28	62	O	32-bit VRAM output port (bits 28 to 16)
VRO27	63	O	
VRO26	64	O	
VRO25	65	O	
VRO24	66	O	
VRO23	67	O	
VRO22	68	O	
VRO21	69	O	
VRO20	70	O	
VRO19	71	O	
VRO18	72	O	
VRO17	73	O	
VRO16	74	O	
V_{SS5}	75	-	GND5 (0 V)
i.c.	76	-	internally connected
V_{DD5}	77	-	+5 V supply voltage 5
VRO15	78	O	32-bit VRAM output port (bits 15 to 3)
VRO14	79	O	
VRO13	80	O	
VRO12	81	O	
VRO11	82	O	
VRO10	83	O	
VRO9	84	O	
VRO8	85	O	
VRO7	86	O	
VRO6	87	O	
VRO5	88	O	
VRO4	89	O	
VRO3	90	O	

SYMBOL	PIN	STATUS	DESCRIPTION
V_{DD6}	91	-	+5 V supply voltage 6
VRO2	92	O	32-bit VRAM output port (bits 2 to 0)
VRO1	93	O	
VRO0	94	O	
DIR	95	I	direction control of Expansion Bus
YUV15	96	I/O	digital 16-bit video input/output signal (bits 15 to 8): luminance (Y)
YUV14	97	I/O	
YUV13	98	I/O	
YUV12	99	I/O	
YUV11	100	I/O	
YUV10	101	I/O	
YUV9	102	I/O	
YUV8	103	I/O	
V_{SS6}	104	-	GND6 (0 V)
i.c.	105	-	internally connected
V_{DD7}	106	-	+5 V supply voltage 7
YUV7	107	I/O	digital 16-bit video input/output signal (bits 7 to 0): colour-difference signals (UV)
YUV6	108	I/O	
YUV5	109	I/O	
YUV4	110	I/O	
YUV3	111	I/O	
YUV2	112	I/O	
YUV1	113	I/O	
YUV0	114	I/O	
HREF	115	I/O	horizontal reference signal
VS	116	I/O	vertical sync input/output signal with respect to the YUV input signal
HS	117	O	horizontal sync signal, programmable
AP	118	I	connected to ground (action pin for testing)
SP	119	I	connected to ground (shift pin for testing)
V_{SS7}	120	-	GND7 (0 V)

PIN CONFIGURATION

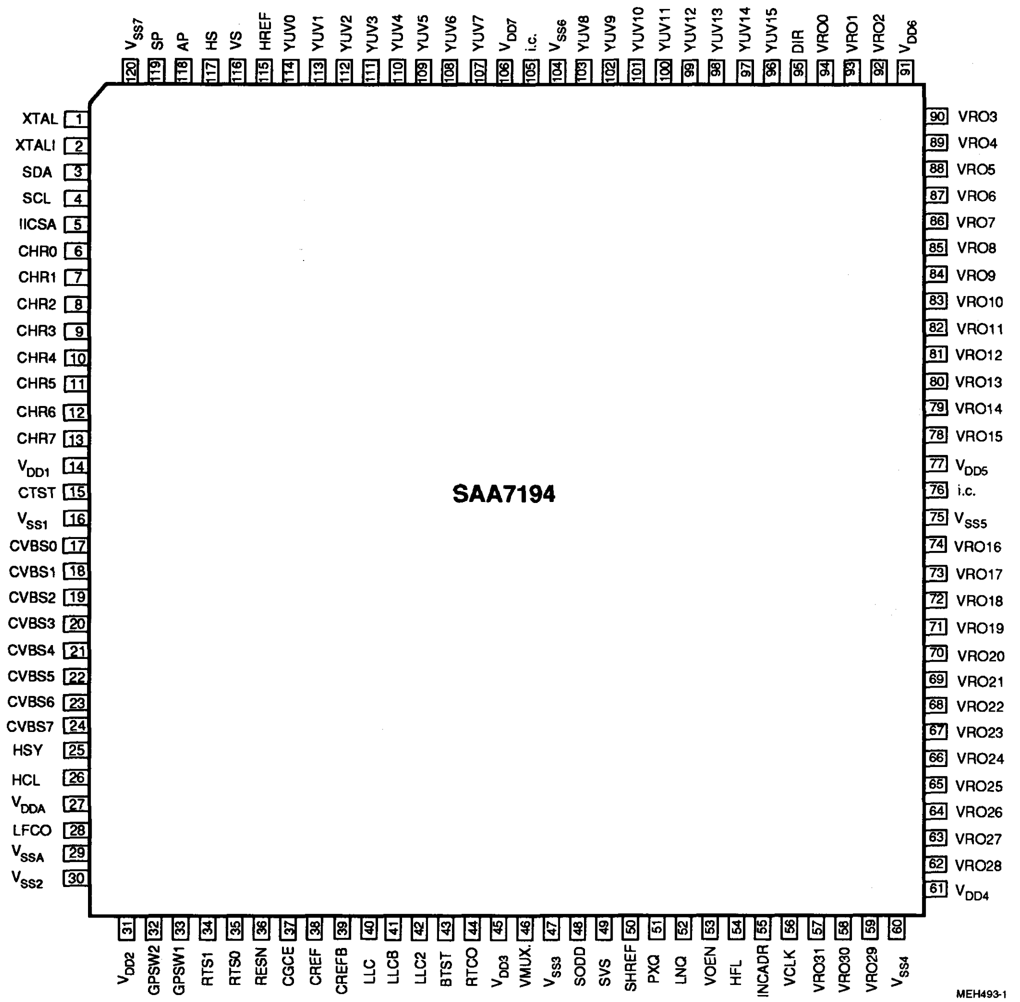


Fig.2 Pin configuration.

7. FUNCTIONAL DESCRIPTION

7.1. FUNCTIONAL DESCRIPTION DECODER PART

PAL, NTSC and SECAM standard colour signals based on line-locked clock are decoded (Fig.25). In Y/C mode (Fig.1(a)), digitized luminance CVBS(7-0) and chrominance CHR(7-0) signals – digitized in two external ADCs – are input. In normal mode only CVBS(7-0) is used. The data rate is 29.5 MHz (50 Hz systems) or 24.54 MHz (60 Hz systems).

Chrominance processor

The input signal passes the input interface, the chrominance bandpass filter to eliminate DC components, and is finally fed to the multiplicator inputs of a quadrature demodulator, where two subcarrier signals (0° and 90° phase-shifted) from a local digital oscillator (DTO1) are applied. The frequency is dependent on the present colour standard. The signals are low-pass filtered and amplified in a gain-controlled amplifier. A final low-pass stage provides a correct bandwidth performance.

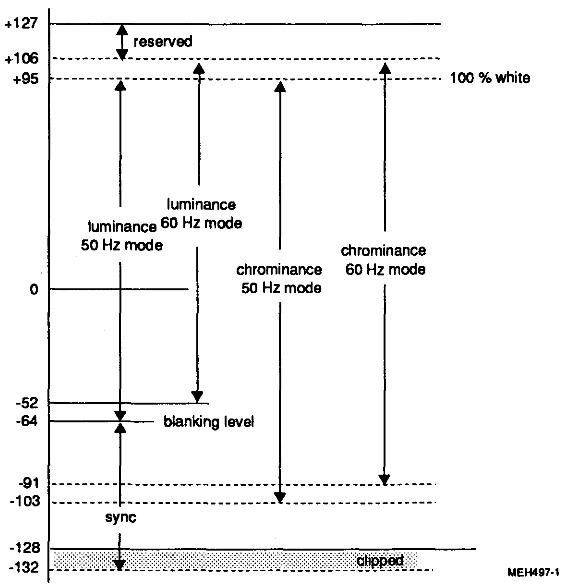
PAL signals are comb-filtered to eliminate crosstalk between the chrominance channels according to PAL standard requirements.

NTSC signals are comb-filtered to eliminate crosstalk from luminance to chrominance for vertical structures.

SECAM signals are fed through a cloche filter, a phase demodulator and a differntiator to achieve proportionality to the instantaneous frequency. The signals are de-multiplexed in the SECAM recombination stage after passing a de-emphasis stage to provide the two serially transmitted colour-difference signals.

The PLL for quadrature demodulation is closed via the cloche filter (to improve noise performance), a phase demodulator, a burst gate accumulator, a loop filter PI1 and a discrete time oscillator DTO1. The gain control loop is closed via the cloche filter, amplitude detector, a burst gate accumulator and a loop filter PI2.

The sequence processor switches signals according to standards.



Notes: All levels are related to EBU colour bar.
Values in decimal at 100 % luminance and 75 % chrominance amplitude.

Fig.3 CVBS(7-0) input signal ranges.

Luminance processor

The data rate of the input signal is reduced to LLC2 frequency by a sample rate converter on the output of the input interface. The high frequency components are emphasized in a prefilter to compensate for losses in the succeeding chrominance trap. The chrominance trap can be adjusted to a center frequency of 3.58 MHz (NTSC) or 4.4 MHz (PAL, SECAM) to eliminate most of the colour carrier components. The chrominance trap is bypassed for S-VHS signals.
The high frequency components in luminance signal are "peaked" using a bandpass filter and a coring stage. The "non-peaked" signals is added to the "peaked" one and output via variable delay to the Expansion-Bus.

Synchronization

The sync input signal is reduced in bandwidth to 1 MHz before it is sliced and separated from luminance signal. The sync pulses are compared in a detector with the divided clock signal of a counter. The resulting output signal is fed to a loop filter that accumulates all the phase deviations. Thereby, a discrete time oscillator DTO2 is driven generating the line frequency control signal LFCO. An external PLL generates the line-locked clock LLC from the signal LFCO.
A noise-limited vertical deflection pulse is generated for vertical processing that also inserts artificial pulses if vertical input pulses are missing.
50/60 Hz as well as odd/even field is automatically detected by the identification stage.

7.2. FUNCTIONAL DESCRIPTION EXPANSION PORT (Fig.1(b))

The Expansion port is a bidirectional interface for digital video signals YUV(15-0) in 4:2:2 format (Table 2). External video signals can be inserted to the scaler or decoded video signals of the decoder part can be output.
The data direction is controlled by pin 95 (DIR = HIGH: data from external; Table 1).

YUV(15-0), HREF, VS, LLCB, CREFB and HS pins are input when bits OECL, OEHV, OEYC of subaddress 0E are set to "0".Different modes are provided (timing see Figures 5 and 6):

Mode 0:
All bidirectional terminals are outputs. The signal of the decoder part (internal YUV(15-0)) is switched to be scaled.

Mode 1:
External YUV(15-0) is input to the scaler. LLCB/ CREFB clock system and HREF/VS from the SAA7194 are used to control the external source.
It is possible to switch between Mode 0 and Mode 1 by means of DIR input (Fig.4).
Pixelwise switching of the scaler source is possible because the internal clock and sync sources are used.

Mode 2:
External YUV(15-0) is input to the scaler. LLCB/CREFB clock system and HREF/VS from external are used.

Mode 3:
YUV(15-0) and HREF/VS terminals are inputs. External YUV(15-0) is input to the scaler with HREF/VS reference from external. LLC/ CREF clock system of the SAA7194 is used.

Table 1 Operation modes

MODE	I²C BIT OEYC	OEHV	OECL	DIR PIN 95	INPUT SOURCE YUV	HREF	VS	LLCB	CREFB
0	1	1	1	LOW	O	O	O	O	O
1	X	1	1	HIGH	I	O	O	O	O
2	X	0	0	HIGH	I	I	I	I	I
3	X	0	1	HIGH	I	I	I	O	O

X = don´t care; I = input to monitor control/scaler; O = output from decoder

7.3. MONITOR CONTROLS

(BCS; Fig.1(b)).

YUV input signals are selected by DIR (pin 95). The internal data timing is twice the input clock rate (LLC), for the Y and UV data are multiplexed for economical use of the multiplier stage.

BRIGHTNESS AND CONTRAST CONTROLS:

The luminance signal can be controlled via I^2C-bus (Table 8) by the bits BRIG(7-0) and CONT(6-0).

Brightness control:	value
00 (hex)	minimum offset
80 (hex)	CCIR level
FF (hex)	maximum offset

Contrast control:	value
00 (hex)	luminance off
40 (hex)	CCIR level
7F (hex)	1.9999 amplitude

SATURATION CONTROL:

The chrominance signal can be controlled via I^2C-bus (Table 8) by the bits SAT(6-0) and HUE(7-0).

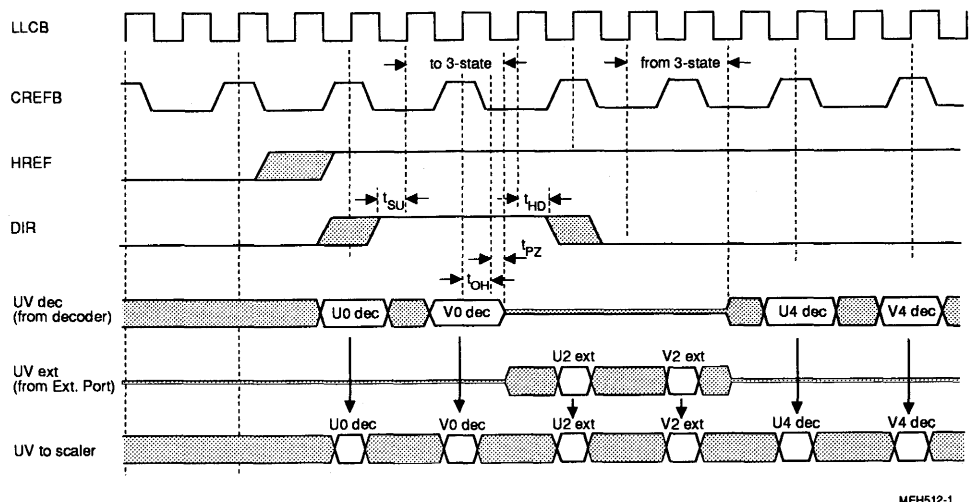
Saturation control:	value
00 (hex)	colour off
40 (hex)	CCIR level
7F (hex)	1.9999 amplitude

Clipping:
All resulting output values are clipped to minimum (equals 1) and maximum (equals 254).

Table 2 YUV-bus format on Expansion Port

PIN	SIGNALS ON EXPANSION PORT (PIXEL BYTE SEQUENCE ON PINS)				
YUV15	Ye7	Yo7	Ye7	Yo7	Ye7
YUV14	Ye6	Yo6	Ye6	Yo6	Ye6
YUV13	Ye5	Yo5	Ye5	Yo5	Ye5
YUV12	Ye4	Yo4	Ye4	Yo4	Ye4
YUV11	Ye3	Yo3	Ye3	Yo3	Ye3
YUV10	Ye2	Yo2	Ye2	Yo2	Ye2
YUV9	Ye1	Yo1	Ye1	Yo1	Ye1
YUV8	Ye0	Yo0	Ye0	Yo0	Ye0
YUV7	Ue7	Ve7	Ue7	Ve7	Ue7
YUV6	Ue6	Ve6	Ue6	Ve6	Ue6
YUV5	Ue5	Ve5	Ue5	Ve5	Ue5
YUV4	Ue4	Ve4	Ue4	Ve4	Ue4
YUV3	Ue3	Ve3	Ue3	Ve3	Ue3
YUV2	Ue2	Ve2	Ue2	Ve2	Ue2
YUV1	Ue1	Ve1	Ue1	Ve1	Ue1
YUV0	Ue0	Ve0	Ue0	Ve0	Ue0
Pixel order	n	n+1	n+2	n+3	n+4

e = even pixel number; o = odd pixel number



$t_{from\ 3\text{-}state\ min} = 1.5\ LLC + t_{PZ\ min}$

$t_{from\ 3\text{-}state} > t_{to\ 3\text{-}state}$

$t_{to\ 3\text{-}state\ max} = 1.5\ LLC + t_{PZ\ max}$

Fig.4 Real-time switching between Mode 0 and Mode1 (internal/external YUV(15-0)).

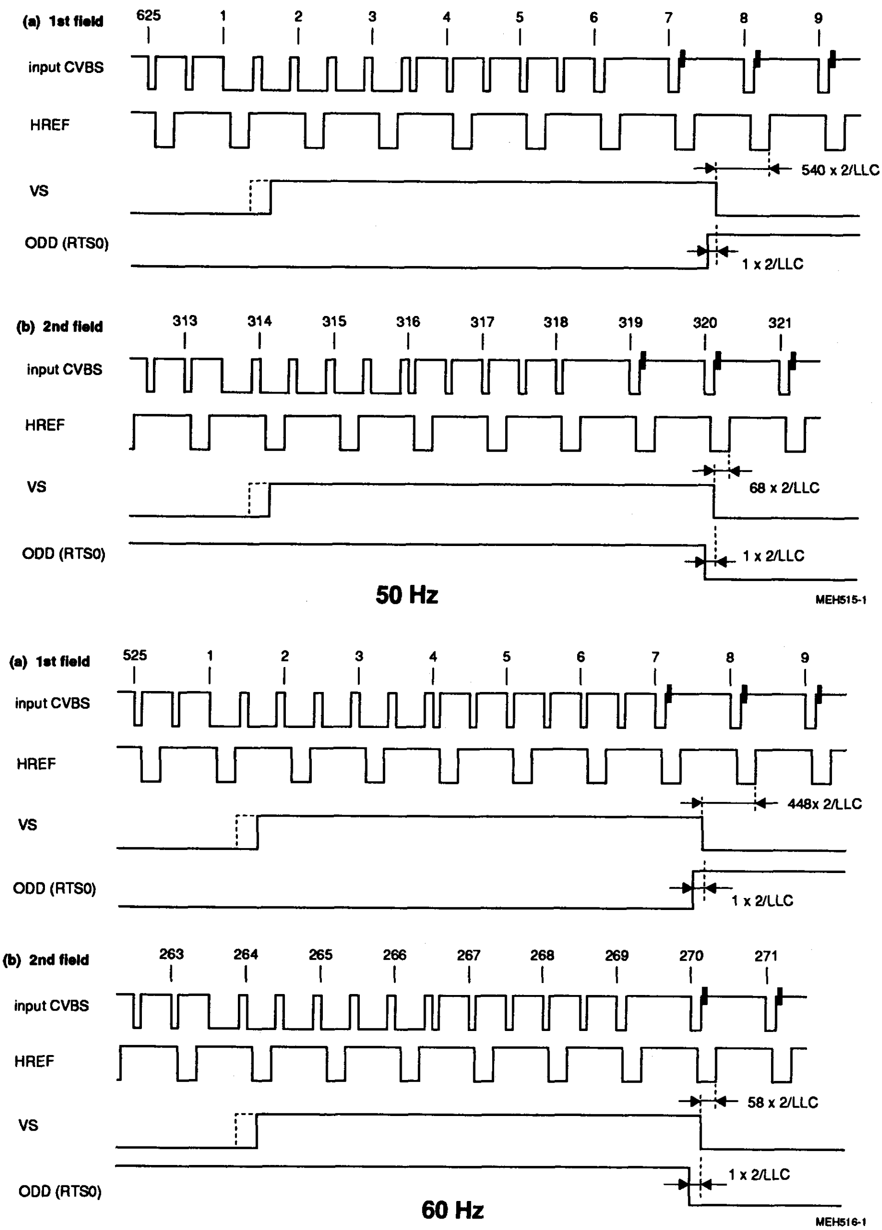


Fig.5 VS and ODD timing on Expansion Port.

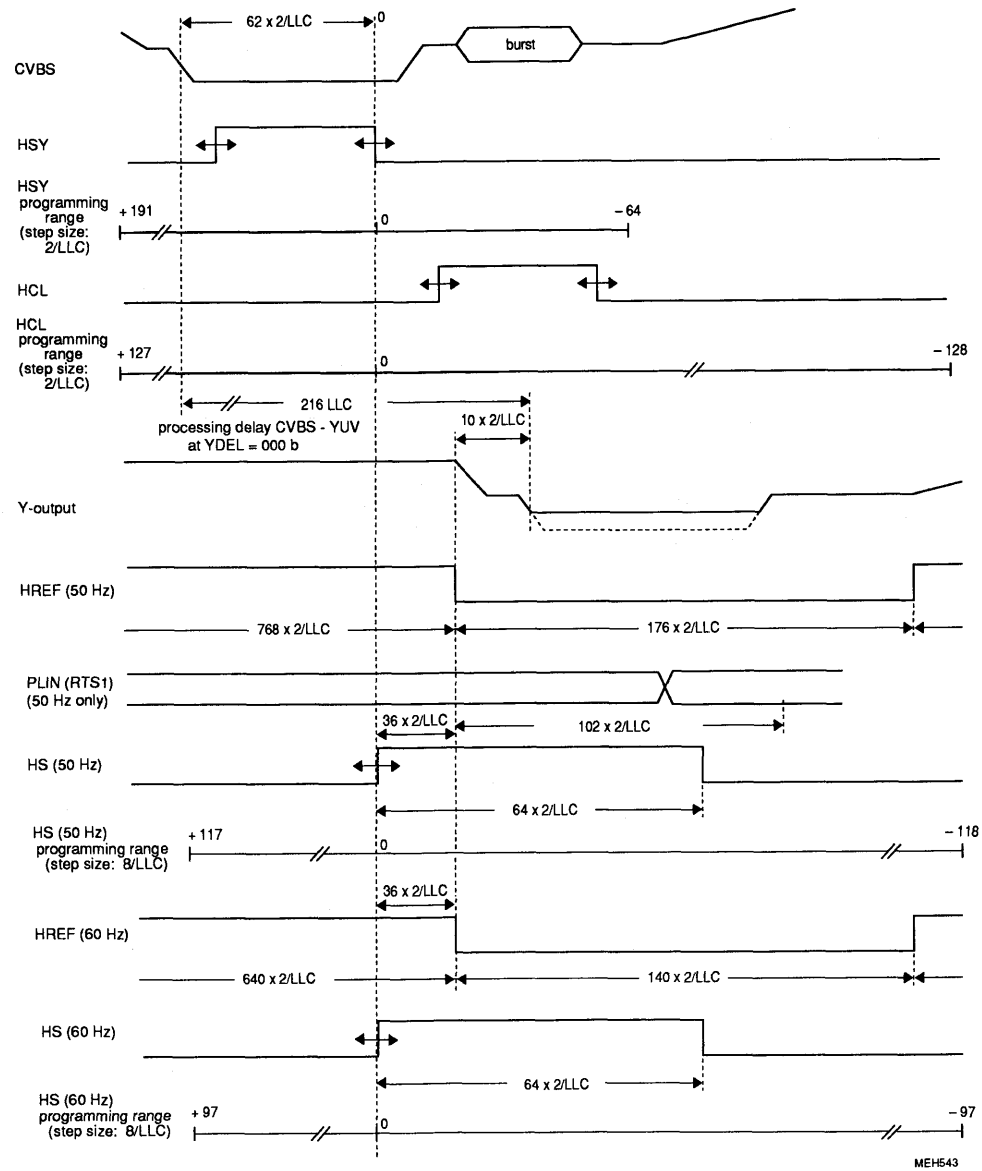


Fig.6 Horizontal sync timing at HRMV = 0 and HRFS = 0 (signals HSY, HCL, HREF, PLIN and HS (50/60 Hz)).

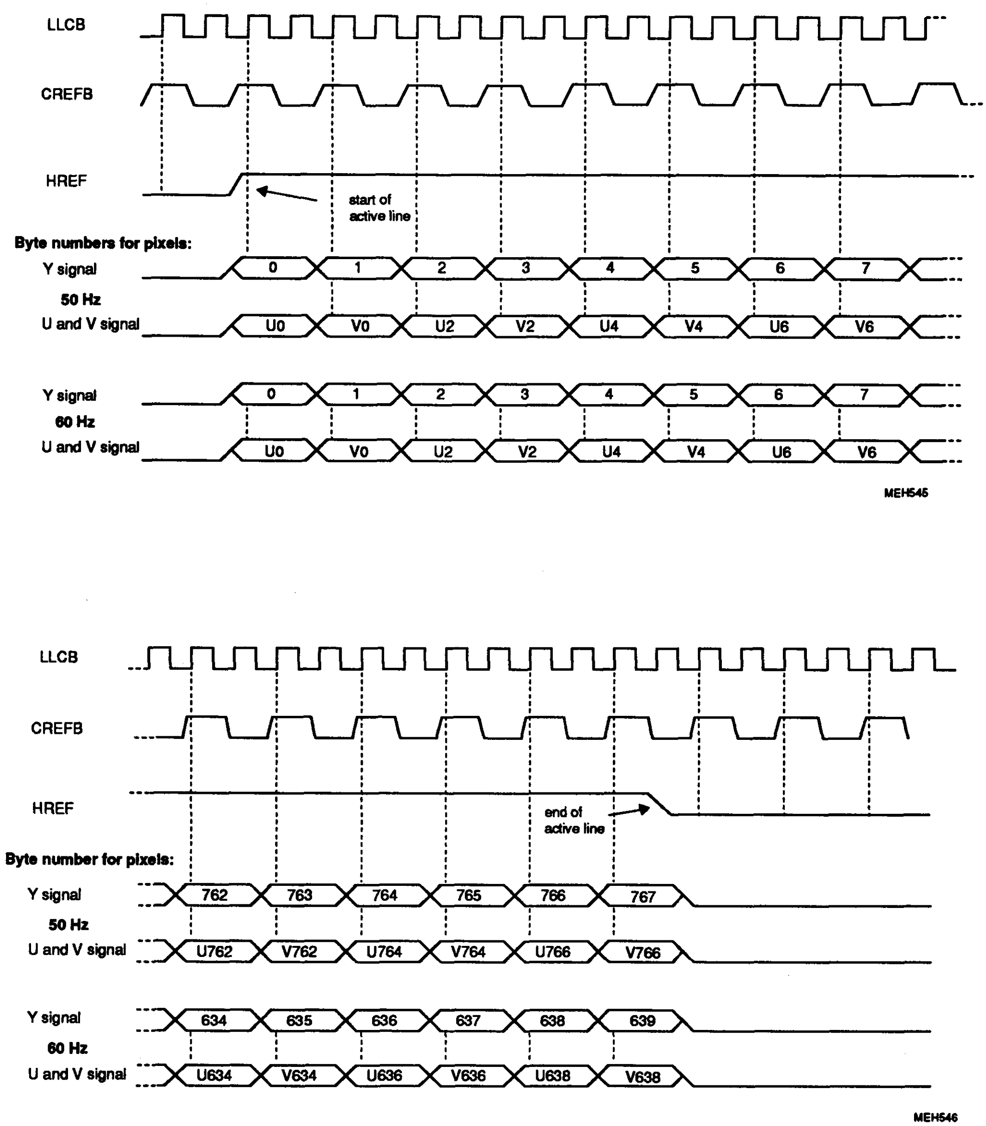


Fig.7 Horizontal and data multiplex timing on Expansion Port.

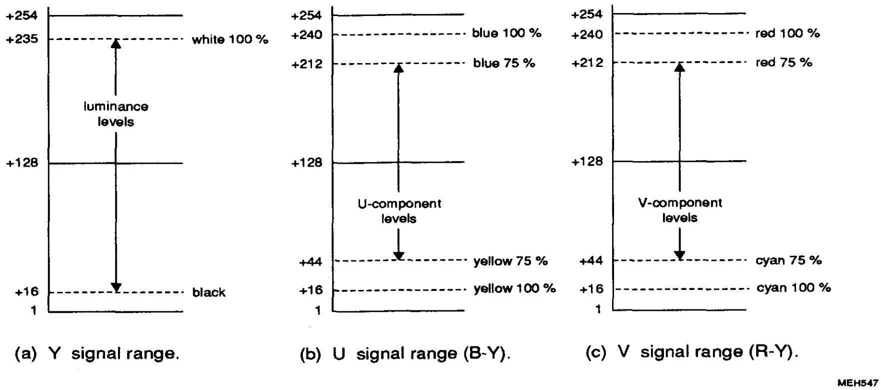


Fig.8 Input and output signal levels on Expansion Port.

RTCO output (pin 44; Fig.9)

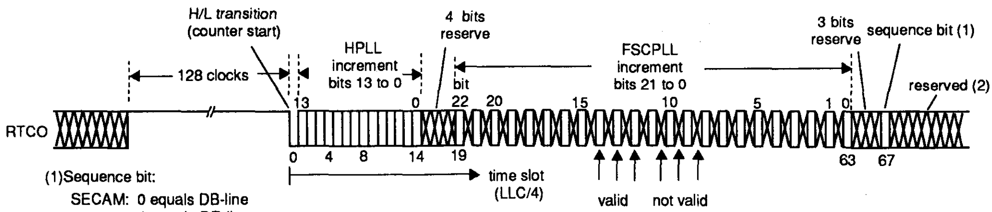
This real-time control and status output signal contains serial information abaut actual system clock, subcarrier frequency and PAL/SECAM sequence. The signal can be used for various applications in external circuits, e. g. in a digital encoder to achieve "clean" encoding.

RTS1 and RTS0 outputs
(pins 34 and 35)

These outputs can be configured in two modes dependent on RTSE bit (subaddress 0D).

RTSE = 0: the output RTS0 contains the odd/even field identification bit (HIGH equals odd); output RTS1 contains the PAL/SECAM sequence bit (HIGH equals non-inverted (R-Y)-line / DB-line)

RTSE = 1: the output RTS0 contains the horizontal lock bit (HIGH equals PLL locked); output RTS1 contains the vertical detection bit (HIGH equals vertical sync detected)



(1)Sequence bit:
SECAM: 0 equals DB-line
1 equals DR-line
PAL: 0 equals (R-Y) line normal
1 equals (R-Y) line inverted
NTSC: 0 (no change)

(2) Reserve bits: 276 for 50 Hz systems; 188 for 60 Hz systems

Fig.9 RTCO timing.

7.4. FUNCTIONAL DESCRIPTION SCALER PART

The scaler part receives YUV(15-0) input data in 4:2:2 format.
The video data from the BCS control are processed in horizontal direction in two separate decimation filters.
The luminance component is also processed in vertical direction (VPU_Y).
Chrominance data are interpolated to a 4:4:4 format; a chroma keying bit is generated.
The 4:4:4 YUV data are then converted from the YUV to the RGB domain in a digital matrix. ROM tables in the RGB data path can be used for anti-gamma correction of gamma-corrected input signals.
Uncorrected RGB and YUV signals can be bypassed.
A scale control unit generates reference and gate signals for scaling of the processed video data.
After data formatting to the various VRAM port formats, the scaled video data are buffered in the 16 word 32-bit output FIFO register. The scaling is performed by pixel and line dropping at the FIFO input. The FIFO output is directly connected to the VRAM output bus VRO(31-0).
Specific reference signals support an easy memory interfacing.

Decimation filters

The decimation filters perform accurate horizontal filtering of the input data stream.
Signal bandwith are matched in front of the pixel decimation stage, thus disturbing artifacts, caused by the pixel dropping, are reduced.
The signal bandwidth can be reduced in steps of (Figures 27 and 28):

2-tap filter = –6 dB at 0.325 pixel rate
3-tap filter = –6 dB at 0.25 pixel rate
4-tap filter = –6 dB at 0.21 pixel rate
5-tap filter = –6 dB at 0.125 pixel rate
9-tap filter = –6 dB at 0.075 pixel rate

The different characteristics are choosen independently by I²C-bus control bits HF2 to HF0 when AFS = 0 (Subaddress 28). In the adaptive mode with AFS = 1, the filter characteristics are choosen dependent on the defined sizing parameters.

Vertical processing (VPU–Y)

Luminance data are fed to a vertical filter consisting of a 384 x 8-bit RAM and an arithmetic block (Fig.1(b)).
Sub-sampling and interpolation operations are applied. The luminance data are processed in vertical direction to preserve the video information for small scaling factors and to reduce artifacts caused by line dropping.
The available modes respectively transfer functions are selectable by bits VP1 and VP0 (subaddress 28).
Adaptive modes, controlled by AFS and AFG bits (subaddresses 28 and 30) are also available.

Adaptive filter selection (AFS = 1):

scaling ratio	filter function (refer to I²C section)
XD/XS	horizontal
≤1	bypassed
≤14/15	filter 1
≤11/15	filter 6
≤7/15	filter 3
≤3/15	filter 4
YD/YS	vertical
≤1	bypassed
≤13/15	filter 1
≤4/15	filter 2

RGB matrix

Y data and UV data are converted after interpolation into RGB data according to CCIR601 recommendation.
Data are bypassed in 16-bit YUV formats or monochrome modes.

The matrix equations are these considering the digital quantization:

$$R = Y + 1.375\,V$$
$$G = Y - 0.703125\,V - 0.34375\,U$$
$$B = Y + 1.734375\,U$$

Anti-gamma ROM tables:
ROM tables are implemented at the matrix output to provide anti-gamma correction of the RGB data. A curve for a gamma of 1.4 is implemented.
The tables can be used (RTB-bit = 0, subaddress 20) to compensate gamma correction for linear data representation of RGB output data.

Chrominance signal keyer

The keyer generates an alpha signal to achieve a 5-5-5 +α RGB alpha output signal. Therefore, the processed UV data amplitudes are compared with thresholds set via I²C-bus (subaddresses "2C to 2F").
A logical "1" signal is generated if the amplitude is inside the specified amplitude range, otherwise a logical "0" is generated.
Keying can be switched off by setting the lower limit higher than the upper limit ("2C or 2E" and "2D or 2F").

Scale control and vertical regions

The scale control block SC includes vertical address/sequence counters to define the current position in the input field and to address the internal VPU memories.
To perform scaling, XD of XS pixel selection in horizontal direction and YD of YS line selection in vertical direction are applied. The pixel and line dropping are controlled at the input of the FIFO register.
The scaling ratio in horizontal and vertical direction is estimated to control the decimation filter function and the vertical data processing in the adaptive mode (AFS and AFG bits).
The input field can be divided into two vertical regions – the bypass region and the scaling region, which are defined via I²C-bus by the parameters VS, VC, YO and YS.

Vertical bypass region:
Data are not scaled, and independent of IIC-bits FS1 and FS0, the output format is always 8-bit grayscale (monochrome). The SAA7194 outputs all active pixels of a line, defined by the HREF input signal if the vertical bypass region is active.
This can be used, for example, to store videotext information in the field memory.

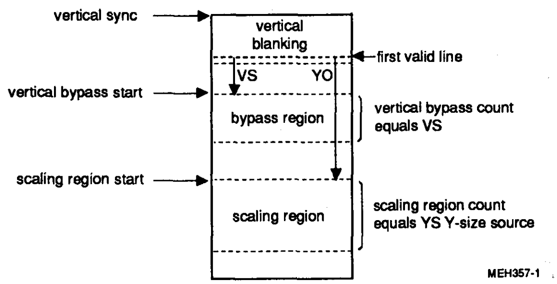


Fig.10 Vertical regions.

The start line of the bypass region is defined by the I²C-bits VS; the number of lines to be bypassed is defined by VC.

Vertical scaling region:

Data is scaled with start at line YO and the output format is selected when FS1 and FS0 are valid.
This is the "normal operation" area. The input/output screen dimensions in horizontal and vertical direction are defined by the parameters

XO, XS and XD for horizontal

YO, YS and YD for vertical.

The circuit processes XS samples of a line. Remaining pixels are ignored if a line is longer than XS. If a line is shorter than XS, processing is aborted when the falling edge of HREF is detected. In this case the output line will have less than XD samples.

Vertical regions in Fig.10:

- the two regions can be programmed via I²C-bus, whereby regions should not overlap (active region overrides the bypass region).
- the start of a normal active picture depends on video standard and has to be programmed to the correct value.
- the offsets XO and YO have to be set according to the internal processing delays to ensure the complete number of destination pixels and lines (Table 11).
- the scaling parameters can be used to perform a panning function over the video frame/field.

Output data representation and levels

Output data representation of the YUV data can be modified by bit MCT (subaddress 30).
The DC gain is 1 for YUV input data. The corresponding RGB levels are defined by the matrix equations, they are limited to the range of 1 to 254 in the 8-bit domain according to CCIR 601.

The luminance levels can be limited to:

16 (239) = black
235 (20) = white
(..) = grayscale luminance levels

(if the YUV or monochrome luminance output formats are selected and LLV-bit = 1).

For the 5-bit RGB formats a truncation from 8-bit to 5-bit word width is implemented. Fill values are inserted dependent on longword position and destination size (see data burst transfer mode):

- "1" for 24-bit RGB, Y and two's complement UV
- "128" for UV (straight binary)
- "254" in 8-bit grayscale format.

Output FIFO register and VRAM port

The output FIFO register is the buffer between the video data stream and the VRAM data input port. Resized video data are buffered and formatted. 32-, 24- and 16-bit video data modes are supported. The various formats are selected by the bits EFE, VOF, FS1 and FS0.
VRAM port formats are shown in Tables 4, 5 and 6. The FIFO register capacity is 16 word x 32 bit (for 32-, 24-, or 16-bit video data).
The I²C-bits LW1, LW0 can be used to define the position of the first pixel each line in the 32-bit-longword formats or to shift the UV sequence to VU in the 16-bit YUV formats.
In case of YUV output, an odd pixel count XD results in an incomplete pair of UV data at the end (LW = 0) or beginning (LW = 2) of a line.

Table 3 VMUX control

BIT VOF	PIN 53 VOEN	PIN 46 VMUX	VRAM BUS VRO(31-16)	VRO(15-0)
0	0	0	3-state	active
0	0	1	active	3-state
1	0	X	active	active
X	1	X	3-state	3-state

VRAM port inputs:
- VMUX, the VRAM output multiplexing signal
- VCLK to clock the FIFO register output data
- VOEN to enable output data.

VRAM port outputs:
- HFL flag (half-full flag)
- INCADR (refer to section "data burst transfer")
- the reference signals for pixel and line selection on outputs VRO(7-0) (only for 24- and 16-bit video data formats refer to "transparent data transfer").

VRAM port transfer procedures

Data transfer on the VRAM port can be done asynchroneously controlled by outputs HFL, INCADR and input VCLK (data burst transfer with bit TTR = 0).

Data transfer on the VRAM port can be done synchroneously controlled by output reference signals on outputs VRO(7-0) and a continuous VCLK of clock rate of LLC/2 (transparent data transfer with bit TTR = 1).

The scaling capability of the SAA7194 can be used in various applications.

Data burst transfer mode

Data transfer on the VRAM port is asynchroneously (TTR = 0). This mode can be used for all output formats. Four signals for communication with the external memory are provided.

- HFL flag, the half-full flag of the FIFO output register is raised when the FIFO contains at least 8 data words (HFL = HIGH). By setting HFL = 1, the SAA7194 requests a data burst transfer by the external memory controller, that has to start a transfer cycle within the next 32 LLC cycles for 32-bit longword modes (16 LLC cycles for 16- and 24-bit modes). If there are pixels in the FIFO at the end of a line, which are not transferred, the circuit fills up the FIFO register with "fill pixels" until it is half-full and sets the HFL flag to request a data burst transfer. After transfer is done, HFL is used in combination with INCADR to indicate the line increments (Fig.11).
- INCADR output signal is used in combination with HFL to control horizontal and vertical address generation for a memory controller. The pulse sequence depends on field formats (interlace/ non-interlace or odd/even fields, Figures 12 and 13) and control bits OF1 and OF0 (subaddress 20).

  HFL = 1 at the rising edge of INCADR:
  the END OF LINE is reached;
  request for line address increment
  HFL = 0 at the rising edge of INCADR:
  the END OF FIELD/FRAME is reached;
  request for line and pixel address reset
- VCLK input signal to clock the FIFO register output data VRO(n). New data are placed on the VRO(n) port with the rising edge of VCLK (Fig.9).
- VOEN input enables output data VRO(n).The outputs are in 3-state mode at VOEN = HIGH. VOEN changes only when VCLK is LOW. If VCLK pulses are applied during VOEN = HIGH, the outputs remain inactive, but the FIFO register accepts the pulses.

Transparent data transfer mode

Data transfer on the VRAM port can be achieved synchroneously (TTR =1) controlled by output reference signals on outputs VRO(7-0), and a contineous clock rate of LLC/2 on input VCLK. The SAA7194 delivers a contineously processed data stream. Therefore, the extended formats of the VRAM output port are selected (bit EFE = 1; Table 5).

The output signals VRO(7-0) have to be used to buffer qualified pre-processed RGB or YUV video data.
The YUV data are only valid in qualified time slots. Control output signals are (Table 5):

α	keying signal of the chroma keyer
O/E	odd/even field bit according to the internal field processing
VGT	vertical gate signal, "1" marks the scaling window in vertical direction from YO to (YO + YS) lines, cut by VS.
HGT	horizontal gate signal, "1" marks horizontal direction from XO to (XO + XS) lines, cut by HREF.
HRF	delay compensated horizontal reference signal.
LNQ	line qualifier signal, active polarity is defined by QPL bit.
PXQ	pixel qualifier signal, active polarity is defined by QPP bit.

Note: Interlaced processing (OF bits, subaddress 20):
To support correct interlaced data storage, the scaler delivers two INCADR/HFL sequences in each qualified line and an additional INCADR/HFL sequence after the vertical reset sequence at the beginning of an ODD field. Thereby, the scaled lines are automatically stored in the right sequence.

INCADR timing:
The distance from the last half-full request (HFL) to the INCADR pulse may be longer than 64 x LLC. The state of HFL is defined for minimum 4 x LLC in front of the rising slope of INCADR and for minimum 2 x LLC afterwards.

Monochrome format:

In case of TTR = 1 and EFE = 1 is Ya = Yb.

Table 4 VRAM port output data formats at EFE-bit = 0 and VOF-bit = 1 (settable via I^2C-bus), burst mode only

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB 5-5-5 + α 32-BIT WORDS			FS1 = 0; FS0 = 1 YUV 4:2:2 32-BIT WORDS			FS1 = 1; FS0 = 0 YUV 4:2:2 16-BIT WORDS			FS1 = 1; FS0 = 1 8-bit monochrome 32-BIT WORDS		
PIXEL ORDER	**n**	**n+2**	**n+4**	**n**	**n+2**	**n+4**	**n**	**n+1**	**n+2**	**n n+1**	**n+4 n+5**	**n+8 n+9**
VRO31	α	α	α	Ye7	Ye7	Ye7	Ye7	Yo7	Ye7	Ya7	Ya7	Ya7
VRO30	R4	R4	R4	Ye6	Ye6	Ye6	Ye6	Yo6	Ye6	Ya6	Ya6	Ya6
VRO29	R3	R3	R3	Ye5	Ye5	Ye5	Ye5	Yo5	Ye5	Ya5	Ya5	Ya5
VRO28	R2	R2	R2	Ye4	Ye4	Ye4	Ye4	Yo4	Ye4	Ya4	Ya4	Ya4
VRO27	R1	R1	R1	Ye3	Ye3	Ye3	Ye3	Yo3	Ye3	Ya3	Ya3	Ya3
VRO26	R0	R0	R0	Ye2	Ye2	Ye2	Ye2	Yo2	Ye2	Ya2	Ya2	Ya2
VRO25	G4	G4	G4	Ye1	Ye1	Ye1	Ye1	Yo1	Ye1	Ya1	Ya1	Ya1
VRO24	G3	G3	G3	Ye0	Ye0	Ye0	Ye0	Yo0	Ye0	Ya0	Ya0	Ya0
VRO23	G2	G2	G2	Ue7	Ue7	Ue7	Ue7	Ve7	Ue7	Yb7	Yb7	Yb7
VRO22	G1	G1	G1	Ue6	Ue6	Ue6	Ue6	Ve6	Ue6	Yb6	Yb6	Yb6
VRO21	G0	G0	G0	Ue5	Ue5	Ue5	Ue5	Ve5	Ue5	Yb5	Yb5	Yb5
VRO20	B4	B4	B4	Ue4	Ue4	Ue4	Ue4	Ve4	Ue4	Yb4	Yb4	Yb4
VRO19	B3	B3	B3	Ue3	Ue3	Ue3	Ue3	Ve3	Ue3	Yb3	Yb3	Yb3
VRO18	B2	B2	B2	Ue2	Ue2	Ue2	Ue2	Ve2	Ue2	Yb2	Yb2	Yb2
VRO17	B1	B1	B1	Ue1	Ue1	Ue1	Ue1	Ve1	Ue1	Yb1	Yb1	Yb1
VRO16	B0	B0	B0	Ue0	Ue0	Ue0	Ue0	Ve0	Ue0	Yb0	Yb0	Yb0
PIXEL ORDER	**n+1**	**n+3**	**n+5**	**n+1**	**n+3**	**n+5**	**OUTPUTS NOT USED**			**n+2 n+3**	**n+6 n+7**	**n+10 n+11**
VRO15	α	α	α	Yo7	Yo7	Yo7	X	X	X	Yc7	Yc7	Yc7
VRO14	R4	R4	R4	Yo6	Yo6	Yo6	X	X	X	Yc6	Yc6	Yc6
VRO13	R3	R3	R3	Yo5	Yo5	Yo5	X	X	X	Yc5	Yc5	Yc5
VRO12	R2	R2	R2	Yo4	Yo4	Yo4	X	X	X	Yc4	Yc4	Yc4
VRO11	R1	R1	R1	Yo3	Yo3	Yo3	X	X	X	Yc3	Yc3	Yc3
VRO10	R0	R0	R0	Yo2	Yo2	Yo2	X	X	X	Yc2	Yc2	Yc2
VRO9	G4	G4	G4	Yo1	Yo1	Yo1	X	X	X	Yc1	Yc1	Yc1
VRO8	G3	G3	G3	Yo0	Yo0	Yo0	X	X	X	Yc0	Yc0	Yc0
VRO7	G2	G2	G2	Ve7	Ve7	Ve7	X	X	X	Yd7	Yd7	Yd7
VRO6	G1	G1	G1	Ve6	Ve6	Ve6	X	X	X	Yd6	Yd6	Yd6
VRO5	G0	G0	G0	Ve5	Ve5	Ve5	X	X	X	Yd5	Yd5	Yd5
VRO4	B4	B4	B4	Ve4	Ve4	Ve4	X	X	X	Yd4	Yd4	Yd4
VRO3	B3	B3	B3	Ve3	Ve3	Ve3	X	X	X	Yd3	Yd3	Yd3
VRO2	B2	B2	B2	Ve2	Ve2	Ve2	X	X	X	Yd2	Yd2	Yd2
VRO1	B1	B1	B1	Ve1	Ve1	Ve1	X	X	X	Yd1	Yd1	Yd1
VRO0	B0	B0	B0	Ve0	Ve0	Ve0	X	X	X	Yd0	Yd0	Yd0

α = keying bit; R, G, B, Y, U and V = digital signals; e = even pixel number; o = odd pixel number;
a b c d = consecutive pixels

Table 5 VRAM port output data formats at EFE-bit = 1 and VOF-bit = 1 (settable via I^2C-bus), burst- and transparent- modes

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB 5-5-5 + α 16-BIT WORDS			FS1 = 0; FS0 = 1 YUV 4:2:2 16-BIT WORDS			FS1 = 1; FS0 = 0 RGB 8-8-8 24-BIT WORDS			FS1 = 1; FS0 = 1 8-bit monochrome 16-BIT WORDS		
PIXEL ORDER	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n n+1**	**n+2 n+3**	**n+4 n+5**
VRO31	α	α	α	Ye7	Yo7	Ye7	R7	R7	R7	Ya7	Ya7	Ya7
VRO30	R4	R4	R4	Ye6	Yo6	Ye6	R6	R6	R6	Ya6	Ya6	Ya6
VRO29	R3	R3	R3	Ye5	Yo5	Ye5	R5	R5	R5	Ya5	Ya5	Ya5
VRO28	R2	R2	R2	Ye4	Yo4	Ye4	R4	R4	R4	Ya4	Ya4	Ya4
VRO27	R1	R1	R1	Ye3	Yo3	Ye3	R3	R3	R3	Ya3	Ya3	Ya3
VRO26	R0	R0	R0	Ye2	Yo2	Ye2	R2	R2	R2	Ya2	Ya2	Ya2
VRO25	G4	G4	G4	Ye1	Yo1	Ye1	R1	R1	R1	Ya1	Ya1	Ya1
VRO24	G3	G3	G3	Ye0	Yo0	Ye0	R0	R0	R0	Ya0	Ya0	Ya0
VRO23	G2	G2	G2	Ue7	Ve7	Ue7	G7	G7	G7	Yb7	Yb7	Yb7
VRO22	G1	G1	G1	Ue6	Ve6	Ue6	G6	G6	G6	Yb6	Yb6	Yb6
VRO21	G0	G0	G0	Ue5	Ve5	Ue5	G5	G5	G5	Yb5	Yb5	Yb5
VRO20	B4	B4	B4	Ue4	Ve4	Ue4	G4	G4	G4	Yb4	Yb4	Yb4
VRO19	B3	B3	B3	Ue3	Ve3	Ue3	G3	G3	G3	Yb3	Yb3	Yb3
VRO18	B2	B2	B2	Ue2	Ve2	Ue2	G2	G2	G2	Yb2	Yb2	Yb2
VRO17	B1	B1	B1	Ue1	Ve1	Ue1	G1	G1	G1	Yb1	Yb1	Yb1
VRO16	B0	B0	B0	Ue0	Ve0	Ue0	G0	G0	G0	Yb0	Yb0	Yb0
PIXEL ORDER	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n n+1**	**n+2 n+3**	**n+4 n+5**
VRO15	X	X	X	X	X	X	B7	B7	B7	X	X	X
VRO14	X	X	X	X	X	X	B6	B6	B6	X	X	X
VRO13	X	X	X	X	X	X	B5	B5	B5	X	X	X
VRO12	X	X	X	X	X	X	B4	B4	B4	X	X	X
VRO11	X	X	X	X	X	X	B3	B3	B3	X	X	X
VRO10	X	X	X	X	X	X	B2	B2	B2	X	X	X
VRO9	X	X	X	X	X	X	B1	B1	B1	X	X	X
VRO8	X	X	X	X	X	X	B0	B0	B0	X	X	X
VRO7 (1)(2)	α	α	α	α	X	α	α	α	α	α	α	α
VRO6 (2)	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E
VRO5 (2)	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT
VRO4 (2)	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT
VRO3	X	X	X	X	X	X	X	X	X	X	X	X
VRO2 (2)	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF
VRO1 (2)	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ
VRO0 (2)	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ

α = keying bit; R, G, B, Y. U and V = digital signals; e = even pixel number; o = odd pixel number; a b = consecutive pixels; O/E = odd/even flag

(1) YUV 16-bit format: the keying signal α is defined only for YU time steps. The corresponding YV sample has also to be keyed. The α signal in monochrome mode can be used only in the transparent mode (TTR = 1), in this case Ya = Yb.

(2) Data valid only when transparent mode active (TTR-bit = 1) and VCLK pin connected to LLC/2 clock rate.

Table 6 VRAM port output data formats at EFE-bit = 0 and VOF-bit = 0 (settable via I²C-bus), burst mode only

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB 5-5-5 + α 32-BIT LONGWORD				FS1 = 0; FS0 = 1 YUV 4:2:2 32-BIT LONGWORD				FS1 = 1; FS0 = 1 8-bit monochrome 32-BIT LONGWORD			
PIXEL ORDER	n		n+2		n		n+2		n n+1		n+4 n+5	
VMUX	1	0	1	0	1	0	1	0	1	0	1	0
VRO31	α	Z	α	Z	Ye7	Z	Ye7	Z	Ya7	Z	Ya7	Z
VRO30	R4	Z	R4	Z	Ye6	Z	Ye6	Z	Ya6	Z	Ya6	Z
VRO29	R3	Z	R3	Z	Ye5	Z	Ye5	Z	Ya5	Z	Ya5	Z
VRO28	R2	Z	R2	Z	Ye4	Z	Ye4	Z	Ya4	Z	Ya4	Z
VRO27	R1	Z	R1	Z	Ye3	Z	Ye3	Z	Ya3	Z	Ya3	Z
VRO26	R0	Z	R0	Z	Ye2	Z	Ye2	Z	Ya2	Z	Ya2	Z
VRO25	G4	Z	G4	Z	Ye1	Z	Ye1	Z	Ya1	Z	Ya1	Z
VRO24	G3	Z	G3	Z	Ye0	Z	Ye0	Z	Ya0	Z	Ya0	Z
VRO23	G2	Z	G2	Z	Ue7	Z	Ue7	Z	Yb7	Z	Yb7	Z
VRO22	G1	Z	G1	Z	Ue6	Z	Ue6	Z	Yb6	Z	Yb6	Z
VRO21	G0	Z	G0	Z	Ue5	Z	Ue5	Z	Yb5	Z	Yb5	Z
VRO20	B4	Z	B4	Z	Ue4	Z	Ue4	Z	Yb4	Z	Yb4	Z
VRO19	B3	Z	B3	Z	Ue3	Z	Ue3	Z	Yb3	Z	Yb3	Z
VRO18	B2	Z	B2	Z	Ue2	Z	Ue2	Z	Yb2	Z	Yb2	Z
VRO17	B1	Z	B1	Z	Ue1	Z	Ue1	Z	Yb1	Z	Yb1	Z
VRO16	B0	Z	B0	Z	Ue0	Z	Ue0	Z	Yb0	Z	Yb0	Z
PIXEL ORDER		n+1		n+3		n+1		n+3		n+2 n+3		n+6 n+7
VMUX	1	0	1	0	1	0	1	0	1	0	1	0
VRO15	Z	α	Z	α	Z	Yo7	Z	Yo7	Z	Yc7	Z	Yc7
VRO14	Z	R4	Z	R4	Z	Yo6	Z	Yo6	Z	Yc6	Z	Yc6
VRO13	Z	R3	Z	R3	Z	Yo5	Z	Yo5	Z	Yc5	Z	Yc5
VRO12	Z	R2	Z	R2	Z	Yo4	Z	Yo4	Z	Yc4	Z	Yc4
VRO11	Z	R1	Z	R1	Z	Yo3	Z	Yo3	Z	Yc3	Z	Yc3
VRO10	Z	R0	Z	R0	Z	Yo2	Z	Yo2	Z	Yc2	Z	Yc2
VRO9	Z	G4	Z	G4	Z	Yo1	Z	Yo1	Z	Yc1	Z	Yc1
VRO8	Z	G3	Z	G3	Z	Yo0	Z	Yo0	Z	Yc0	Z	Yc0
VRO7	Z	G2	Z	G2	Z	Ve7	Z	Ve7	Z	Yd7	Z	Yd7
VRO6	Z	G1	Z	G1	Z	Ve6	Z	Ve6	Z	Yd6	Z	Yd6
VRO5	Z	G0	Z	G0	Z	Ve5	Z	Ve5	Z	Yd5	Z	Yd5
VRO4	Z	B4	Z	B4	Z	Ve4	Z	Ve4	Z	Yd4	Z	Yd4
VRO3	Z	B3	Z	B3	Z	Ve3	Z	Ve3	Z	Yd3	Z	Yd3
VRO2	Z	B2	Z	B2	Z	Ve2	Z	Ve2	Z	Yd2	Z	Yd2
VRO1	Z	B1	Z	B1	Z	Ve1	Z	Ve1	Z	Yd1	Z	Yd1
VRO0	Z	B0	Z	B0	Z	Ve0	Z	Ve0	Z	Yd0	Z	Yd0

α = keying bit; R, G, B, Y, U and V = digital signals; e = even pixel number; o = odd pixel number;
a b c d = consecutive pixels; Z = high-ohmic (3-state).

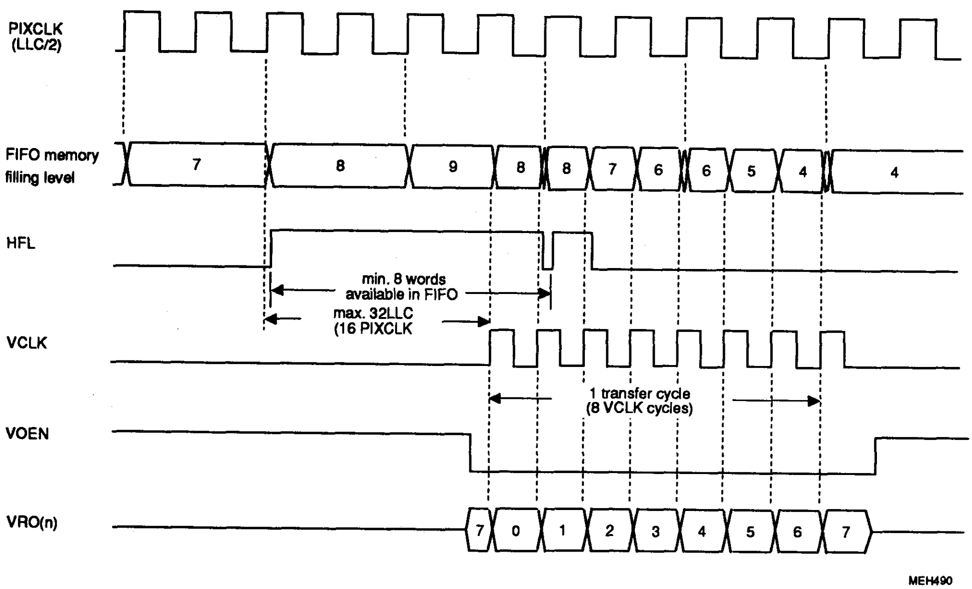


Fig.11 Output port transfer to VRAM at 32-bit data format without scaling. If VCLK cycles occur at VOEN = HIGH, the FIFO register is unchanged, but the outputs VRO(31-0) remain in 3-state position.

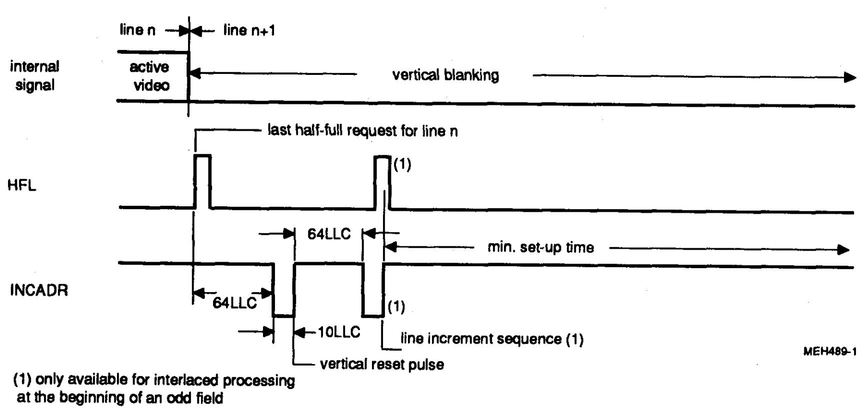


Fig.12 Vertical reset timing to the VRAM.

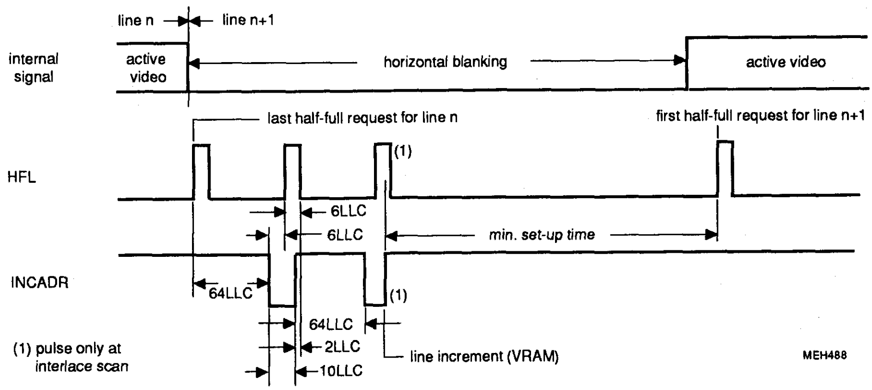


Fig.13 Horizontal increment timing to the VRAM.

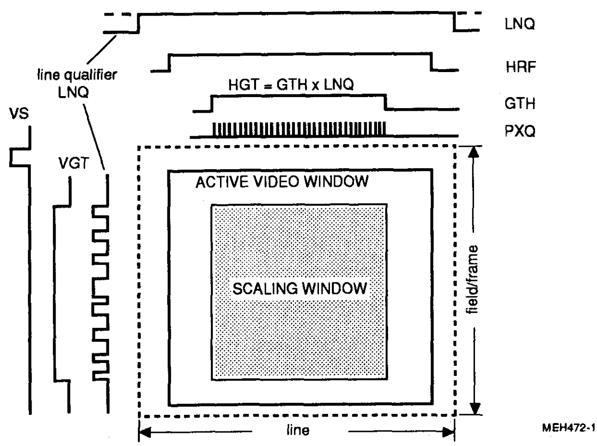


Fig.14 Reference signals for scaling window.

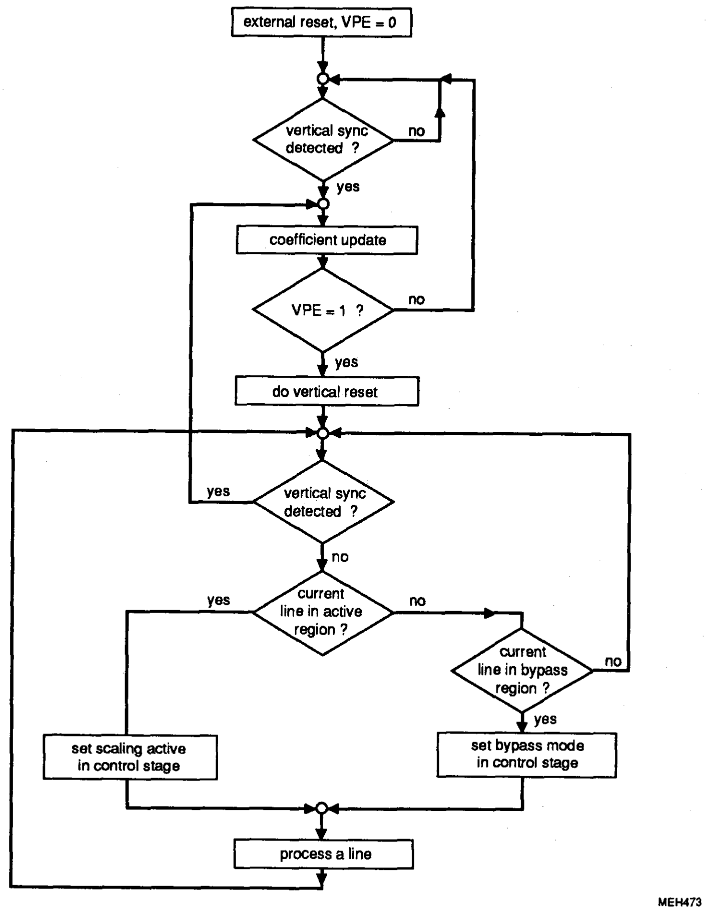


Fig.15 Operation cycle.

Field processing

The phase of the field sequence (odd/even dependent on inputs HREF and VS) is detected by means of the falling edge of VS. The current field phase is reported in the status byte by the OEF bit (Table 7). OEF bit can be stable 0 or 1 for non-interlaced input frames or non-standard input signals VS and/or HREF (nominal condition for VS and HREF – SAA7194 with active vertical noise limiter). A free-running odd/even flag is generated for internal field processing if the detection reports a stable OEF bit. The POE bit (subaddress 0B) can be used to change the polarity of the internal flag (in case of non-standard VS and HREF signals) to control the phase of the free-running flag, and to compensate mis-detections. Thus, the SAA7194 can be used under various VS/HREF timing conditions.

The SAA7194 operates on fields. To support progressive displays and to avoid movement blurring and artifacts, the circuit can process both or single fields of interlaced or non-interlaced input data. Therefore the OF bits can be used. The bits OF1 and OF0 (Table 10) determine the INCADR/HFL generation in "data burst transfer mode". One of the fields (odd or even) is ignored when OF1 = 1; then no line increment sequence (INCADR/HFL) is generated, the vertical reset pulse is only generated.

With OF1 = OF0 = 0 the circuit supports correct interlaced data storage (see note of previously described "transparent data transfer").

Operation cycle

The operation is synchronized by the input field. The cycle is specified in the flow chart (Fig.15).
The circuit is inactive after power-on reset, VPE is 0 and the FIFO control is set "empty". The internal control registers are updated with the falling edge of VS signal. The circuit is switched active and waits for a transmission of VS and a vertical reset sequence to the memory controller. Afterwards, the scaler waits for the beginning of a scaling or bypass region. If the active scaling region begins, while the bypass region is active, the bypass region is interrupted. If a vertical sync appears, the processing of the current line is finished. Then , the scaler performs a coefficient update and generates a new vertical reset (if it is still active).

Line processing starts when a line is decided to be active, the circuit starts to scale it. Active pixels are loaded into the FIFO register. An HFL flag is generated to initialize a data transfer when eight words are completed.
The end of a line is reached when the programmed pixel number is processed or when a horizontal sync pulse occurs. If there are pixels in the FIFO register, it is filled up until it is half-full to cause a data transfer. Horizontal increment pulses are transmitted after this data transfer.

Remarks:
The scaler part will always wait for the HREF/VS pulse before the line increment/vertical reset sequence is performed.
After each line/field, the FIFO control is set to empty when the increment/vertical reset pulses are transmitted. No additional actions are necessary if the memory controller has ignored the HFL signal. There is no need to handle over-/underflow of the FIFO register.

7.5. Power-on reset

- the bits VTRC and SSTB in subaddress "0Dh" are set to zero
- all bits in subaddress "0Eh" are set to zero
- the FIFO register contents are undefined
- outputs VRO, YUV, CREFB, LLCB, HREF, HS, and VS are set to 3-state
- output INCADR = HIGH
- output HFL = LOW until the VPE bit is set to "1"
- subaddress "30" is set to 00h and VPE-bit in subaddress "20h" is set to zero (Table 10).

8. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A	-------	DATAn	A	P

S	=	start condition
SLAVE ADDRESS	=	**0100 000X** (IICSA = LOW) **or 0100 001X** (IICSA = HIGH)
A	=	acknowledge, generated by the slave
SUBADDRESS*	=	subaddress byte (Tables 8 to 11)
DATA	=	data byte (Tables 8 to 11)
P	=	stop condition
X	=	read/write control bit X = 0, order to write (the circuit is slave receiver) X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 7 I²C-bus status byte (X in address byte = 1 ; 41h at IICSA = LOW or 43h at IICSA = HIGH).

FUNCTION	DATA D7	D6	D5	D4	D3	D2	D1	D0
status byte 0 (transmitted after RESN = 0 or at SSTB = 0)	ID3	ID2	ID1	ID0	DIR	X	OEF	SVP
status byte 1 (transmitted at SSTB = 1)	STTC	HLCK	FIDT	X	X	X	ALTD	CODE

Function of status bits:

ID3 to ID0 — Software model of SAA7194 compatible with

ID3	ID2	ID1	ID0	version
0	0	0	0	V0 (first version)

DIR — State of input DIR (pin 95): direction control of Expansion Port YUV
- DIR = 0 : the scaler uses internal source (decoder output)
- DIR = 1 : the scaler uses external data of expansion bus

OEF — Identification of field sequence dependent on HREF and VS:
0 = even field detected; 1 = odd field detected

SVP — State of VRAM port (state of, VPE-bit cleared by RESN):
- 0 = inputs HFL and INCADR inactive;
- 1 = inputs HFL and INCADR active.

STTC — Horizontal time constant information (for future application with logical comb-filter only):
0 = TV time constant (slow);
1 = VCR time constant (fast)

HLCK — Horizontal PLL information: 0 = HPLL locked; 1 = HPLL unlocked

FIDT — Field information: 0 = 50 Hz system detected; 1 = 60 Hz system detected

ALTD — Line alternation: 0 = no line alternating colour burst detected;
1 = line alternating colour burst detected (PAL or SECAM)

CODE — Colour information: 0 = no colour detected; 1 = colour detected

X — for future enhancements, do not evaluate

Table 8 I²C-bus decoder control; subaddress and data bytes for writing (X in address byte = 0 ; 40h at IICSA = LOW or 42h at IICSA = HIGH)

FUNCTION	SUBADDRESS	DATA								DF*
		D7	D6	D5	D4	D3	D2	D1	D0	
Increment delay	00	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0	
H-sync begin; 50 Hz	01	HSYB7	HSYB6	HSYB5	HSYB4	HSYB3	HSYB2	HSYB1	HSYB0	
H-sync stop; 50 Hz	02	HSYS7	HSYS6	HSYS5	HSYS4	HSYS3	HSYS2	HSYS1	HSYS0	
H-clamp begin; 50 Hz	03	HCLB7	HCLB6	HCLB5	HCLB4	HCLB3	HCLB2	HCLB1	HCLB0	
H-clamp stop; 50 Hz	04	HCLS7	HCLS6	HCLS5	HCLS4	HCLS3	HCLS2	HCLS1	HCLS0	
H-sync after PHI1; 50 Hz	05	HPHI7	HPHI6	HPHI5	HPHI4	HPHI3	HPHI2	HPHI1	HPHI0	
Luminance control	06	BYPS	PREF	BPSS1	BPSS0	CORI1	CORI0	APER1	APER0	
Hue control	07	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0	
Colour-killer QUAM	08	CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0	0	0	0	
Colour-killer SECAM	09	CKTS4	CKTS3	CKTS2	CKTS1	CKTS0	0	0	0	
PAL switch sensitivity	0A	PLSE7	PLSE6	PLSE5	PLSE4	PLSE3	PLSE2	PLSE1	PLSE0	
SECAM switch sensitivity	0B	SESE7	SESE6	SESE5	SESE4	SESE3	SESE2	SESE1	SESE0	
Chroma gain control	0C	COLO	LFIS1	LFIS0	0	0	0	0	0	
Standard/mode control	0D	VTRC	0	0	0	RTSE	HRMV	SSTB	SECS	
I/O and clock control	0E	HPLL	0	OECL	OEHV	OEYC	CHRS	GPSW2	GPSW1	
Control #1	0F	AUFD	FSEL	SXCR	SCEN	0	YDEL2	YDEL1	YDEL0	
Control #2	10	0	0	0	0	0	HRFS	VNOI1	VNOI0	
Chroma gain reference	11	CHCV7	CHCV6	CHCV5	CHCV4	CHCV3	CHCV2	CHCV1	CHCV0	
Chroma saturation	12	0	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0	
Luminance contrast	13	0	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0	
H-sync begin; 60 Hz	14	HS6B7	HS6B6	HS6B5	HS6B4	HS6B3	HS6B2	HS6B1	HS6B0	
H-sync stop; 60 Hz	15	HS6S7	HS6S6	HS6S5	HS6S4	HS6S3	HS6S2	HS6S1	HS6S0	
H-clamp begin; 60 Hz	16	HC6B7	HC6B6	HC6B5	HC6B4	HC6B3	HC6B2	HC6B1	HC6B0	
H-clamp stop; 60 Hz	17	HC6S7	HC6S6	HC6S5	HC6S4	HC6S3	HC6S2	HC6S1	HC6S0	
H-sync after PHI1; 60 Hz	18	HP6I7	HP6I6	HP6I5	HP6I4	HP6I3	HP6I2	HP6I1	HP6I0	
Luminance brightness	19	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0	
Reserved	1A to 1F	0	0	0	0	0	0	0	0	

*) Default register contents fill in by hand

Table 9 Function of the register bits of Table 8 for subaddresses "00" to "19"

IDEL7 to IDEL0 "00"	Increment delay time (dependent on application), step size = 4 / LLC. The delay time is selectable from –4 / LLC (–1 decimal multiplier) to –1024 / LLC (–256 decimal multiplier) equals data FF to 00 (hex). A sign-bit, designated A08 and internally set HIGH, indicates always negative values. The maximum delay time in 60 Hz systems is –780 equally to 3D (hex); the maximum delay time in 50 Hz systems is –944 equally to 14 (hex) Different processing times in the chrominance channel and the clock generation could result in phase errors in the chrominance processing by transients in clock frequency. An adjustable delay (IDEL) is necessary if the processing time in the clock generation is unknown. (The horizontal PLL does not operate if the maximum delays are exeeded. The system clock frequency is set to a value of the last update and is within ±7.1 % of nominal frequency).
HSYB7 to HSYB0 "01"	Horizontal sync begin for 50 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two´s complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.
HSYS7 to HSYS0 "02"	Horizontal sync stop for 50 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two´s complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.
HCLB7 to HCLB0 "03"	Horizontal clamp start for 50 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HCLS7 to HCLS0 "04"	Horizontal clamp stop for 50 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HPHI7 to HPHI0 "05"	Horizontal sync start after PHI1 for 50 Hz, step size = 8 / LLC. The delay time is selectable from –32 to +31.7 µs (+118 to –118 decimal multiplier), equals data 75 to 8A (hex) Forbidden, outside available central counter range, are +127 to +118 decimal multiplier, equals data 7E to 76 (hex) as well as –119 to –128 decimal multiplier, equals data 89 to 80 (hex)
BYPS "06"	input mode select bit: 0 = CVBS mode (chrominance trap active) 1 = S-Video mode (chrominance trap bypassed)
PREF	use of pre-filter: 0 = pre-filter off (bypassed); 1 = pre-filter on; PREF may be used if chrominance trap is active.
BPSS1 to BPSS0	Aperture bandpass to select different characteristics with maximums (0.2 to 0.3 x LLC / 2): (see table below)

BPSS1	BPSS0	characteristics
0	0	)
0	1	) Figures 17 to 26
1	0	)
1	1	)

CORI1 to CORI0 "05"	Coring range for high frequency components according to 8-bit luminance, Fig.16. CORI1 CORI0 | coring 0 0 | coring off 0 1 | ±1 LSB of 8-bit 1 0 | ±2 LSB of 8-bit 1 1 | ±3 LSB of 8-bit
APER1 to APER0 "06"	Aperture bandpass filter weights high frequency components of luminance signal: APER1 APER0 | factor 0 0 | 0) 0 1 | 0.25) 1 0 | 0.5) 1 1 | 1) Figures 17 to 26
HUE7 to HUE0 "07"	Hue control from +178.6° to −180.0°, equals data bytes 7F to 80 (hex); 0° equals 00.
CKTQ4 to CKTQ0 "08"	Colour-killer threshold QAM (PAL, NTSC) from approximately −30 dB to −18 dB, equals data bytes F8 to 07 (hex)
CKTS4 to CKTS0 "09"	Colour-killer threshold SECAM from approximately −30 dB to −18 dB, equals data bytes. F8 to 07 (hex)
PLSE7 to PLSE0 "0A"	PAL switch sensitivity from LOW to HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.
SESE7 to SESE0 "0B"	SECAM switch sensitivity from LOW to HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.
COLO "0C"	Colour-on bit: 0 = automatic colour-killer; 1 = forced colour-on.
LFIS1 to LFIS0	Automatic gain control (AGC filter): LFIS1 LFIS0 | loop filter time constant 0 0 = | slow 0 1 = | medium 1 0 = | fast 1 1 = | actual gain stored (for test purposes only)
VTRC "0D"	VTR/TV mode bit : 0 = TV mode; 1 = VTR mode.
RTSE	Realtime output mode select bit: 0 = PLIN switched to output RTS1 (pin 34); ODD switched to RTS0 (pin 35) 1 = HL switched to output RTS1 (pin 34); VL switched to RTS0 (pin 35)
HRMV	HREF position select: 0 = default; 1 = HREF is 8 x LLC2 clocks earlier
SSTB	Status byte select: 0 = status byte 0 selected; 1 = status byte 1 selected
SECS	SECAM mode bit : 0 = other standards; 1 = SECAM

HPLL "0E"	Horizontal clock PLL: 0 = PLL closed; 1 = PLL open and horizontal frequency fixed.
OECL	Select internal/external clock source: 0 = LLCB and CREFB are inputs; 1 = LLCB and CREFB are outputs
OEHV	Output enable of horizontal/vertical sync: 0 = HS, HREF and VS pins are inputs (outputs high-impedance) 1 = HS, HREF and VS pins are outputs
OEYC	Data output YUV(15-0) enable: 0 = data pins are inputs; 1 = data pins are controlled by DIR (pin 95)
CHRS	S-VHS bit (chrominance from CVBS or from chrominance input): 0 = controlled by BYPS-bit (subaddress 06) 1 = chrominance from chrominance input (CHR(7-0))
GPSW2 to GPSW1	General purpose switches: GPSW2 GPSW1 — set port output pins 32 (GPSW2) and 33 (GPSW1) 0 0 0 1 1 0 1 1 use is dependent on application
AUFD "0F"	Automatic field detection: 0 = field selection by FSEL-bit; 1 = automatic field detection by SAA7194.
FSEL	Field select (AUFD-bit = 0): 0 = 50 Hz (625 lines); 1 = 60 Hz (525 lines)
SXCR	SECAM cross-colour reduction: 0 = reduction off; 1 = reduction on.
SCEN	Enable sync and clamping pulse: 0 = HSY and HCL outputs HIGH (pins 25 and 26) 1 = HSY and HCL outputs active
YDEL2 to YDEL0	Luminance delay compensation: (see table below)
HRFS "10"	Select HREF position: 0 = normal, HREF is matched to YUV output on Expansion Port 1 = HREF is matched to CVBS input port

General purpose switches (GPSW2 to GPSW1):

GPSW2	GPSW1	set port output pins 32 (GPSW2) and 33 (GPSW1)
0	0	use is dependent on application
0	1	
1	0	
1	1	

Luminance delay compensation (YDEL2 to YDEL0):

YDEL2	YDEL1	YDEL0	delay	
0	0	0	0 x 2 / LLC	
0	0	1	+1 x 2 / LLC	
0	1	0	+2 x 2 / LLC	step size = 2 / LLC =
0	1	1	+3 x 2 / LLC	67.8 ns for 50 Hz
1	0	0	–4 x 2 / LLC	81.5 ns for 60 Hz
1	0	1	–3 x 2 / LLC	
1	1	0	–2 x 2 / LLC	
1	1	1	–1 x 2 / LLC	

<table>
<tr><td>VNOI1 to VNOI0</td><td>Vertical noise reduction
<table>
<tr><th>VNOI1</th><th>VNOI0</th><th>mode</th></tr>
<tr><td>0</td><td>0</td><td>normal</td></tr>
<tr><td>0</td><td>1</td><td>searching window</td></tr>
<tr><td>1</td><td>0</td><td>free-running mode</td></tr>
<tr><td>1</td><td>1</td><td>vertical noise reduction bypassed</td></tr>
</table></td></tr>
<tr><td>CHCV7 to CHCV0
"11"</td><td>Chrominance gain control (nominal values) for QAM-modulated input signals, effects UV output amplitude (SECAM with fixed gain):
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>gain</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>maximum gain</td></tr>
<tr><td></td><td>:</td><td></td><td></td><td></td><td>:</td><td></td><td></td><td>to)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>CCIR level for PAL) default programmed</td></tr>
<tr><td></td><td>:</td><td></td><td></td><td></td><td>:</td><td></td><td></td><td>to) values dependend on</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>CCIR level for NTSC) application</td></tr>
<tr><td></td><td>:</td><td></td><td></td><td></td><td>:</td><td></td><td></td><td>to)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>minimum gain</td></tr>
</table></td></tr>
<tr><td>SATN6 to SATN0
"12"</td><td>Chrominance suturation control for for VRAM port:
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>gain</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1.999 (maximum saturation)</td></tr>
<tr><td></td><td>:</td><td></td><td></td><td></td><td>:</td><td></td><td></td><td>to</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 (CCIR level)</td></tr>
<tr><td></td><td>:</td><td></td><td></td><td></td><td>:</td><td></td><td></td><td>to</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0 (colour off)</td></tr>
</table></td></tr>
<tr><td>CONT6 to CONT0
"13"</td><td>Luminance contrast control for VRAM port:
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>gain</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1.999 (maximum contrast)</td></tr>
<tr><td></td><td>:</td><td></td><td></td><td></td><td>:</td><td></td><td></td><td>to</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 (CCIR level)</td></tr>
<tr><td></td><td>:</td><td></td><td></td><td></td><td>:</td><td></td><td></td><td>to</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0 (luminance off)</td></tr>
</table></td></tr>
<tr><td>HS6B7 to HS6B0
"14"</td><td>Horizontal sync begin for 60 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two´s complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.</td></tr>
<tr><td>HS6S7 to HS6S0
"15"</td><td>Horizontal sync stop for 60 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two´s complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.</td></tr>
<tr><td>HC6B7 to HC6B0
"16"</td><td>Horizontal clamp begin for 60 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).</td></tr>
</table>

HC6S7 to HC6S0 "17"	Horizontal clamp stop for 60 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HP6I7 to HP6I0 "18"	Horizontal sync start after PHI1 for 60 Hz, step size = 8 / LLC. The delay time is selectable from –32 to +31.7 µs (+97 to –97 decimal multiplier), equals data 61 to 9F (hex) Forbidden, outside available central counter range, are +127 to +98 decimal multiplier, equals data 7E to 62 (hex) as well as –98 to –128 decimal multiplier, equals data 9E to 80 (hex)
BRIG7 to BRIG0 "19"	Luminance brightness control for VRAM port:

D7	D6	D5	D4	D3	D2	D1	D0	gain
1	1	1	1	1	1	1	1	255 (bright)
	:				:			to
1	0	0	0	0	0	0	0	128 (CCIR level)
	:				:			to
0	0	0	0	0	0	0	0	0 (dark)

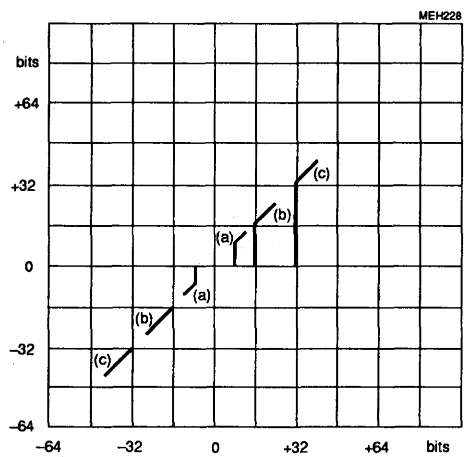


Fig.16 Coring function adjustment by subaddress 06 to affect the bandfilter output signal. The thresholds are related to the 13-bit word width in the luminance processing part and influence the 1LSB to 3LSB (Y0 to Y2) with respect to the 8-bit luminance output

(a) CORI1 = 0; CORI0 = 1

(b) CORI1 = 1; CORI0 = 0

(a) CORI1 = 1; CORI0 = 1

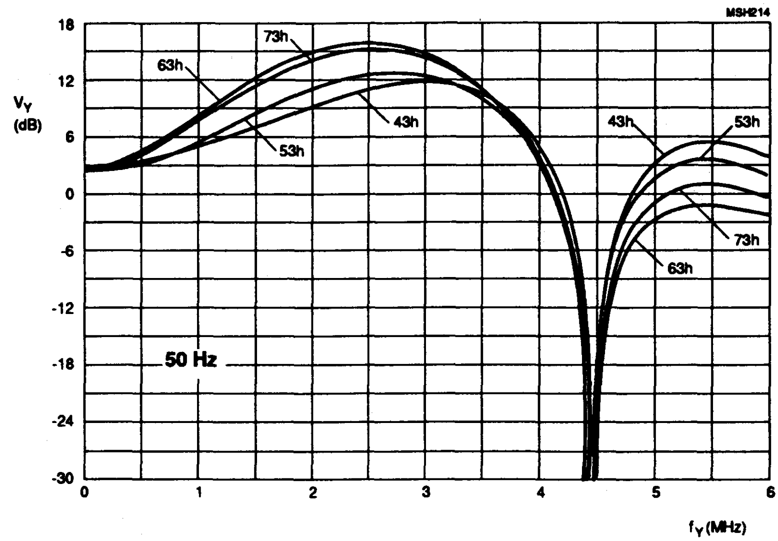


Fig.17 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; maximum aperture bandpass filter characteristic.

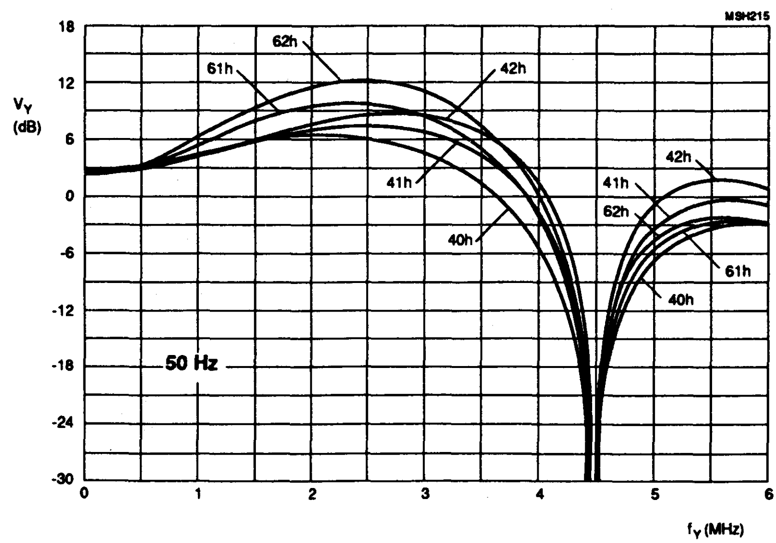


Fig.18 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; other aperture bandpass filter characteristics.

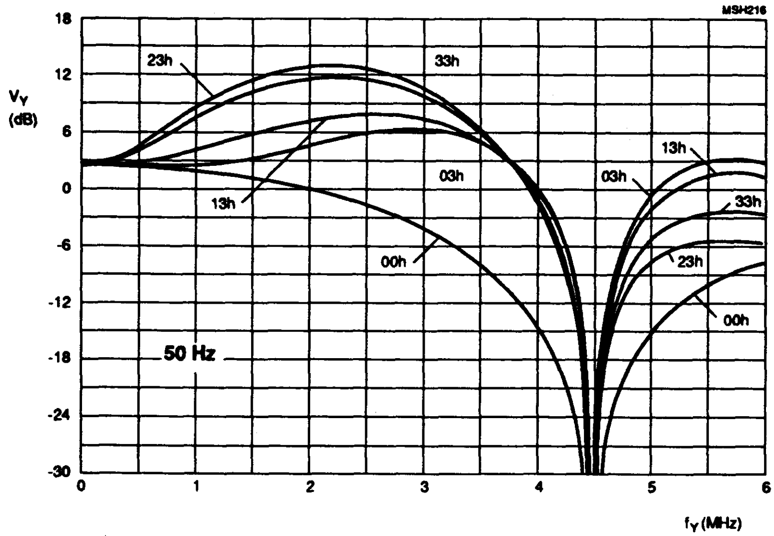


Fig.19 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter off and coring off; maximum aperture bandpass filter characteristic.

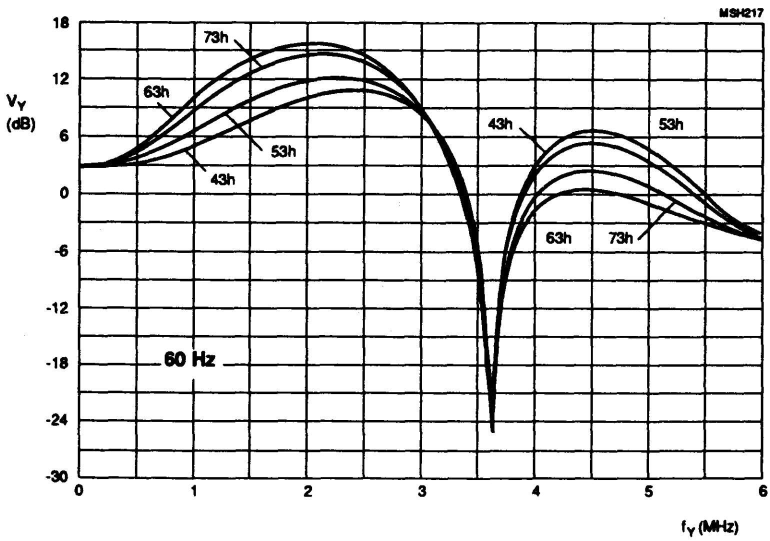


Fig.20 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; maximum aperture bandpass filter characteristic.

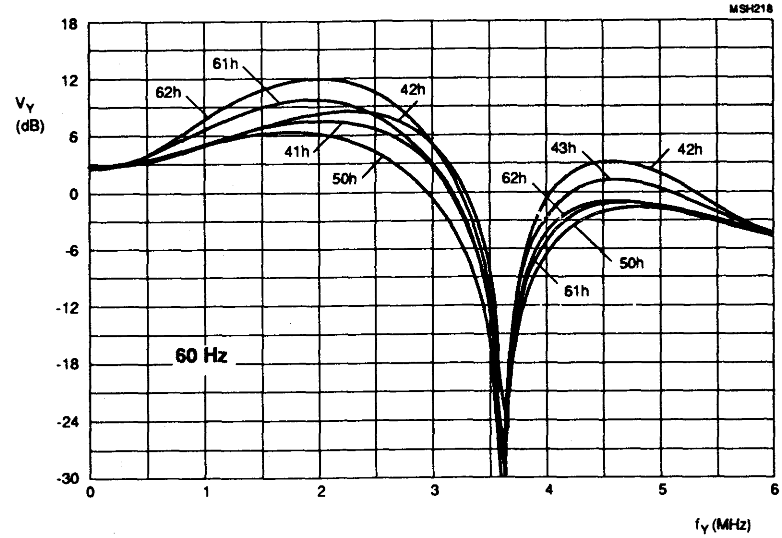


Fig.21 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; other aperture bandpass filter characteristics.

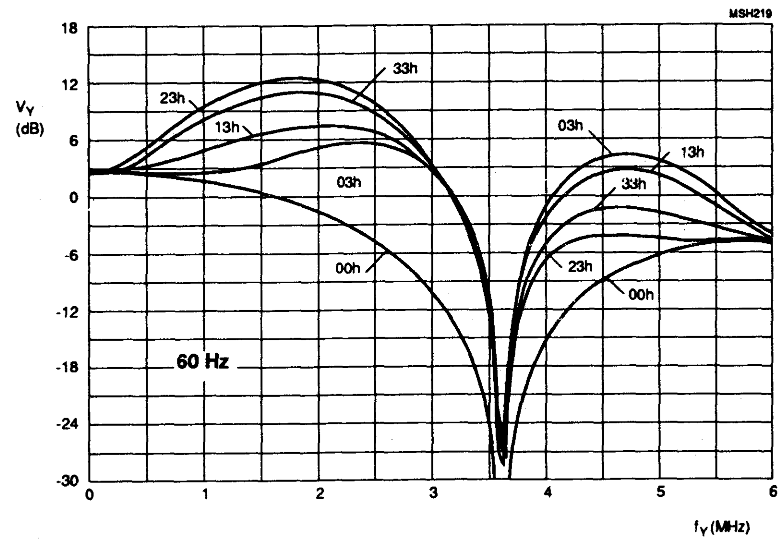


Fig.22 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter off and coring off; maximum and minimum aperture bandpass filter characteristics.

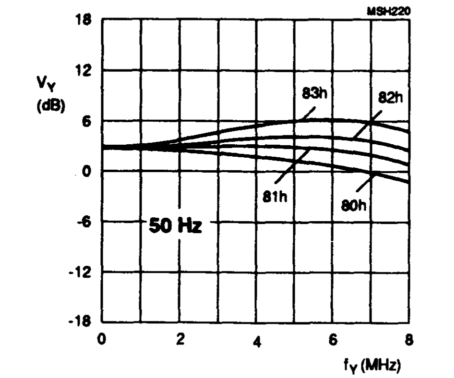


Fig.23 Luminance control in 50 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter off and coring off; different aperture bandpass filter characteristics.

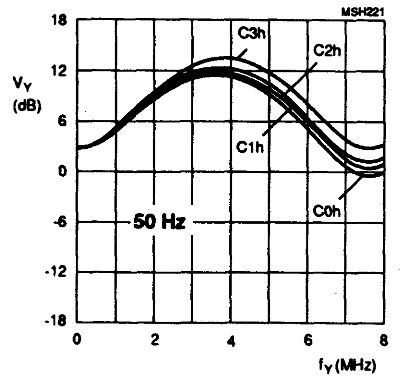


Fig.24 Luminance control in 50 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter on and coring off; different aperture bandpass filter characteristics.

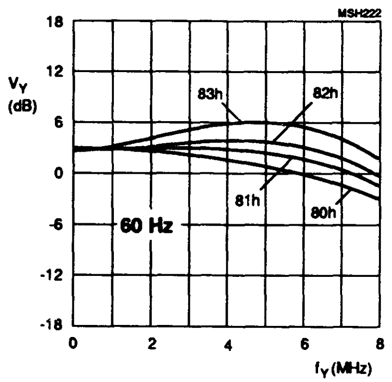


Fig.25 Luminance control in 60 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter off and coring off; different aperture bandpass ffilter characteristics.

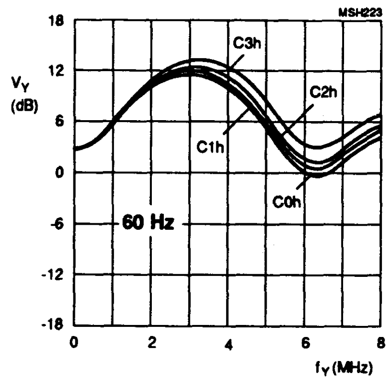


Fig.26 Luminance control in 60 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter on and coring off; different aperture bandpass filter characteristics.

Table 10 I²C-bus scaler control; subaddress and data bytes for writing

FUNCTION	SUBADDRESS	DATA D7	D6	D5	D4	D3	D2	D1	D0	DF*
Formats and sequence	20	RTB	OF1	OF0	VPE	LW1	LW0	FS1	FS0	
Output data pixel/line (1)	21	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0	
Input data pixel/line (1)	22	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
Horiz. window start (1)	23	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0	
Horizontal filter	24	HF2	HF1	HF0	XO8	XS9	XS8	XD9	XD8	
Output data lines/field (2)	25	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0	
Input data lines/field (2)	26	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
Vertical window start (2)	27	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0	
AFS/vertical Y processing	28	AFS	VP1	VP0	YO8	YS9	YS8	YD9	YD8	
Vertical bypass start (3)	29	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0	
Vertical bypass count (3)	2A	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	
	2B	0	0	0	VS8	0	VC8	0	POE	
Chroma keying										
lower limit for V	2C	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	
upper limit for V	2D	VU7	VU6	VU5	VU4	VU3	VU2	VU1	VU0	
lower limit for U	2E	UL7	UL6	UL5	UL4	UL3	UL2	UL1	UL0	
upper limit for U	2F	UU7	UU6	UU5	UU4	UU3	UU2	UU1	UU0	
Data path setting**	30	VOF	AFG	LLV	MCT	QPL	QPP	TTR	EFE	
Unused	31 to 3F									

(1) continued in "24"; (2) continued in "28"; (3) continued in "2B";
*) Default register contents fill in by hand. **) Data representation, transfer mode and adaptivity

Table 11 Function of the register bits of Table 10 for subaddresses "20" to "30"

RTB "20"	ROM table bypass switch: 0 = anti-gamma ROM active; 1 = table is bypassed
OF1 to OF0	Set output field mode: OF1 / OF0 / field mode DVS process 0 / 0 / both fields for interlaced storage 0 / 1 / both fields for non-interlaced storage 1 / 0 / odd fields only (even fields ignored) for non-interlaced storage 1 / 1 / even fields only(odd fields ignored) for non-interlaced storage
VPE	VRAM port outputs enable: 0 = HFL and INCADR inactive (HFL = LOW, INCADR = HIGH); VRO outputs in 3-state 1 = HFL and INCADR enabled; VRO outputs dependent on VOEN

LW1 to LW0	First pixel position in VRO data for FS1 = 0; FS0 = 0 (RGB) and FS1 = 0; FS0 = 1(YUV): LW1 LWO | 31 to 24 | 23 to 16 | 15 to 8 | 7 to 0 0 0 | pixel 0 | pixel 0 | pixel 1 | pixel 1) 0 1 | pixel 0 | pixel 0 | pixel 1 | pixel 1) EFE = 0; TTR = 0 1 0 | black | black | pixel 0 | pixel 0) 1 1 | black | black | pixel 0 | pixel 0) First pixel position in VRO data for FS1 = 1; FS0 = 1 (monochrome): LW1 LWO | 31 to 24 | 23 to 16 | 15 to 8 | 7 to 0 0 0 | pixel 0 | pixel 1 | pixel 2 | pixel 3) 0 1 | black | pixel 0 | pixel 1 | pixel 2) EFE = 0; TTR = 0 1 0 | black | black | pixel 0 | pixel 1) 1 1 | black | black | black | pixel 0) 0 0 | pixel 0 | pixel 1 | X | X) 0 1 | black | pixel 0 | X | X) EFE = 1; TTR = 0; LW only effects the greyscale format 1 0 | pixel 0 | pixel 1 | X | X) 1 1 | black | pixel 0 | X | X)
FS1 to FS0	FIFO output register format select (EFE- bit see "30"): EFE FS1 FS0 | output format (Tables 2 and 3) 0 0 0 | RGB 5-5-5 + alpa; 2x16-bit/pixel; 32-bit word length; RGB matrix on, VRAM output format 0 0 1 | YUV 4:2:2; 2x16-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format 0 1 0 | YUV 4:2:2; 1x16-bit/pixel;16-bit word length; RGB matrix off, optional output format 0 1 1 | monochrome mode; 4x8-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format 1 0 0 | RGB 5-5-5 + alpa; 1x16-bit/pixel; 16-bit word length; RGB matrix on, VRAM output + transparent format 1 0 1 | YUV 4:2:2 + alpa; 1x16-bit/pixel; 16-bit word length; RGB matrix off, VRAM output + transparent format 1 1 0 | RGB 8-8-8 + alpa; 1x24-bit/pixel; 24-bit word length; RGB matrix on, VRAM output + transparent format 1 1 1 | monochrome mode; 2x8-bit/pixel; 16-bit word length; RGB matrix off, VRAM output + transparent format
XD9 to XD0 "21 and 24"	Pixel number per line (straight binary) on output (VRO): 00 0000 0000 to 11 1111 1111 (number of XS pixels as a maximum; take care of vertical processing)
XS9 to XS0 "22 and 24"	Pixel number per line (straight binary) on inputs (YIN and UVIN): 00 0000 0000 to 11 1111 1111 (number of input pixels per line as a maximum; take care of vertical processing)
XO8 to XO0 "23 and 24"	Horizontal start position (straight binary) of scaling window (take care of active pixel number per line). start with 1st pixel after HREF rise = 0 0000 0011 to 1 1111 1111 (003 to 1FF) window start and window end may be cut by internal delay compensated HREF = 0 phase. XO has to be matched to the internal processing delay.

HF2 to HF0 "24"	Horizontal decimation filter HF2 HF1 HF0 | taps | filter (Figures 27 and 28) 0 0 0 | 2 | filter 1 0 0 1 | 3 | filter 2 0 1 0 | 5 | filter 3 0 1 1 | 9 | filter 4 1 0 0 | 1 | filter bypassed 1 0 1 | 1 | filter bypassed + delay in Y channel of 1T 1 1 0 | 8 | filter 5 1 1 1 | 4 | filter 6 The filter coefficients are related to the luminance path. The filter coefficient may differ from upper table when a combination with vertical Y processing and adaptive modes are provided.
YD9 to YD0 "25 and 28"	Line number per output field (straight binary): 00 0000 0000 to 11 1111 1111 (number of YS lines as a maximum)
YS9 to YS0 "26 and 28"	Line number per input field (straight binary): 00 0000 0000 0 line 11 1111 1111 1023 lines (maximum = number of lines/field – 3) Maximum input field size (VS = VC = AS = 0) in DMSD-SQP 60 Hz system is 259 (01 0000 0011) in DMSD-SQP 50 Hz system is 309 (01 0011 0101)
YO8 to YO0 "27 and 28"	Vertical start of scaling window. Take care of active line number per field (straight binary); window start and cut may be cut by the external VS signal: 0 0000 0000 start with 3rd line after the rising slope of VS 0 0000 0011 start with 1st line after the falling slope of nominal VS (7151B, 7191B input) 1 1111 1111 511 + 3 lines after the rising slope of VS (maximum value)
AFS "28"	Adaptive filter switch: 0 = off; use VP1, VP0 and HF2 to HF0 bits 1 = on; filter characteristics are selected by the scaler
VP1 to VP0	Vertical luminance data processing VP1 VP0 | processing (approximate equations) 0 0 | bypassed 0 1 | delay of one line $H(z) = z^{-H}$ 1 0 | vertical filter 1: $(H(z) = 1/2\ (1 + z^{-H}))$ 1 1 | vertical filter 2: $(H(z) = 1/4\ (1 + 2z^{-H} + z^{-2H}))$
VS8 to VS0 "29 and 2B"	Vertical bypass start, sets begin of the bypass region (straight binary). Scaling region overrides bypass region (YO bits): 0 0000 0000 start with 3rd line after the rising slope of VS 0 0000 0011 start with 1st line after the falling slope of nominal VS (7151B, 7191B input) 1 1111 1111 511 + 3 lines after the rising slope of VS (maximum value)
VC8 to VC0 "2A and 2B"	Vertical bypass count, sets length of bypass region (straight binary): 0 0000 0000 0 line length 1 1111 1111 511 lines length (maximum = number of lines/field – 3)
POE	Polarity, internally detected odd/even flag O/E: 0 = flag unchanged; 1 = flag inverted
VL7 to VL0 "2C"	Set lower limit V for colour-keying (8 bit; two's complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level

VU7 to VU0 "2D"	Set upper limit V for colour-keying (8 bit; two's complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
UL7 to UL0 "2E"	Set lower limit U for colour-keying (8 bit; two's complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
UU7 to UU0 "2F"	Set upper limit U for colour-keying (8 bit; two's complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
VOF "30"	Set VRAM bus output format: 0 = enabling of 32 to 16 bit multiplexing via VMUX (pin 46) 1 = disabling of 32 to 16 bit multiplexing via VMUX (pin 46)
AFG	Adaptive geometrical filter: 0 = linear H and V data processing; 1 = approximated geometrical H and V interpolation (improved scaling accuracy of luminance)
LLV	Luminance limiting value: 0 = amplitude range between 1 and 254; 1 = amplitude range between 16 and 235, suitable for monochrome and YUV modes
MCT	Monochrome and two's complement output data select: 0 = inverse grayscale luminance (if grayscale is selected by FS bits) or straight binary U, V data output 1 = non-inverse monochrome luminance (if grayscale is selected by FS bits) or two'complement U, V data output
QPL	Line qualifier polarity flag : 0 = LNQ is active-LOW (pin 52); 1 = LNQ is active-HIGH
QPP	Pixel qualifier polarity flag : 0 = PXQ is active-LOW (pin 51); 1 = PXQ is active-HIGH
TTR	Transparent data transfer: 0 = normal operation (VRAM data burst transfer) 1 = FIFO register transparent
EFE	Extended formats enable bit (see FS-bits in subaddress "20"): 0 = 32-bit longword output formats; 1 = extended output formats ("one pixel a time")

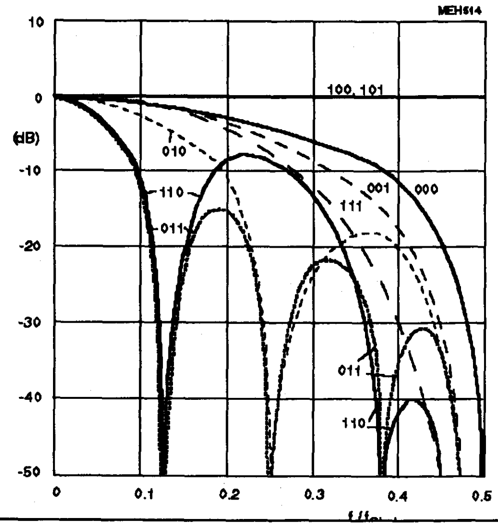


Fig.27 Horizontal frequency characteristic of luminance signal (Y) dependent on HF2 to HF0 bits (subaddress 24).

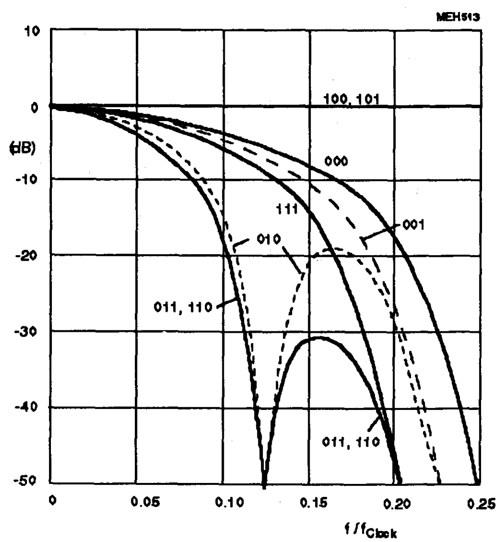


Fig.28 Horizontal frequency characteristic of chrominance signals (UV) without UV interpolation dependent on HF2 to HF0 bits (subaddress 24).

9. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 14, 27, 31, 45, 61, 77, 91 and 106)	−0.5	6.5	V
V_I	voltage on all input/output pins	−0.5	V_{DD}+0.5	V
P_{tot}	total power dissipation	-	1.2	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±2000	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10. CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage range (pins 14, 31, 45, 61, 77, 91 and 106)		4.5	5	5.5	V
V_{DDA}	analog supply voltage range (pin 27)		4.5	5	5.5	V
I_{DDD}	digital supply current	inputs LOW; outputs without load	-	150	220	mA
I_{DDA}	analog supply current		-	20	30	mA
Data clock and control inputs						
V_{IL}	input voltage LOW	LLC, LLCB	−0.5	-	0.6	V
V_{IH}	input voltage HIGH	LLC, LLCB	2.4	-	V_{DD}+0.5	V
V_{IL}	input voltage LOW	other inputs	−0.5	-	0.8	V
V_{IH}	input voltage HIGH	other inputs	2.0	-	V_{DD}+0.5	V
I_{LI}	input leakage current	V_{IL} = 0	-	-	10	µA
C_I	input capacitance data		-	-	8	pF
	input capacitance clocks		-	-	10	pF
	input capacitance 3-state I/O	high-impedance state	-	-	8	pF
Data and control outputs		note 1				
V_{OL}	output voltage LOW		0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
LFCO output (pin 28)						
V_o	LFCO output signal (peak-to-peak value)		1.4	2.1	2.6	V
V_{28}	output voltage range		1	-	V_{DD}	V
I²C-bus, SDA and SCL (pins 3 and 4)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3	-	V_{DD}+0.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{3,4}$	input current		-	-	±10	µA
I_{ACK}	output current on pin 3	acknowledge	3	-	-	mA
V_{OL}	output voltage at acknowledge	I_3 = 3 mA	-	-	0.4	V
Clock input timing (LLC and LLCB)		Fig.32				
t_{LLC}, t_{LLCB}	cycle time		31	-	45	ns
δ	duty factor	$t_{LLC\,H}$ / t_{LLC}	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
Data, Control, CREF and CREFB input timing		Fig.32; note 2				
t_{SU}	set-up time		11	-	-	ns
t_{HD}	hold time		3	-	-	ns
Data and control output timing		Fig.32; note 3				
C_L	load capacitance	data, HREF and VS	15	-	50	pF
		control	7.5	-	25	pF
t_{OH}	output hold time	C_L = 15 pF	13	-	-	ns
t_{PD}	propagation delay from negative edge of LLCB	data, HREF and VS; C_L = 50 pF	-		29	ns
		control; C_L = 25 pF	-		29	ns
t_{PZ}	propagation delay from negative edge of LLCB (to 3-state)	note 4	-		15	ns
Clock output timing (LLCB)		Fig.32				
C_L	output load capacitance		15	-	40	pF
t_{LLCB}	cycle time		31	-	45	ns
δ	duty factor	$t_{LLCB\,H}$ / t_{LLCB}	40	50	60	%
t_r	rise time	0.6 to 2.6 V	-	-	5	ns
t_f	fall time	2.6 to 0.6 V	-	-	5	ns
$t_{d\,LLCB}$	delay between LLC and LLCB		-	-	20	ns
Data qualifier output timing (CREFB)		Fig.32				
t_{OH}	output hold time	C_L = 15 pF	4	-	-	ns
t_{PD}	propagation delay from negative edge of LLCB	C_L = 40 pF	-	-	20	ns
Horizontal PLL						
$f_{H\,n}$	nominal line frequency	50 Hz system	-	15625	-	Hz
		60 Hz system	-	15734	-	Hz
Δf_H / $f_{H\,n}$	permissible static deviation	50 Hz system	-	-	±5.6	%
		60 Hz system	-	-	±6.7	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Subcarrier PLL						
$f_{SC\,n}$	nominal subcarrier frequency	PAL	-	4.433618	-	MHz
		NTSC	-	3.579545	-	MHz
Δf_{SC}	lock-in range	PAL, NTSC	±400	-	-	Hz
Crystal oscillator		note 11, Fig.32				
f_n	nominal frequency	3rd harmonic	-	26.8	-	MHz
$\Delta f / f_n$	permissible deviation f_n		-	-	±50	10^{-6}
	temperature deviation from f_n		-	-	±20	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	-	70	°C
	load capacitance C_L		8	-	-	pF
	series resonance resistance R_S		-	50	80	Ω
	motional capacitance C_1		-	1.1±20%	-	fF
	parallel capacitance C_0		-	3.5±20%	-	pF
	Philips catalogue number		9922 520 30004			
VCLK timing (pin 56)		Fig.31				
t_{VCLK}	VRAM port clock cycle time	note 5	50	-	200	ns
$t_{p\,L}$, $t_{p\,H}$	LOW and HIGH times	note 6	17	-	-	ns
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
VRO and reference signal output timing		Fig.31				
C_L	output load capacitance	VRO outputs	15	-	40	pF
		other outputs	7.5	-	25	pF
t_{OH}	VRO data hold time	C_L = 10 pF; note 7	0	-	-	ns
t_{OHL}	related to LCC (INCADR, HFL)	C_L = 10 pF; note 8	0		-	ns
t_{OHV}	related to VCLK (HFL)	C_L = 10 pF; note 8	0		-	ns
t_{OD}	VRO data delay time	C_L = 40 pF; note 7	-	-	25	ns
t_{ODL}	related to LCC (INCADR, HFL)	C_L = 25 pF; note 8	-	-	60	ns
t_{ODV}	related to VCLK (HFL)	C_L = 25 pF; note 8	-	-	60	ns
t_D	VRO disable time to 3-state	C_L = 40 pF; note 9	-	-	40	ns
		C_L = 25 pF; note 10	-	-	24	ns
t_E	VRO enable time from 3-state	C_L = 40 pF; note 9	-	-	40	ns
		C_L = 25 pF; note 10	-	-	25	ns
Response times to HFL flag						
$t_{HFL\,VOE}$	HFL set to VRAM port enable		-	tbd	-	ns
$t_{HFL\,VCLK}$	HFL set to VCLK burst		-	tbd	-	ns

Notes to the characteristics

1. Levels measured with load circuits dependent on output type. Control outputs (HREF, VS excluded): 1.2 kΩ at 3 V (TTL load) and C_L = 25 pF. Data, HREF and VS outputs: 1.2 kΩ at 3 V (TTL load) and C_L = 50 pF.
2. Data input signals are CVBS(7-0), CHR(7-0) and YUV(15-0). Control input signals are HREF, VS and DIR.
3. Data outputs are YUV(15-0). Control outputs are HREF, VS, HS, HSY, HCL, SODD, SVS, SHREF, PXQ, LNQ, RTCO and RTS(1-0). The calculation of t_{HD}, t_{DH}, t_{OH} and $t_{p\,D}$ includes t_r and t_f.
4. The minimum propagation delay from 3-state to data active is 0 related to the falling edge of LLCB.
5. Maximum t_{VCLK} = 200 ns for test mode only. The applicable maximum cycle time depends on data format, horizontal scaling and input data rate.
6. Measured at 1,5 V level; $t_{p\,L}$ may be unfinite.
7. Timings of VRO refer to the rising edge of VLCK.
8. The timing of INCADR refers to LLCB; the rising edge of HFL always refers to LLCB. During a VRAM transfer, the falling edge of HFL is generated by VCLK. Both edges of HFL refer to LLCB during horizontal increment and vertical reset cycles.
9. Asynchronous signals. Its timing refers to the 1.5 V switching point of VOEN input signal (pin 50).
10. The timing refers to the 1.5 V switching point of VMUX signal (pin 46) in 32- to 16-bit multiplexing mode. Corresponding pairs of VNO outputs are together connected.
11. If the internal oscillator is not being used, the applied clock signal must be TTL-compatible.

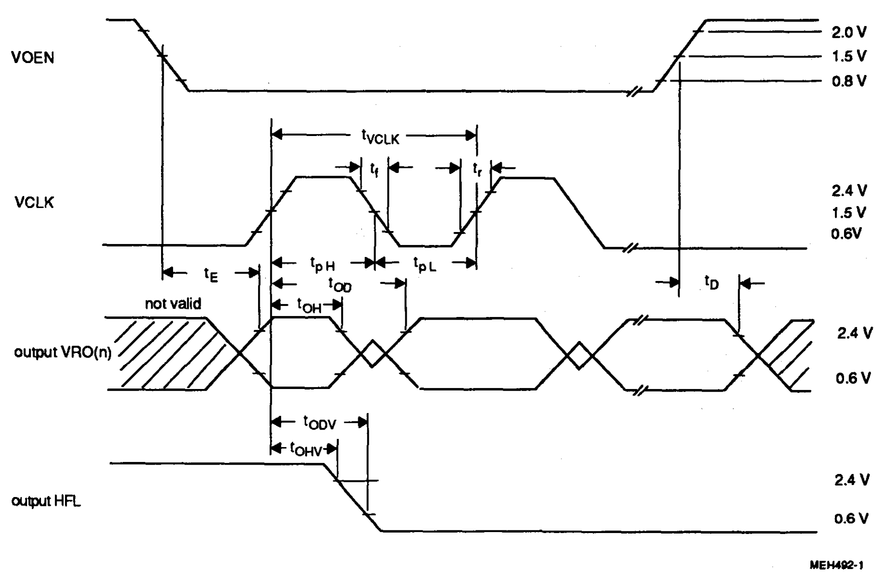


Fig.31 Data output timing (VCLK).

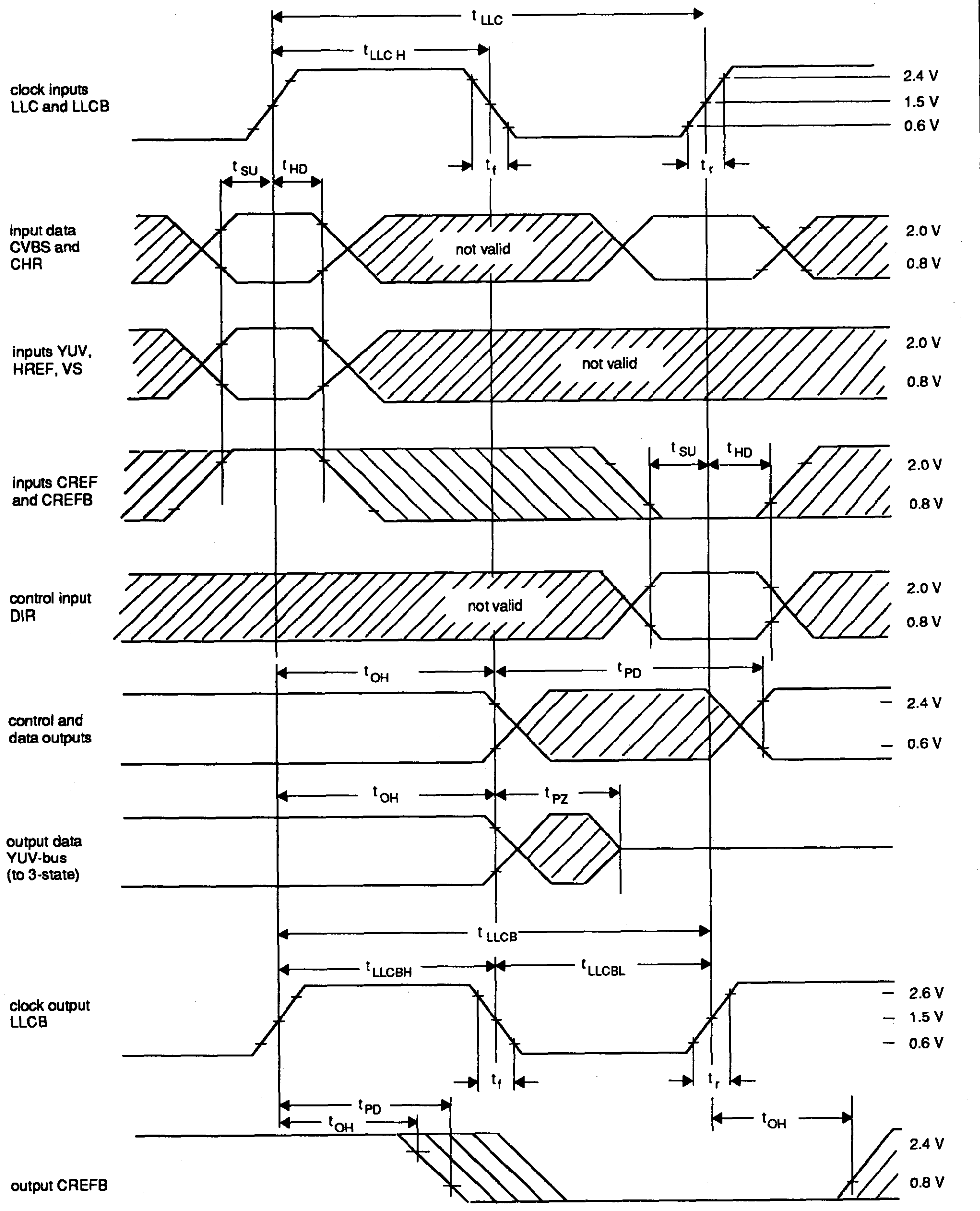


Fig.28 Data input/output timing by LLC and LLCB.

11. PROCESSING DELAYS

Table 12 Processing delays of signals

PORTS	DELAY IN LLC/LLCB CYCLES	REMARKS
CVBS/CHR to YUV	216	-
YUV to VRO	56 in YUV mode; 58 in RGB mode	only in transparent mode
CVBS/CHR to VRO	272 in YUV mode; 274 in RGB modes	only in transparent mode

12.1. APPLICATION INFORMATION

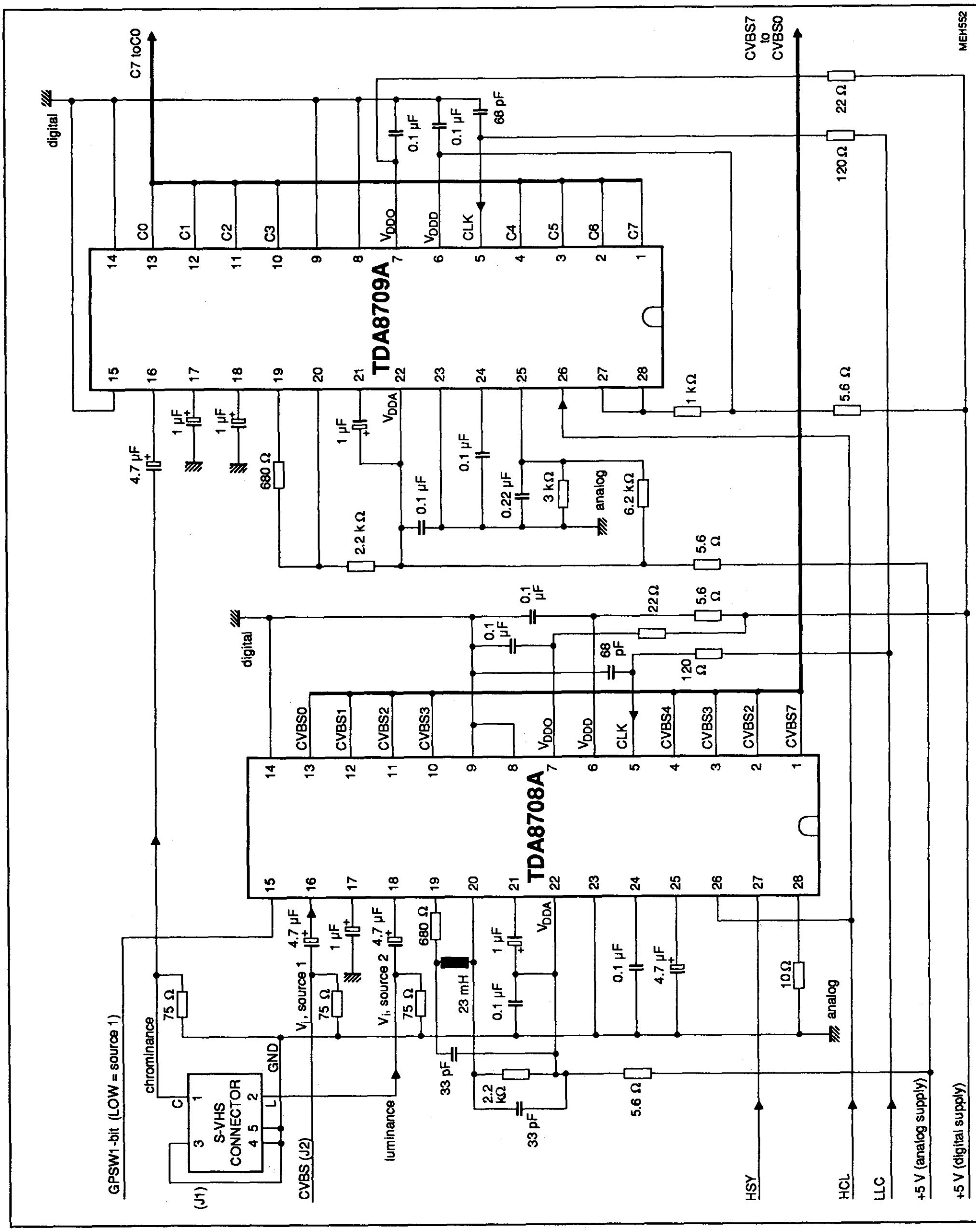


Fig. 29 Application circuit analog-to-digital convertions.

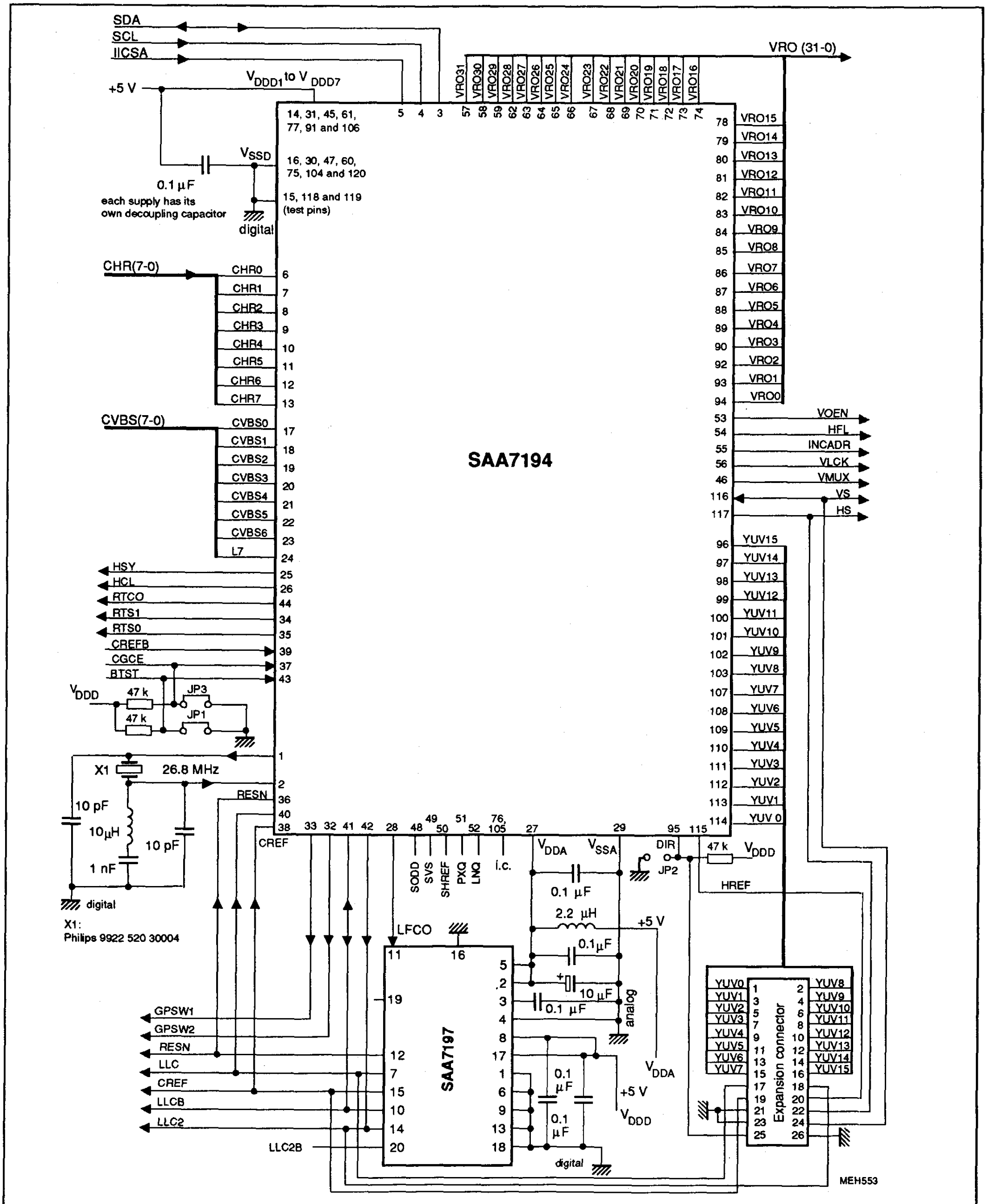


Fig.30 Application of SAA7194.

12.1. PROGRAMMING EXAMPLE

Coefficients to set operation for application circuits Figures 29 and 30. Slave address byte is 40 h at pin 5 connected to V_{SSD} (or 42h at pin 5 connected to V_{DDD}).

Table 13 Programming examples

SUBADDRESS	BITS	FUNCTION	VALUE (hex)
00	IDEL(7:0)	increment delay	4C
01	HSYB(7:0)	H-sync beginning for 50 Hz	30
02	HSYS(7:0)	H-sync stop for 50 Hz	00
03	HCLB(7:0)	H-clamp beginning for 50 Hz	E8
04	HCLS(7:0)	H-clamp stop for 50 Hz	B6
05	HPHI(7:0)	HS pulse position for 50 Hz	F4
06	BYPS, PREF, BPSS(1:0), CORI(1:0), APER(1:0)	luminance bandwidth control	01 (1)
07	HUEC(7:0)	hue control (0 degree)	00
08	CKTQ(4:0)	colour-killer threshold QUAM	F8
09	CKTS(4:0)	colour-killer threshold SECAM	F8
0A	PLSE(7:0)	PAL-switch sensivity	40
0B	SESE(7:0)	SECAM-switch sensivity	40
0C	COLO, LFIS(1:0)	chrominance gain control settings	00
0D	VTRC, RTSE, HRMV, SSTB, SECS	standard/mode control	04 (2) (4); 05 (3) (4)
0E	HPLL, OECL, OEHV, OEYC, CHRS, GPSW(2:1)	I/O and clock controls	38, 3B (5)
0F	AUFD, FSEL, SXCR, SCEN, YDEL(2:0)	miscellaneous controls #1	90
10	HRFS, VNOI(1:0)	miscellaneous controls #2	00
11	CHCV(7:0)	chrominance gain nominal value	2C (6); 59 (7)
12	SATN(6:0)	chrominance saturation control value	40
13	CONT(6:0)	luminance contrast control value	40
14	HS6B(7:0)	H-sync beginning for 60 Hz	34
15	HS6S(7:0)	H-sync stop for 60 Hz	0A
16	HC6B(7:0)	H-clamp beginning for 60 Hz	F4
17	HC6S(7:0)	H-clamp stop for 60 Hz	CE
18	HP6I(7:0)	HS pulse position for 60 Hz	F4
19	BRIG(7:0)	luminance brightness control value	80
1A to 1F	reserved	set to zero	00
20	RTB, OF(1:0), VPE, LW(1:0), FS(1:0),	data formats and field sequence processing	10 (8)
21	XD(7:0)	LSB's output pixel/line	80 (9); FF (13)
22	XS(7:0)	LSB's input pixel/line	80 (9); FF (13)
23	XO(7:0)	LSB's for horizontal window start position	03 (9); 00 (13)
24	HF(2:0), XO(8), XS(9, 8), XD(9, 8)	horizontal filter select and MSB's of subaddresses 21, 22, 23	85 (9); 8F (13)

SUBADDRESS	BITS	FUNCTION	VALUE (hex)
25	YD(7:0)	LSB's output lines/field	90 (9); FF (13)
26	YS(7:0)	LSB's input lines/field	90 (9); FF (13)
27	YO(7:0)	LSB's vertical window start position	03 (9); 00 (13)
28	AFS, VP(1:0), YO(8), YS(9, 8), YD(9, 8)	adaptive and vertical filter select and MSB's of subaddresses 25, 26, 27	00 (9); 0F (13)
29	VS(7:0)	LSB's vertical bypass start position	00 (10)
2A	VC(7:0)	LSB's vertical bypass lines/field	00 (10)
2B	VS(8), VC(8), POE	MSB's of subaddresses 29, 2A and odd/even polarity switch	00 (10)
2C	VL(7:0)	chroma key: lower limit V (R-Y)	00
2D	VU(7:0)	chroma key: upper limit V (R-Y)	FF (11)
2E	UL(7:0)	chroma key: lower limit U (B-Y)	00
2F	UU(7:0)	chroma key: upper limit U (B-Y)	00
30	VOF, AFG	VRAM port MUX enable, adaptivity	80 (12)

Notes to Table 13

1. dependent on application (Figures 29 and 30)
2. for QUAM standards
3. for SECAM
4. HPLL is in TV-mode, value for VCR-mode is 84h (85h for SECAM VCR-mode)
5. for Y/C-mode
6. nominal value for UV-CCIR-level with NTSC source
7. nominal value for UV-CCIR-level with PAL source
8. ROM-table is active, scaler process both fields for interlaced display; VRAM port enabled; longword position = 0; 16-bit 4:2:2 YUV output format selected.
9. scaler processes a segment of (384 pixels x 144 lines) with defaults XO and YO set to the first valid pixel/line and line/field (for decoder as input source) with scaler factors of 1:1; horizontal and vertical filters are bypassed, filter select adaptivity is disabled.
10. no vertical bypass region is defined
11. chrominance keyer is disabled (VL = 0; VU = –1)
12. 32-bit to 16 VRAM port MUX, adaptive scale and Y-limiter are disabled; pixel and line qualifier polarity for transparent mode are set to zero (active); data burst transfer for the 32-bit longword formats is set.
13. if no scaling and no panning is wanted, the parameters XD, XS, YD and YS should be set to maximum (3FFh) and the parameters XO and YO should be set to minimum (000h). In this case, the HREF and VS signals define the processing window of the scaler.

Digital video decoder, scaler and clock generator circuit (DESCPro)

SAA7196

FEATURES

- Digital 8-bit luminance input video (Y) or CVBS
- Digital 8-bit chrominance input (CVBS or C from CVBS, Y/C, S-Video (S-VHS or Hi8))
- Luminance and chrominance signal processing for main standards PAL, NTSC and SECAM
- Horizontal and vertical sync detection for all standards
- User programmable luminance peaking for aperture correction
- Compatible with memory-based features (line-locked clock, square pixel)
- Cross-colour reduction by chrominance comb filtering for NTSC or special cross-colour cancellation for SECAM
- UV signal delay lines for PAL to correct chrominance phase errors
- Square-pixel format with 768/640 active samples per line
- The bidirectional Expansion Port (YUV-bus) supports data rates of 780 x f_H (NTSC) and 944 x f_H (PAL, SECAM) in 4:2:2 format
- Brightness, contrast, hue and saturation controls for scaled outputs
- Down-scaling of video windows with 1023 active samples per line and 1023 active lines per frame to randomly sized windows
- 2 D data processing for improved signal quality of scaled luminance data, especially for compression applications
- Chroma key (α-generation)
- YUV to RGB conversation including Anti-gamma ROM tables for RGB
- 16-word output FIFO (32-bit words)•Output configurable for 32/24/16-bit video data bus
- Scaled 16-bit 4:2:2 YUV output
- Scaled 15-bit RGB (5-5-5+α) and 24-bit (8-8-8+α) output
- Scaled 8-bit monochrome output
- Line increment, field sequence (odd/even, interlace/non-interlace), and vertical reset control for easy memory interfacing
- Output of discontinuous data bursts of scaled video data or continuous data output with corresponding qualifier signals
- Real-time status information
- I^{2}C-bus control
- Only one crystal of 26.8 MHz
- Clock generator on chip

Digital video decoder, scaler and clock generator circuit (DESCPro)

SAA7196

GENERAL DESCRIPTION

The CMOS circuit SAA7196, digital video decoder and scaler (DESC), is a highly integrated circuit for DeskTop Video applications. It combines the functions of a digital multistandard decoder (SAA7191B), a digital video scaler (SAA7186) and a clock generator (SAA7197).

The decoder is based on the principle of line-locked clock decoding. It runs at square-pixel frequencies to achieve correct aspect ratio.

Monitor controls are provided to ensure best display.

Four data ports are supported:

Ports CVBS(7-0) and CHR(7-0) of the input interface are used in Y/C mode (Fig.1(a)) to decode digitized luminance and chrominance signals (digitized in two external ADCs).

In normal mode, the CVBS(7-0) input is only used, and only one ADC is necessary (Fig.3).

The 32-bit VRAM output port is interface to the video memory; it outputs the down-scaled video data. Different formats and operation modes are supported by this circuit.

The circuit is I^2C-bus-controlled; its I^2C-bus interface is clocked by LLC to ensure proper control.

The I^2C-bus control is identical to that of SAA7194. It is divided into two sections:

- subaddress 00h to 1F for the decoder part (Tables 8 and 9)
- subaddress 20h to 3F for the scaler part (Tables 10 and 11)

  The programming of the subaddresses for the scaler part becomes effective at the first vertical sync pulse VS after a transmission.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5	5.5	V
$I_{DD\ tot}$	total supply current	-	170	250	mA
V_I	data input level	TTL-compatible			
V_O	data output level	TTL-compatible			
LLC	clock frequency	-	-	32	MHz
T_{amb}	operating ambient temperature range	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7196	120	QFP	plastic	SOT349 AA1

BLOCK DIAGRAM

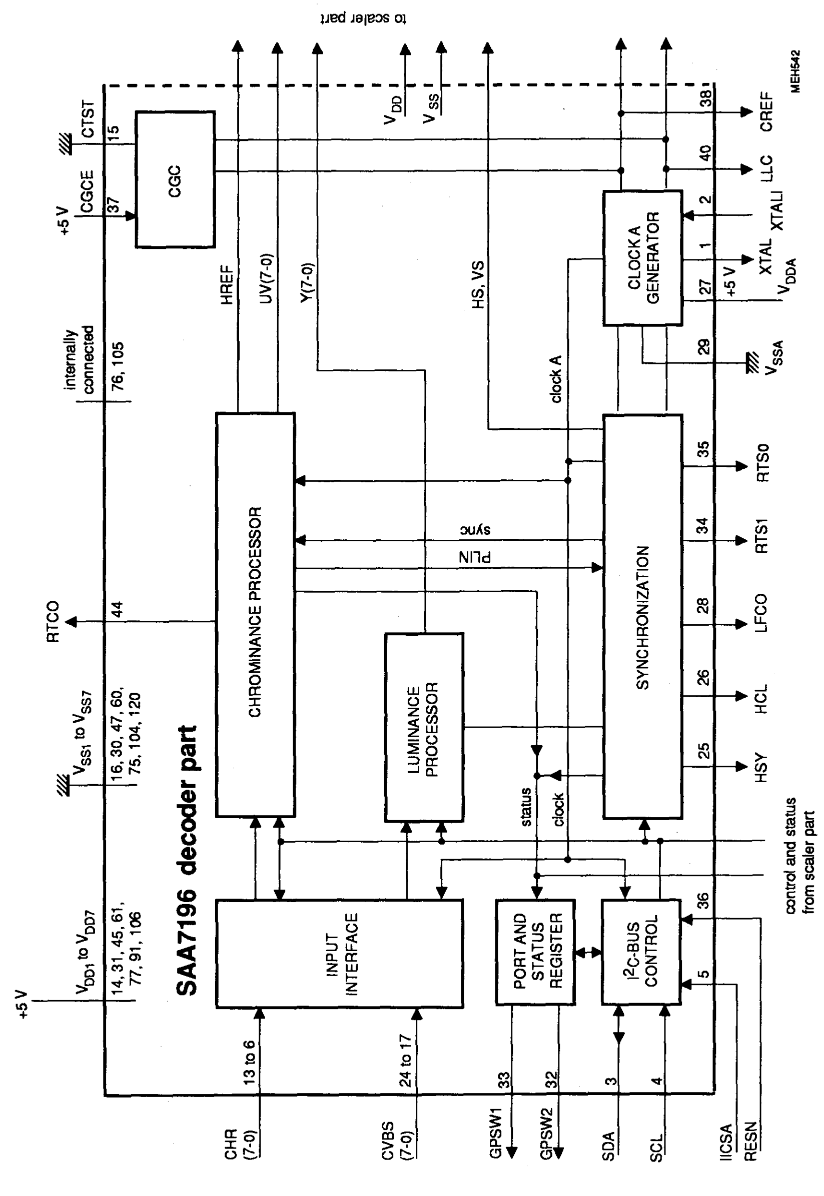


Fig.1(a) Block diagram of decoder part; (continued in Fig.1(b)).

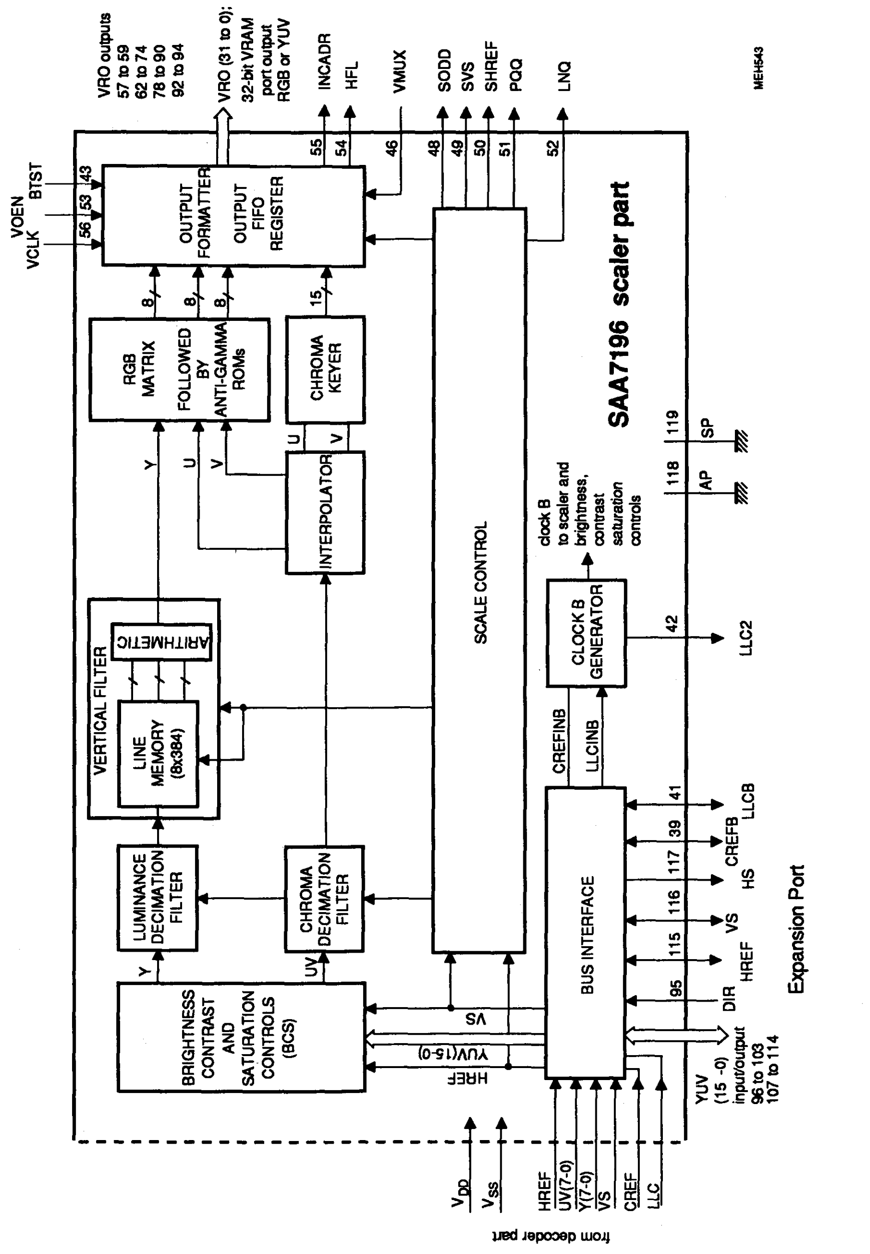


Fig.1(b) Block diagram of brightness, contrast, saturation controls and scaler part; (continued from Fig.1(a)).

PINNING

SYMBOL	PIN	STATUS	DESCRIPTION
XTAL	1	O	26.8 MHz crystal oscillator output, not used if TTL clock signal is used
XTALI	2	I	26.8 MHz crystal oscillator input, or external clock input (TTL, squarewave)
SDA	3	I/O	I^2C-bus data line
SCL	4	I	I^2C-bus clock line
IICSA	5	I	I^2C-bus set address
CHR0	6	I	digital chrominance input signal (bits 0 to 7)
CHR1	7	I	
CHR2	8	I	
CHR3	9	I	
CHR4	10	I	
CHR5	11	I	
CHR6	12	I	
CHR7	13	I	
V_{DD1}	14	-	+5 V supply voltage 1
CTST	15	-	connected to ground; CTST = HIGH for CGC test in future enhancements
V_{SS1}	16	-	GND1 (0 V)
CVBS0	17	I	digital CVBS input signal (bits 0 to 7)
CVBS1	18	I	
CVBS2	19	I	
CVBS3	20	I	
CVBS4	21	I	
CVBS5	22	I	
CVBS6	23	I	
CVBS7	24	I	
HSY	25	O	horizontal sync indicator output (programmable)
HCL	26	O	horizontal clamping pulse output (programmable)
V_{DDA}	27	-	+5 V analog supply voltage
LFCO	28	O	line frequency control output signal to CGC (multiple of present line frequency)
V_{SSA}	29	-	analog ground (0 V)
V_{SS2}	30	-	GND2 (0 V)

SYMBOL	PIN	STATUS	DESCRIPTION
V_{DD2}	31	-	+5 V supply voltage 2
GPSW2	32	O	general purpose output 2 (settable via I²C-bus)
GPSW1	33	O	general purpose output 1 (settable via I²C-bus)
RTS1	34	O	real time status output 1 controlled by RTSE-bit
RTS0	35	O	real time status output 0 controlled by RTSE-bit
RESN	36	I	reset input (active-LOW for at least 30 clock cycles LLC)
CGCE	37	I	enable input for internal CGC (connected to +5 V)
CREF	38	O	clock qualifier output
CREFB	39	I/O	clock reference qualifier input/output (HIGH indicates valid input data YUV(15-0))
LLC	40	O	line-locked video system clock output (maximum 32 MHz)
LLCB	41	I/O	line-locked clock signal input/output, maximum 32 MHz (twice of pixel rate in 4:2:2 format)
LLC2	42	O	line-locked clock signal output (pixel clock)
BTST	43	I	connected to ground; BTST = HIGH sets all outputs (except pins 1 and 28) and to to high-impedance state (testing)
RTCO	44	O	real time control output
V_{DD3}	45	I	+5 V supply voltage 3
VMUX	46	I	VRAM output multiplexing, control input for the 32- to 16-bit multiplexer (Table 3)
V_{SS3}	47	I	GND3 (0 V)
SODD	48	O	odd/even field sequence reference output related to the scaler output (test only)
SVS	49	O	vertical sync signal related to the scaler output (test only)
SHREF	50	O	delayed HREF signal related to the scaler output (test only)
PXQ	51	O	pixel qualifier output signal to mark active pixels of a qualified line (polarity: QPP-bit; test only)
LNQ	52	O	line qualifier output signal to mark active video phase (polarity: QPP-bit; test only)
VOEN	53	I	enable input of VRAM output
HFL	54	O	FIFO half-full flag output signal
INCADR	55	O	line increment / vertical reset control output
VCLK	56	I	clock input signal of FIFO output
VRO31	57	O	32-bit digital VRAM output port (bits 31 to 29)
VRO30	58	O	
VRO29	59	O	
V_{SS4}	60	-	GND4 (0 V)

SYMBOL	PIN	STATUS	DESCRIPTION
V_{DD4}	61	-	+5 V supply voltage 4
VRO28	62	O	32-bit VRAM output port (bits 28 to 16)
VRO27	63	O	
VRO26	64	O	
VRO25	65	O	
VRO24	66	O	
VRO23	67	O	
VRO22	68	O	
VRO21	69	O	
VRO20	70	O	
VRO19	71	O	
VRO18	72	O	
VRO17	73	O	
VRO16	74	O	
V_{SS5}	75	-	GND5 (0 V)
i.c.	76	-	internally connected
V_{DD5}	77	-	+5 V supply voltage 5
VRO15	78	O	32-bit VRAM output port (bits 15 to 3)
VRO14	79	O	
VRO13	80	O	
VRO12	81	O	
VRO11	82	O	
VRO10	83	O	
VRO9	84	O	
VRO8	85	O	
VRO7	86	O	
VRO6	87	O	
VRO5	88	O	
VRO4	89	O	
VRO3	90	O	

SYMBOL	PIN	STATUS	DESCRIPTION
V_{DD6}	91	-	+5 V supply voltage 6
VRO2	92	O	32-bit VRAM output port (bits 2 to 0)
VRO1	93	O	
VRO0	94	O	
DIR	95	I	direction control of Expansion Bus
YUV15	96	I/O	digital 16-bit video (Y) input/output signal (bits 15 to 8)
YUV14	97	I/O	
YUV13	98	I/O	
YUV12	99	I/O	
YUV11	100	I/O	
YUV10	101	I/O	
YUV9	102	I/O	
YUV8	103	I/O	
V_{SS6}	104	-	GND6 (0 V)
i.c.	105	-	internally connected
V_{DD7}	106	-	+5 V supply voltage 7
YUV7	107	I/O	digital 16-bit colour-difference (UV) input/output signal (bits 7 to 0)
YUV6	108	I/O	
YUV5	109	I/O	
YUV4	110	I/O	
YUV3	111	I/O	
YUV2	112	I/O	
YUV1	113	I/O	
YUV0	114	I/O	
HREF	115	I/O	horizontal reference signal
VS	116	I/O	vertical sync input/output signal with respect to the YUV input signal
HS	117	O	horizontal sync signal, programmable
AP	118	I	connected to ground (action pin for testing)
SP	119	I	connected to ground (shift pin for testing)
V_{SS7}	120	-	GND7 (0 V)

PIN CONFIGURATION

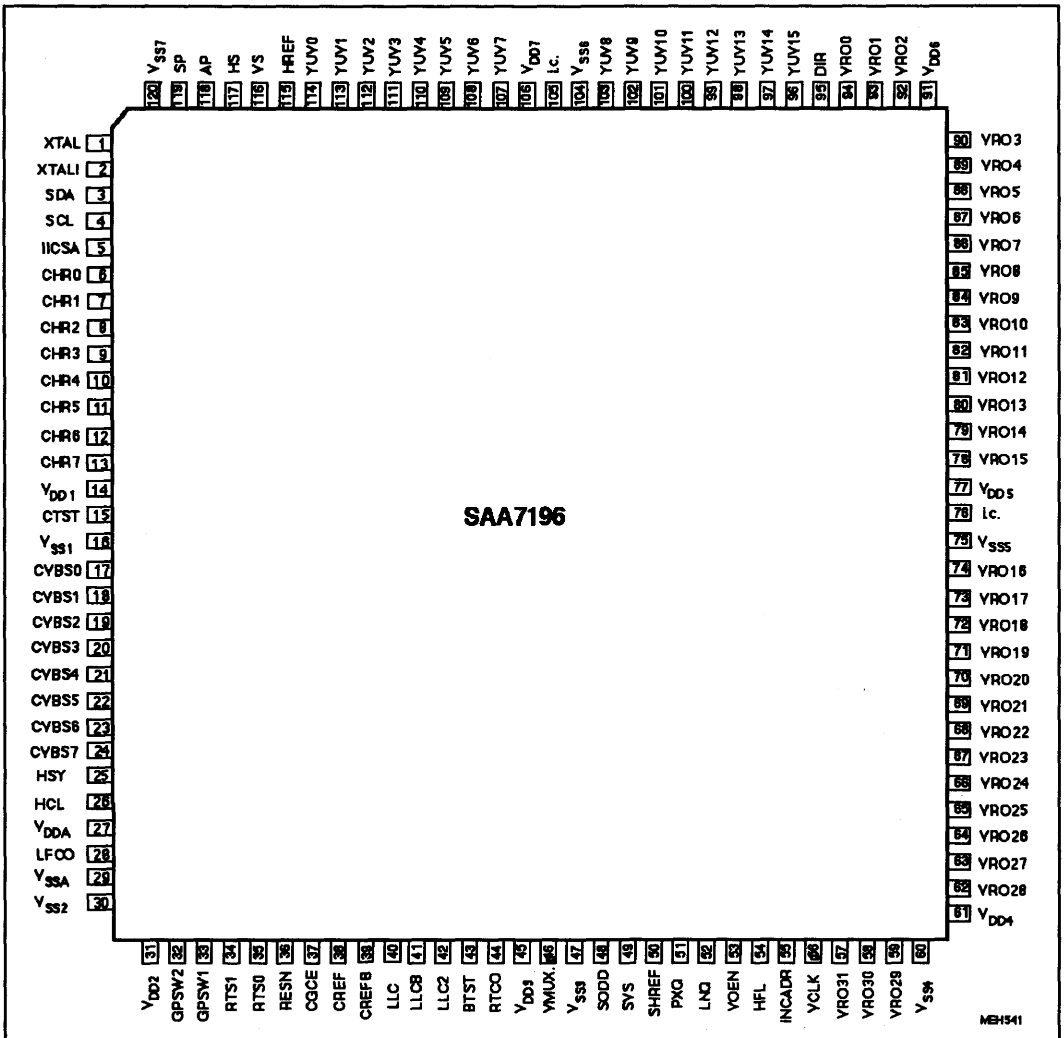


Fig.2 Pin configuration.

Clock signal generator circuit for Destop Video systems (SCGC)

SAA7197

Supercedes data of April 1991

FEATURES

- Suitable for Desktop Video systems
- Two different sync sources selectable
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LLCA, LLCB, LLC2A and LLC2B (2nd and 4th multiples of input frequency)
- PLL mode or VCO mode selectable
- Reset control and power fail detection

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	5	-	9	mA
I_{DDD}	digital supply current	10	-	60	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_i	input frequency range	6.0	-	7.2	MHz
V_I	input voltage LOW input voltage HIGH	0 2.4	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA7197 generates all clock signals required for a digital TV system suitable for the SAA719x family. The circuit operates in either the phase-locked loop mode (PLL) or voltage controlled oscillator mode (VCO).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7197	20	DIL	plastic	SOT146
SAA7197T	20	mini-pack (SO20)	plastic	SOT163A

Clock signal generator circuit for Destop Video systems (SCGC)

SAA7197

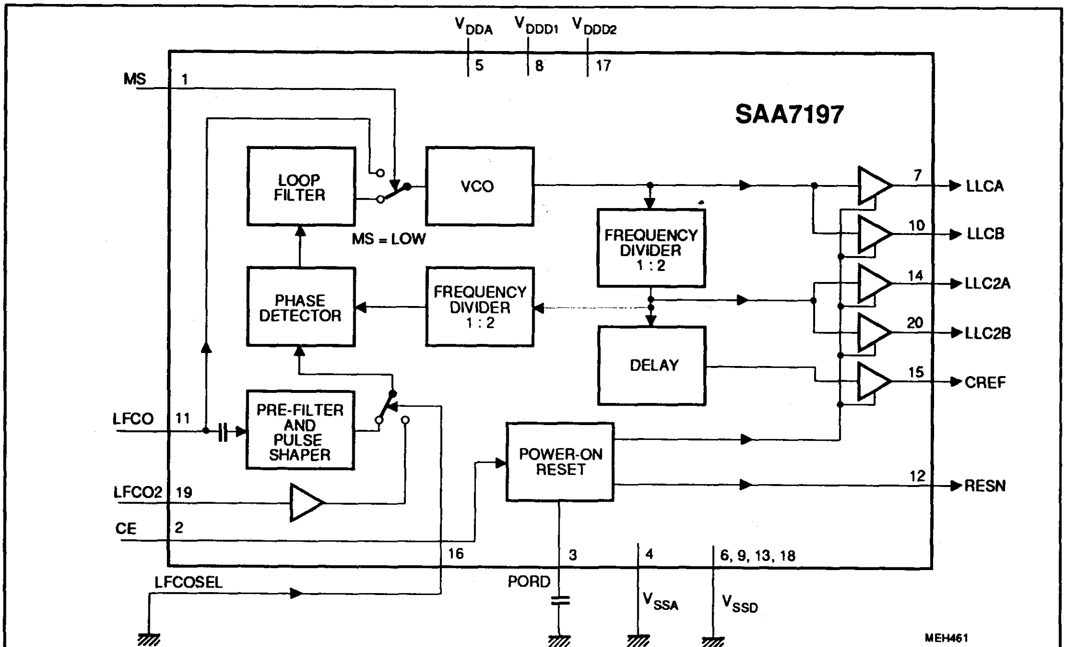


Fig.1 Block diagram.

FUNCTION DESCRIPTION

The SAA7197 generates all clock signals required for a digital TV system suitable for the SAA719x family consisting of an 8-bit analog-to-digital converter (ADC8), digital video multistandard decoder, square pixel (DMSD-SQP), digital video colour space converter (DCSC) and optional extentions. The SAA7197 completes a system for Desktop Video applications in conjunction with memory controllers.

The input signal LFCO is a digital-to-analog converted signal provided by the DMDS-SQPs horizontal PLL. It is the multiple of the line frequency:

7.38 MHz = 472 x f_H in 50 Hz systems
6.14 MHz = 360 x f_H in 60 Hz systems

LFCO2 (TTL-compatible signal from an external reference source) can be applied to pin 19 (LFCOSEL = HIGH).

The input signal LFCO or LFCO2 is multiplied by factors 2 or 4 in the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LLCA (pin7), LLCB (pin 10), LLC2A (pin 14) and LLC2B (pin 20). The rectangular output signals have 50 % duty factor. Outputs with equal frequency may be connected together externally. The clock outputs go HIGH during power-on reset (and chip enable) to ensure that no output clock signals are available the PLL has locked-on.

Mode select MS

The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit operates as an oscillator and frequency divider. This function is not tested.

Source select LFCOSEL

Line frequency control signal LFCO (pin 11) is selected by LFCOSEL = LOW. LFCOSEL = HIGH selects LFCO2 input signal (pin 19). This function is not tested.

Chip enable CE

The buffer outputs are enabled and RESN set HIGH by CE = HIGH (Fig.4). CE = LOW sets the clock outputs HIGH and RESN output LOW.

CREF output

2 f_{LFCO} output to control the clock dividers of the DMSD-SQP chip family.

Power-on reset

Power-on reset is activated at power-on, when the supply voltage decreases below 3.5 V (Fig.4) or when chip enable is done. The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuits of this digital TV system.
The LFCO or LFCO2 input signals have to be applied before RESN becomes HIGH.

Clock signal generator circuit for Destop Video systems (SCGC)

SAA7197

PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode)*
CE	2	chip enable /reset (HIGH = outputs enabled)
PORD	3	power-on reset delay, dependent on external capacitor
V_{SSA}	4	analog ground (0 V)
V_{DDA}	5	analog supply voltage (+5 V)
V_{SSD1}	6	digital ground 1 (0 V)
LLCA	7	line-locked clock output signal (4 times f_{LFCO})
V_{DDD1}	8	digital supply voltage 1 (+5 V)
V_{SSD2}	9	digital ground 2 (0 V)
LLCB	10	line-locked clock output signal (4 times f_{LFCO})
LFCO	11	line-locked frequency control input signal 1
RESN	12	reset output (active-LOW, Fig.4)
V_{SSD3}	13	digital ground 3 (0 V)
LLC2A	14	line-locked clock output signal 2A (2 times f_{LFCO})
CREF	15	clock reference output, qualifier signal (2 times f_{LFCO})
LFCOSEL	16	LFCO source select (LOW = LFCO selected)*
V_{DDD2}	17	digital supply voltage 2 (+5 V)
V_{SSD4}	18	digital ground 4 (0 V)
LFCO2	19	line-locked frequency control input signal 2*
LLC2B	20	line-locked clock output signal 2B (2 times f_{LFCO})

PIN CONFIGURATION

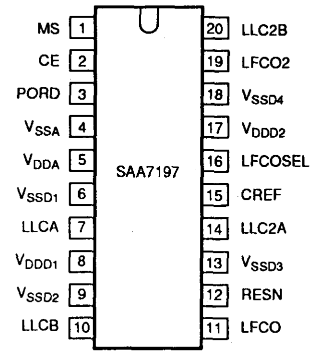


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins as well as supply pins together connected.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	−0.5	7.0	V
V_{DDD}	digital supply voltage (pins 8 and 17)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{DDA} - V_{DDD}$	-	±100	mV
V_O	output voltage (I_{OM} = 20 mA)	−0.5	V_{DDD}	V
P_{tot}	total power dissipation (DIL20)	0	1.1	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling** for all pins	-	tbf	V

* MS and LFCO2 functions are not tested. LFCO2 is a multiple of horizontal frequency.

** Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices ".

CHARACTERISTICS

V_{DDA} = 4.5 to 5.5 V; V_{DDD} = 4.5 to 5.5 V; f_{LFCO} = 5.5 to 8.0 MHz and T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
I_{DDA}	analog supply current (pin 5)		5	-	9	mA
I_{DDD}	digital supply current ($I_8 + I_{17}$)	note 1	10	-	60	mA
V_{reset}	power-on reset threshold voltage	Fig.4	-	3.5	-	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	-	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	-	V_{DDA}	V
f_{LFCO}	input frequency range		5.5	-	8.0	MHz
C_{11}	input capacitance		-	-	10	pF
Inputs MS, CE, LFCOSEL and LFCO2 (pins 1, 2, 16 and 19)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}	V
f_{LFCO2}	input frequency range for LFCO2	note 3	5.5	-	8.0	MHz
I_{LI}	input leakage current		-	-	10	µA
C_I	input capacitance		-	-	5	pF
Output RESN (pin 12)						
V_{OL}	output voltage LOW		0	-	0.4	V
V_{OH}	output voltage HIGH		2.4	-	V_{DDD}	V
t_d	RESN delay time	C_3 = 0.1µF; Fig.4	20	-	200	ms
Output CREF (pin 15)						
V_{OL}	output voltage LOW		0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DDD}	V
f_{CREF}	output frequency CREF	Fig.3	-	2 $f_{LFCO(2)}$		MHz
C_L	output load capacitance		15	-	40	pF
t_{SU}	set-up time	Fig.3; note 1	12	-	-	ns
t_{HD}	hold time	Fig.3; note 1	4	-	-	ns
Output signals LLCA, LLCB, LLC2A and LLC2B (pins 7, 10, 14, and 20); note 3						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.6	-	V_{DDD}	V
		CE = HIGH (pin 2)	2.6	-	V_{DDD}	V
t_{comp}	composite rise time	Fig.3; notes 1 and 2	-	-	8	ns

Clock signal generator circuit for Destop Video systems (SCGC)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LL}	output frequency LLCA	Fig.3	-	4 $f_{LFCO(2)}$		MHz
	output frequency LLCB		-	4 $f_{LFCO(2)}$		MHz
	output frequency LLC2A		-	2 $f_{LFCO(2)}$		MHz
	output frequency LLC2B		-	2 $f_{LFCO(2)}$		MHz
t_r, t_f	rise and fall times	Fig.3;	-	-	5	ns
t_{LL}	duty factor LLCA, LLCB, LLC2A and LLC2B (mean values)	note 1; Fig.3; at 1.5 V level	40	50	60	ns

Notes to the characteristics

1. f_{LFCO} = 7.0 MHz and output load 40 pF (Fig.3)
2. t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Fig.3) including rise time, skew and jitter components. Measurements taken between 0.6 V and 2.6 V. Skew between two LLx clocks will not deviate more than ±2 ns if output loads are matched within 20 %.
3. LFCO2 functions not tested.

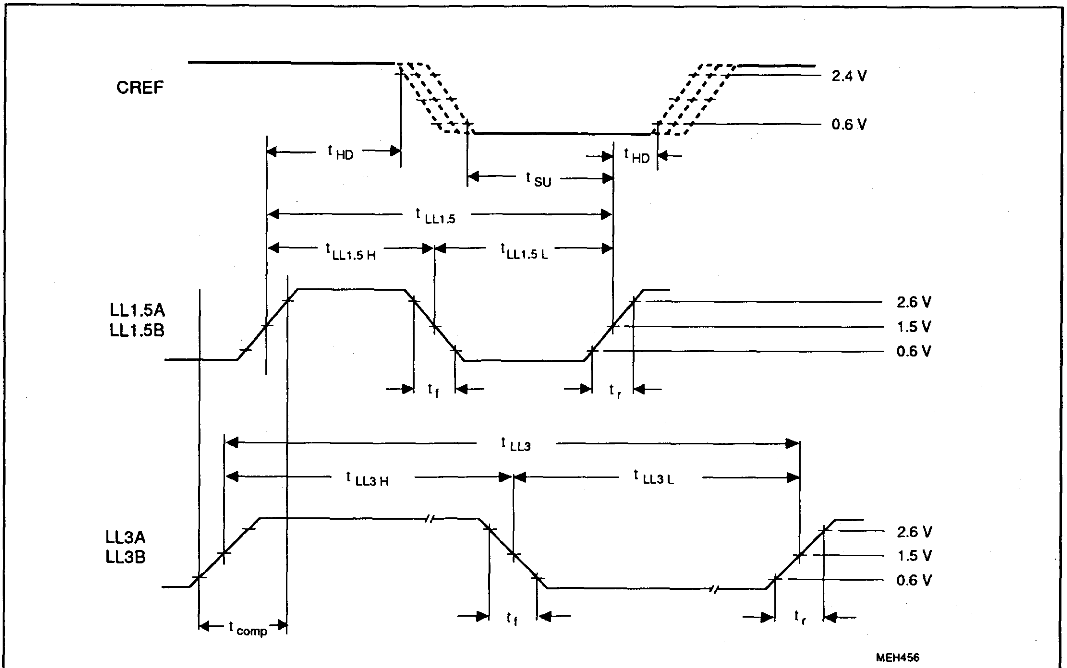


Fig.3 Output timing.

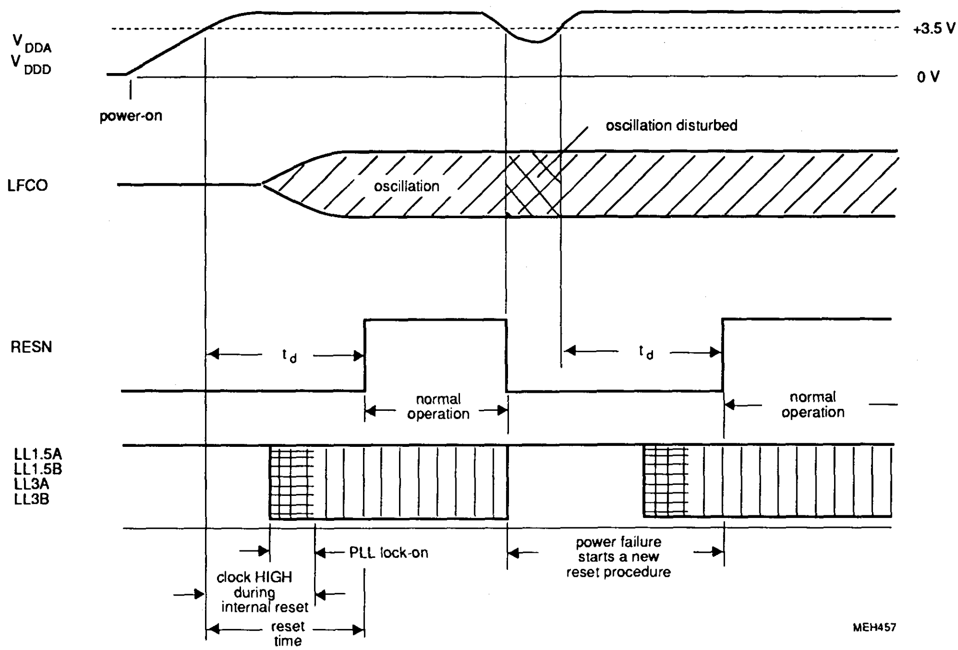


Fig.4 Reset procedure.

Digital video encoder, GENLOCK-capable

SAA7199B

1. FEATURES

- Monolithic integrated CMOS video encoder circuit
- Standard MPU (12 lines) and I^2C-bus interfaces for controls
- Three 8-bit signal inputs PD(7-0) for RGB respectively YUV or indexed colour signals (Tables 10 to 17)
- Square pixel and CCIR input data rates
- Band-limited composite sync pulses
- Three 256X8 colour look-up tables (CLUTs) e. g. for gamma-correction
- External subcarrier from a digital decoder (SAA7151B or SAA7191B)
- Multi-purpose key for real-time format switching
- Autonomous internal blanking
- Optional GENLOCK operation with adjustable horizontal sync timing and adjustable subcarrier phase
- Stable GENLOCK operation in VCR standard playback mode
- Optional still video capture extension
- Three suitable video 9-bit digital-to-analog converters
- Composite analog output signals CVBS, Y and C for PAL/NTSC
- "Line 21" data insertion possible

2. GENERAL DESCRIPTION

The SAA7199B encodes digital base-band colour/video data into analog Y, C and CVBS signals (S-Video included). Pixel clock and data are line-locked to the horizontal scanning frequency of the video signal. The circuit can be used in a square pixel or in a consumer TV application. Flexibility is provided by programming facilities via MPU-bus (parallel) or I^2C-bus (serial).

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage range (pins 2, 21 and 41)	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage range (pins 64, 66, 70 and 72)	4.75	5.0	5.25	V
I_P	total supply current	-	-	200	mA
V_I	input signal levels	TTL-compatible			
V_o	analog output signals Y, C and CVBS without load (peak-to-peak value)	-	2	-	V
R_L	output load resistance	90	-	-	Ω
ILE	LF integral linearity error in output signal (9-bit DAC)	-	-	±1	LSB
DLE	LF differential linearity error in output signal (9-bit DAC)	-	-	±0.5	LSB
T_{amb}	operating ambient temperature range	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7199B	84	PLCC	plastic	SOT189CG

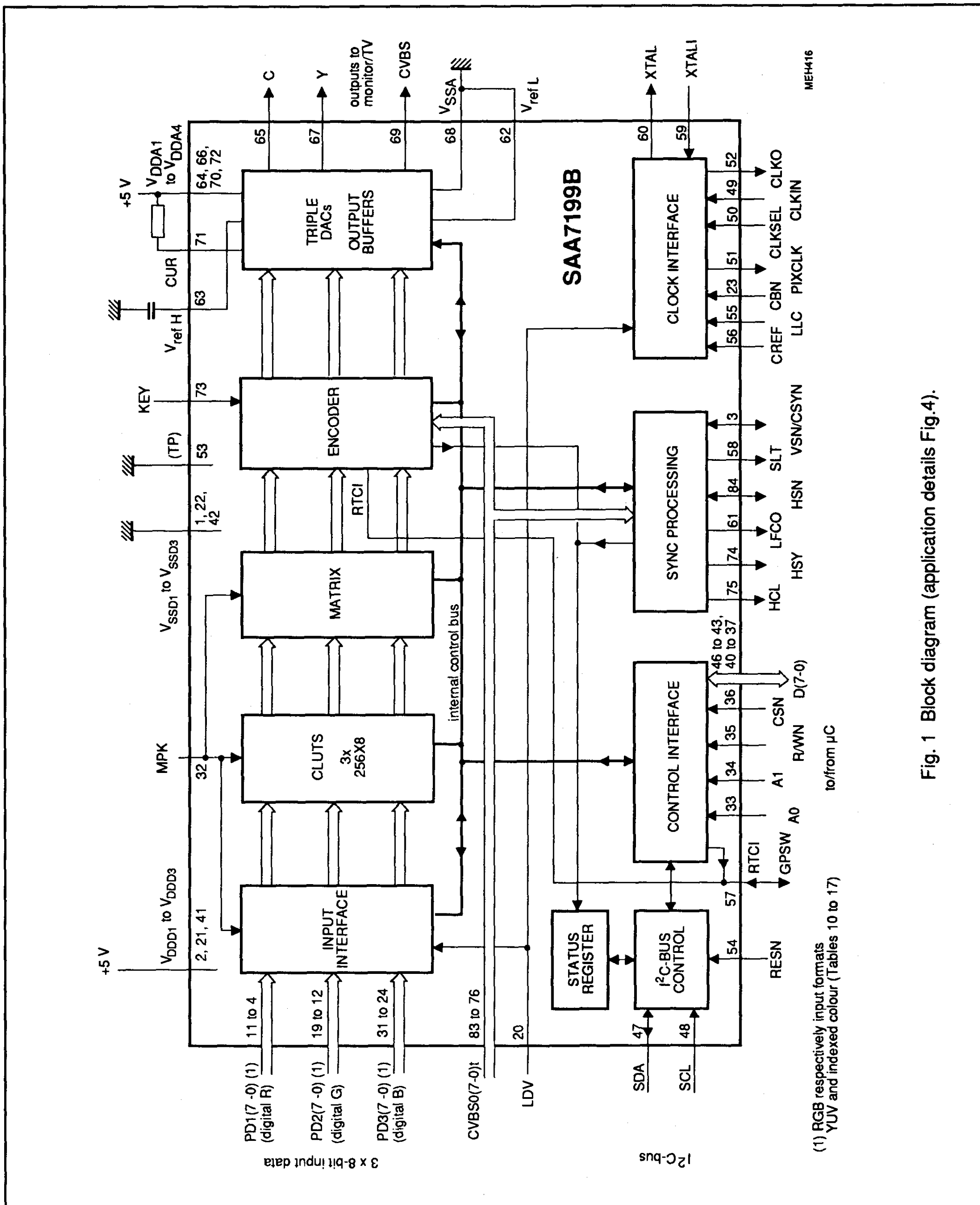


Fig. 1 Block diagram (application details Fig.4).

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSD1}	1	digital ground 1 (0 V)
V_{DDD1}	2	+5 V digital supply 1
VSN	3	vertical sync output (3-state), conditionally composite sync output; active LOW or active HIGH
PD1(0)	4	data 1 input: digital signal R (red) respectively V signal (formats in Table 6)
PD1(1)	5	
PD1(2)	6	
PD1(3)	7	
PD1(4)	8	
PD1(5)	9	
PD1(6)	10	
PD1(7)	11	
PD2(0)	12	data 2 input: digital signal G (green) respectively Y signal or indexed colour data (formats in Table 6)
PD2(1)	13	
PD2(2)	14	
PD2(3)	15	
PD2(4)	16	
PD2(5)	17	
PD2(6)	18	
PD2(7)	19	
LDV	20	load data clock input signal to input interface (samples PDn(7-0), CBN, MPK, KEY and RTCI)
V_{DDD2}	21	+5 digital supply 2
V_{SSD2}	22	digital ground 2 (0 V)
CBN	23	composite blanking input; active LOW
PD3(0)	24	data 3 input: digital signal B (blue) respectively U signal (formats in Table 6)
PD3(1)	25	
PD3(2)	26	
PD3(3)	27	
PD3(4)	28	
PD3(5)	29	
PD3(6)	30	
PD3(7)	31	
MPK	32	multi-purpose key; active HIGH
A0	33	subaddress bit A0 for microcomputer access (Table 3)
A1	34	subaddress bit A1 for microcomputer access (Table 3)

SYMBOL	PIN	DESCRIPTION
R/WN	35	read/ write not input signal from microcontroller
CSN	36	chip select input for parallel interface; active LOW
D0 D1 D2 D3	37 38 39 40	bidirectional port from/to microcontroller (bits D3 to D0)
V_{DDD3}	41	+5 V digital supply 3
V_{SSD3}	42	digital ground 3
D4 D5 D6 D7	43 44 45 46	bidirectional port from/to microcontroller (bits D7 to D4)
SDA	47	I^2C-bus data line
SCL	48	I^2C-bus clock line
CLKIN	49	external clock signal input (maximum 60 MHz)
CLKSEL	50	clock source select input
PIXCLK	51	CLKO/2 or conditionally CLKO output signal
CLKO	52	selected clock output signal (LLC or CLKIN)
TP	53	connect to ground (test pin)
RESN	54	reset input; active LOW
LLC	55	line-locked clock input signal from external CGC
CREF	56	clock qualifier of external CGC
GPSW / RTCI	57	general purpose switch output (set via I^2C-bus or MPU-bus); real-time control input, defined by I^2C or MPU programming
SLT	58	GENLOCK flag (3-state): HIGH = sync lost in GENLOCK mode; LOW = otherwise
XTALI	59	crystal oscillator input (26.8 or 24.576 MHz)
XTAL	60	crystal oscillator output
LFCO	61	line frequency control output signal for external CGC
$V_{ref\,L}$	62	reference LOW voltage of DACs (resistor chains)
$V_{ref\,H}$	63	reference HIGH voltage of DACs (resistor chains)
V_{DDA4}	64	+5 V analog supply 4 for resistor chains of the DACs
C	65	chrominance analog output signal C
V_{DDA1}	66	+5 V analog supply 1 for output buffer amplifier of DAC1
Y	67	luminance analog output signal Y
V_{SSA}	68	analog ground (0 V)

SYMBOL	PIN	DESCRIPTION
CVBS	69	CVBS analog output signal
V_{DDA2}	70	+5 V analog supply 2 for output buffer amplifier of DAC2
CUR	71	current input for analog output buffers
V_{DDA3}	72	+5 V analog supply 3 for output buffer amplifier of DAC3
KEY	73	key signal to insert CVBS input signal into encoded CVBS output signal; active HIGH
HSY	74	horizontal sync indicator output signal; active HIGH (3-state output to ADC)
HCL	75	horizontal clamping output; active HIGH (3-state output)
CVBS0	76	digital CVBS input signal
CVBS1	77	
CVBS2	78	
CVBS3	79	
CVBS4	80	
CVBS5	81	
CVBS6	82	
CVBS7	83	
HSN	84	horizontal sync output; active LOW or active HIGH for 60/66/72 x PIXCLK at 12.27/13.5/14.75 MHz (3-state output)

FUNCTIONAL DESCRIPTION

The SAA7199B is a digital video encoder that translates digital RGB, YUV or 8-bit indexed colour signals into the analog PAL/NTSC output signals Y (luminance), C (4.43/3.58 MHz chrominance) and CVBS (composite signal including sync).

Four different modes are selectable (Table 9):

- stand-alone mode (horizontal and vertical timings are generated)
- slaver mode (stand-alone unit that accepts external horizontal and vertical timing), and optional real-time information for subcarrier/clock from a digital colour decoder
- GENLOCK mode (GENLOCK capabilities are achieved in conjunction with determined ICs).
- test mode (only clock signal is required)

The input data rate (pixel sequence) has an integer relationship to the number of horizontal clock cycles (Table 1). A sufficient stable external clock signal ensures correct encoding. The generated clock frequency in the GENLOCK mode may deviate by ±7 % depending on the reference signal which is corresponding to its input sync signal. The clock will be nominal in the GENLOCK mode when the reference signal is absent (nominal with crystal oscillator accuracy for TV time constants, and nominal ±1.4 % for VCR time constants).

The on-chip colour conversion matrix provides CCIR 601 code-compatible transcoding of RGB to YUV data.

Table 1 Pixel relationships

ACTIVE PIXELS PER LINE	FIELD RATE	MULTIPLES OF LINE FREQUENCY	PIXCLK OUTPUT SIGNAL (MHz)	XTAL (MHz)
640 (square)	60 Hz	780	12.272727	26.8
720	60 Hz	858	13.5	24.576
768 (square)	50 Hz	944	14.75	26.8
720	50 Hz	864	13.5	24.576

RGB data out of bounds, with respect to CCIR 601 specification, can be clipped to prevent over-loading of the colour modulator. RGB data input can be either in linear colour space or in gamma-corrected colour space. YUV data must be gamma-corrected according to CCIR 601. This circuit operates primarily in a 24-bit colour space (3 x 8-bit) but can also accomodate different data formats (4:1:1, 4:2:2 and 4:4:4) as well as 8-bit indexed pseudo-colour space operations (FMT-bits in Table 6).

RGB CLUTs on chip provide gamma-correction and/or other CLUT functions. They consist of programmable tables to be loaded

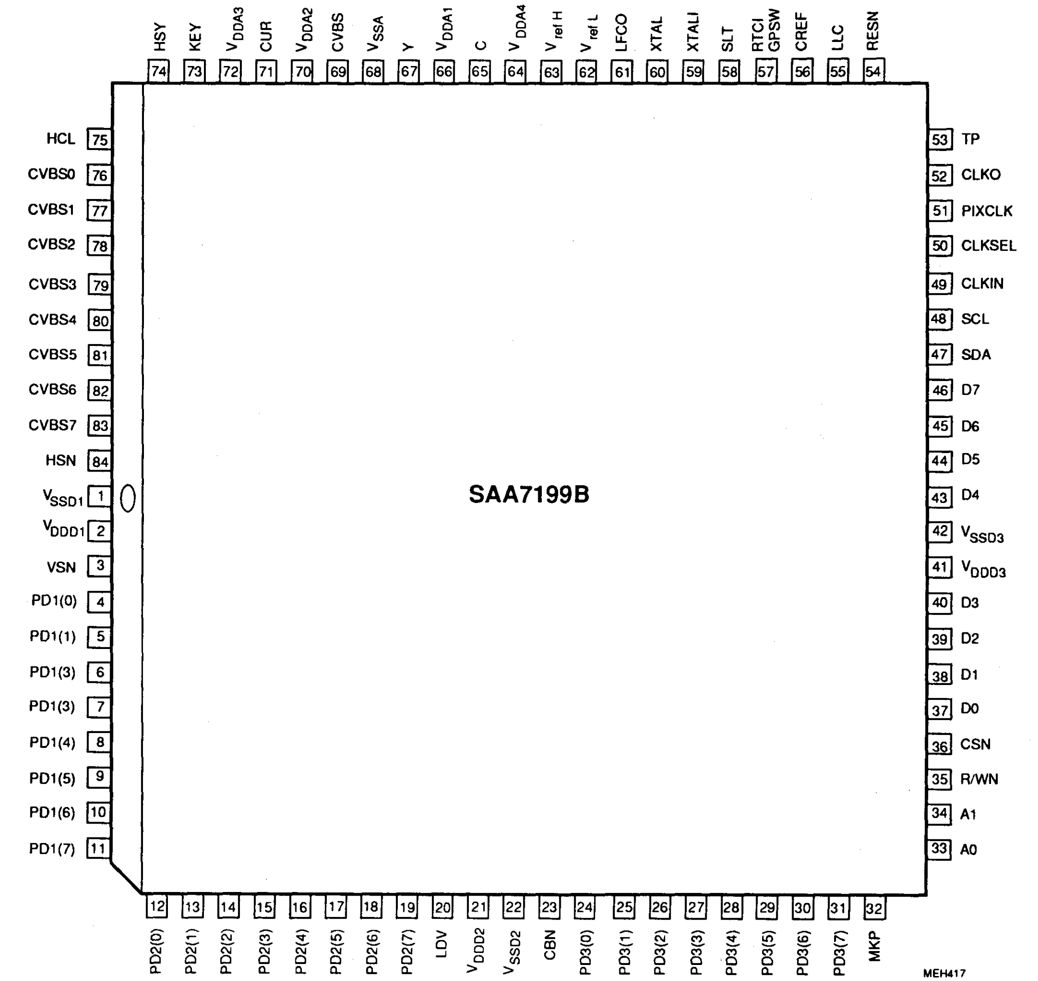


Fig.2 Pin configuration.

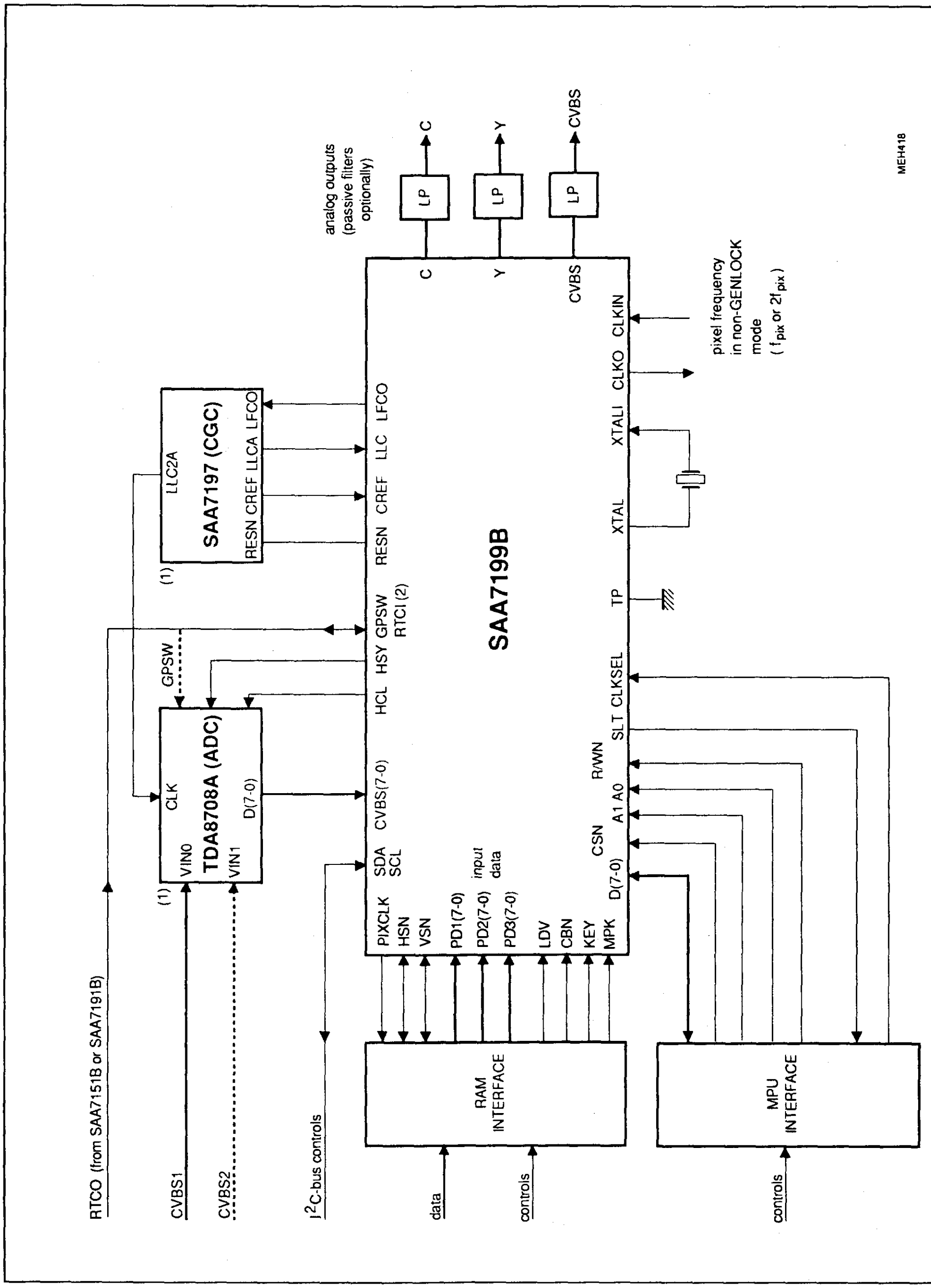
independently, and they generate 24-bit gamma-corrected output signals from 24-bit data of one of the input formats or from 8-bit indexed pseudo-colour data.

Required modulation is performed. The digital YUV data is encoded according to standards RS-170A (composite NTSC) and CCIR 624-4 (composite PAL-B/G). S-Video output signal is available (Y/C) as well as some sub-standard output signals (STD-bits in Table 6).
A 7.5 IRE set-up level is automatically selected in the 60 Hz mode – there is none in 50 Hz mode.

The analog signal outputs can drive directly into terminated 75 Ω coaxial lines, a passive external filter is recommended (Figures 3 and 13).

Analog post-filtering is required (LP in Fig.3).

GENLOCK to an external reference signal is achieved by addition of a video ADC and a clock generator combination. Thus, the system is enabled to lock on a stable video source or to a stable VCR source (normal playback). The SAA7199B, the ADC and the clock generator



(1) necessary in GENLOCK mode
(2) RTCI optional (GPSW not possible)

Fig.3 System configuration.

combination (Fig.3) form a control loop achieving a highly stable line-locked clock. The clock has to be generated by a crystal oscillator without this possibility.
The GENLOCK mode is not available in a single device set-up.

Control interface

The SAA7199B supports a standard parallel MPU interface as well as the serial I²C-bus interface. The MPU has a direct access to internal control registers and colour tables. Update is possible at any time, excluding coincident internal reading and external writing of the same cell (the current pixel value could be destroyed).
The two interfaces of Table 2 are selected automatically. However, the I²C control is inactive when the MPU interface is selected by CSN = LOW. No simultaneous access must occur. I²C-bus and MPU control complement each other and have access to common registers controlled via a common internal bus. The programmer can use virtually identical programs.
The internal memory space is devided into the look-up table and the control table, each with its own 8-bit address register is used as a pointer for specific location. This address register is provided with auto-incrementation and can be written by only one addressing.

The look-up table contains three banks of 256 bytes. Therefore, each read or write cycle must access to all three banks in a determined order. The support logic is part of the control interface.

Timing (Fig.3).

The reference to generate internal clocks from LLC in GENLOCK operation with SAA7197 is CREF (CREF = LLC/2). In this case input CLKSEL is HIGH and the SRC-bit is 1.

In non-GENLOCK operation the signal from CLKIN is used and LDV is clock reference (input CLKSEL = 0; SCR-bit = CPR-bit = 0).

Table 2 Access to the contol interface

SYMBOL	DESCRIPTION
SDA (I²C-bus) SCL	serial data line (bi-directional) clock line
A1, A0 (MPU-bus) R/WN CSN GPSW RESN	address inputs read/write control chip select; I²C-bus disabled (at LOW) general purpose switch output (bit of control register) reset signal (active-LOW)

Table 3 Address assignment

ADDRESS INPUTS A1	A0	I²C-BUS SUBADDRESS	SELECTION
0	0	00	ADR-CLUT (address register of look-up tables)
0	1	01	DATA-CLUT
1	0	02	ADR-CTRL (index register of control table)
1	1	03	DATA-CTRL

Pins LLC and CLKIN are tied together when no switching between LLC and CLKIN is applied. In Fig.3 it is assumed that LLC and CLKIN are double the pixel clock frequency of CREF respectively LDV.
CREF must be at the same frequency (or constant HIGH or LOW) when LLC is at pixel clock frequency.
CPR-bit = 1 if CLKIN is at pixel clock frequency.
Buffered CLKO signal is always delayed. LLC or CLKIN signals are according to CLKSEL

Mapping

Mapping of external control signals onto internal bus. The method is simple. The MPU- bus contains the signals of Table 4 (names in chip-internal nomenclature).

Bit allocation

The Bit Allocation Map (BAM) shows the individual control signals, used to control the different operational modes of the circuit. The I²C-bus is normally used for control. The SAA7199B additionally has a MPU-bus interface for direct microprocessor connection. The following BAM resembles the I²C-bus type but can be also used for the parallel bus. The control registers of Table 5 are indexed from 00 to 0F (hex). Auto-incrementation is applied.

Digital-to-analog converters

The converters use a combination of resistor chains with low-impedance output buffers. The bottom output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V. Fig.15 shows the application for 1.23 V/ 75 Ω outputs, using the serial 25 Ω + 22 Ω resistors.

Each digital-to-analog converter has its own supply pin for purpose of decoupling. V_{DDA4} is the supply voltage for the resistor chains of the three DACs. The accuracy of this supply voltage influences directly the output amplitudes.
The current CUR into pin 71 is 0.3 mA (V_{DDA4} = 5 V, R_{64-71} = 20 kΩ); a larger current improves the bandwidth but increases the integral non-linearity.

Table 4 Signals on the internal bus

SYMBOL	DESCRIPTION	
R-WN C-TN D-AN DI/DO(0-7) EN	Select read/write (read = 1; write = 0) Control table/look-up table (control table = 1; look-up table = 0) Select data/address (data = 1; address = 0) Data bus on port inputs/outputs D7 to D0 Enable from control interface to synchronize data transfer	
INTERNAL PARALLEL BUS	**PARALLEL INTERFACE**	**I²C-BUS INTERFACE**
R-WN C-TN A-TN DI/DO(0-7) EN	R/WN (pin 35) A1 (pin 34) A0 (pin 33) D7 to D0 CSN and R/WN	LSB of slave address byte (read = HIGH; write = LOW) X) 4 subaddresses after decoding X) Data bits D7 to D0 for each subaddress Enable by every 9th clock of sample of SCL (control of serial-to-parallel conversion)

Table 5 Bit allocation map (I²C-bus access in Table 8)

INDEX BINARY	HEX	DATA BYTE D7	D6	D5	D4	D3	D2	D1	D0	DF**
Input processing										
0000 0000	00	VTBY	FMT2	FMT1	FMT0	SCBW	CCIR	MOD1	MOD0	5C
0000 0001	01	TRER7	TRER6	TRER5	TRER4	TRER3	TRER2	TRER1	TRER0	XX
0000 0010	02	TREG7	TREG6	TREG5	TREG4	TREG3	TREG2	TREG1	TREG0	XX
0000 0011	03	TREB7	TREB6	TREB5	TREB4	TREB3	TREB2	TREB1	TREB0	XX
Sync processing										
0000 0100	04	SYSEL1	SYSEL0	SCEN	VTRC	NINT	HPLL	HLCK*	OEF*	10
0000 0101	05	0	0	GDC5	GDC4	GDC3	GDC2	GDC1	GDC0	21
0000 0110	06	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0	52
0000 0111	07	0	0	PSO5	PSO4	PSO3	PSO2	PSO1	PSO0	32
Control, clock and output formatter										
0000 1000	08	DD	KEYE	SRC	CPR	COKI	IM	GPSW	SRSN	64
0000 1001	09	0	BAME	MPKC1	MPKC0	IEPI	RTSC	RTIN	RTCE	02
0000 1010+	0A+	0	0	0	0	0	0	0	0	00
0000 1011+	0B+	0	0	0	0	0	0	0	0	00
Encoder control										
0000 1100	0C	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0	XX++
0000 1101	0D	FSCO7	FSCO6	FSCO5	FSCO4	FSCO3	FSCO2	FSCO1	FSCO0	00
0000 1110	0E	0	0	0	CLCK*	STD3	STD2	STD1	STD0	0C
0000 1111+	0F+	0	0	0	0	0	0	0	0	

*) read only bits +) reserved ++) adjust as required.

**) DF is the default value for a typical programming example: GENLOCK mode for a VCR; non-gamma-corrected RGB data (realtime keying is possible). SLT will be set if there is no horizontal lock. NTSC-M standard with normal colour bandwidth and 12.2727 MHz pixel rate. CSYN signal will be provided, coming 8 pixel clocks earlier, to compensate pipeline delay in the previous RAM interface. The encoded CVBS is 12 clocks earlier than the CVBS reference on the input of the previous ADC. The CLUTs are bypassed at MPK = HIGH in real-time.

Table 6 Function of register bits of Table 5

Bits	Function
Index "00" VTBY	Video look-up table by-pass: 0 = not bypassed; 1 = bypassed (OR connectable with MPK)
FMT2 to FMT0	Input formats: FMT2 FMT1 FMT0 – format 0 0 0 – YUV 4:1:1 format; DMSD2 compatible 0 0 1 – YUV 4:1:1 format; customized 0 1 0 – YUV 4:2:2 format; DMSD2 compatible 0 1 1 – YUV 4:2:2 format; customized 1 0 0 – YUV 4:4:4 format 1 0 1 – RGB 4:4:4 format 1 1 0 – reserved 1 1 1 – 8-bit indexed colour
SCBW	Chrominance bandwidth: 0 = enhanced; 1 = standard
CCIR	Select level: 0 = DMSD2 levels; 1 = CCIR levels
MOD1 to MOD0	Select mode: MOD1 MOD0 – mode 0 0 – GENLOCK mode 0 1 – stand-alone mode 1 0 – slave mode 1 1 – test mode
Index "01" TRER7 to TRER0	Test register Red (read/write via MPU-bus; write only via I^2C-bus)
Index "02" TREG7 to TREG0	Test register Green (read/write via MPU-bus; write only via I^2C-bus)
Index "03" TREB7 to TREB0	Test register Blue (read/write via MPU-bus; write only via I^2C-bus)
Index "04" SYSEL1 to SYSEL0	Sync select: SYSEL1 SYSEL0 – synchronized from 0 0 – CSYN (active LOW; pin 3) 0 1 – HSN and VSN (active LOW; pins 84 and 3) 1 0 – CSYN (active HIGH; pin 3) 1 1 – HSN and VSN (active HIGH; pins 84 and 3)
SCEN	Sync/clamping (HSY/HCL) enable: 0 = disabled (set to HIGH); 1 = enabled
VTRC	Select TV/VTR mode: 0 = 0 TV mode (slow); 1 = VTR mode (fast)
NINT	Select interlace of encoded signal: 0 = interlaced (262.5/262.5 or 312.5/312.5) 1 = non-interlaced (262/262 or 312/312 in modes 1 and 3 only)

HPLL	Select horizontal lock: 0 = lock enabled; 1 = lock disabled (crystal reference)
OEF	Status bit field organization (to be read): 0 = even field; 1 = odd field
HLCK	Status bit sync indication (to be read): 0 = locked to external sync 1 = external sync lost
Index "05" GDC5 to GDC0	GENLOCK delay compensation, note 1: data 00 to 3F equals timing of CVBS output signal is (46 – GDC) pixel clocks = t_{ofs} earlier with respect to reference point t_{REF1}. (t_{REF1} corresponds to the falling edge of the horizontal sync pulse of CVBS input signal; t_{ofs} is designated for propagation delay of extern GENLOCK source, Fig.10).
Index "06" IDEL7 to IDEL0	Increment delay: update of line-locked clock frequency (Table 5, data "43" hex recommended)
Index "07" PSO7 to PSO0	Phase sync in output signal, note 1: data 00 to 3F equals to active slope of HSN, VSN/CSYN is (58 – PSO) pixel clocks = t_{Rint} earlier with respect to reference point t_{REF2}. (t_{REF2} corresponds to PSO = 58; t_{Rint} is designated for pipeline delay of the feeding RAM interface, Fig.10).
Index "08" DD	Digital video encoder disable: 0 = enabled; 1 = disabled
KEYE	Keying enable: 0 = disabled; 1 = enabled (logically AND-connected with KEY)
SRC	Clock source: 0 = external system clock; 1 = DTV2 system clock
CPR	Clock phase reference: 0 = LDV is (pin 20); 1 = LDV is not
COKI	Colour-killer: 0 = colour on; 1 = colour off (subcarrier is switched off)
IM	Interrupt mask: 1 = interrupt not masked at sync lost (pin 58) 0 = interrupt masked.at sync lost (pin 58)
GPSW	General purpose switch at bit RTIN = 1: 0 = pin 57 LOW; 1 = pin 57 HIGH
SRSN	Software reset: 0 = no reset; 1 = reset (see reset procedure)
Index "09" BAME	Burst amplitude indication: 0..= burst amplitude measurement is overridden; colour lock always assumed 1 = burst amplitude is used to control the CLCK status bit, recommended for reference signal without subcarrier burst (pure black and white) in order to avoid PLL hunting.

MPKC1 to MPKC0	Multi-purpose key control: At MKP = LOW (pin 32) are all functions as given by software programming; MKP = HIGH sets in real-time with respect to PDn(7-0).

Set by bits MPKC1	MPKC0	in function blocks input formatter	CLUTs	matrix	level matching
0	0	control via CCIR bit and FMT bits	bypass	control via FMT bits	control via CCIR bit
0	1	Format 5 (RGB) CCIR level	active, no indexed colour	active	CCIR level
1	X	Format 7 (indexed colour) CCIR level	active, indexed colour	active	CCIR level

IEPI	Polarity of external PAL-ID signal (H/2 signal) from RTCI input (pin 57): 0 = not inverted; 1 = inverted
RTSC	Real-time select control: 0 = Real-time control HPLL increment is selected, that means, information about actual clock frequency from the digital colour decoder is received (SAA7151B or SAA7191B); the corresponding subcarrier frequency is calculated. 1 = Real-time control FSC increment with PAL-ID is selected, that means, information about actual subcarrier frequency and PAL-ID from the digital colour decoder is received (SAA7151B or SAA7191B).
RTIN	Select real-time control input: 0 = pin 57 is input for RTCI signal 1 = pin 57 is port output GPSW.
RTCE	Real-time control enabled: 0 = disabled; 1 = enabled (RTIN = 0)
Index "0C" CHPS7 to CHPS0	Phase adjustment between chrominance output signal and reference: 00 to FF equals 0^{o} to 358.59375^{o} in steps of 1.40625^{o}.
Index "0D" FSC7 to FSC0	Fine adjustment of subcarrier frequency in non-GENLOCK modes: 00 to 7F increasing and FF to 80 decreasing equal approximately $\pm 450 \times 10^{-6}$ of the subcarrier frequency in 256 steps.
Index "0E" CLCK	Lock to external chrominance (to be read): 0 = possible; 1 = not possible.

STD3 to STD0	Colour encoding standards:

STD3	STD2	STD1	STD0	standard
0	0	0	0	NTSC 4.43; 60 Hz; SQP (12.27 MHz)
0	0	0	1	NTSC 4.43; 50 Hz; SQP (14.75 MHz)
0	0	1	0	PAL-B/G 4.43; 50 Hz; SQP (14.75 MHz)
0	0	1	1	NTSC 4.43; 60 Hz; CCIR (13.5 MHz)
0	1	0	0	NTSC 4.43; 50 Hz; CCIR (13.5 MHz)
0	1	0	1	PAL-B/G 4.43; 50 Hz; CCIR (13.5 MHz)
0	1	1	0	reserved
0	1	1	1	reserved
1	0	0	0	PAL-M; 60 Hz; SQP (12.27 MHz)
1	0	0	1	PAL-M; 60 Hz; CCIR (13.5 MHz)
1	0	1	0	PAL-N; 50 Hz; CCIR (13.5 MHz)
1	0	1	1	PAL-N; 50 Hz; SQP (14.75 MHz)
1	1	0	0	NTSC-M; 60 Hz; SQP (12.27 MHz)
1	1	0	1	NTSC-M; 60 Hz; CCIR (13.5 MHz)
1	1	1	0	reserved
1	1	1	1	reserved

Status bits to be read via I²C-bus:	Table 7
Status bits to be read by microcontroller :	All registers from 00 up to 0F can be read via MPU-bus. Read-only bits are OEF, HCLK (index "04") and CLCK (index "0E")

Note to Table 6

Field blanking (Figures 11 and 12): normally, video to be encoded should not become active after the active edge of VSN or CSYN before line 22.5 at 50 Hz (line 18 at 60 Hz). Total internal field blanking is 11 lines at 50 Hz (13 lines at 60 Hz).

Colour look-up tables (CLUTs)

The CLUTs consist of RAM tables. The RAM tables can be loaded – with X = 0 to 255 according to equation 1 – for the signals R, G and B . Gamma-correction (pre-distortion) by following equation:

$$Y = \mathrm{NINT}(b + a \times X1^{1/g}); \quad Y(X \leq 16) = 16; \quad Y(X \geq 235) = 235 \quad \text{(equation 1)}$$

with g = 2.2 is

$$a = 219 / (235^{-2.2} - 16^{-2.2})$$

$$b = 16 - a \times 16^{-2.2}$$

The RAM tables are loaded via MPU-bus or via I²C-bus (Table 8).

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1011 000X**
A = acknowledge, generated by the slave
SUBADDRESS* = subadress byte (Table 8)
DATA = data byte (Table 5)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 7 I²C-bus status byte (address byte "B1")

FUNCTION		STATUS BYTE D7	D6	D5	D4	D3	D2	D1	D0
Read status		0	0	0	0	FFOS	OEF	CLCK	HLCK

Function of the bits:
FFOS first field of sequence: 0 = false; 1 = first of 4 fields for NTSC (first of 8 fields for PAL). FFOS is not valid for non-interlaced signals.
OEF field organization: 0 = even field; 1 = odd field
CLCK possibility of lock to external chrominance: 0 = possible; 1 = not possible
HLCK sync indication: 0 = locked to external sync; 1 = external sync lost.

Table 8 I²C-bus write bytes (address byte "B0")

ACCESS TO CONTROL REGISTERS Address byte "B0" — subaddress byte "02" — index byte (00 to 0F, Table 5) — data bytes (auto-increment)
ACCESS TO CLUTS REGISTERS Address byte "B0" — subaddress byte "00" — CLUT address bytes (00 to FF) — 3 data bytes for one RGB sequence (auto-increment)

Table 9 Four different modes

STAND-ALONE MODE The SAA7199B receives a line-locked clock CLKIN and generates CSYN or HSN/VSN output signals, which trigger the RGB respectively the YUV source signal to provide data and composite blanking CBN.
SLAVE MODE The SAA7199B receives the line-locked clock CLKIN, CSYN or HSN/VSN, CBN and data from an RGB respectively YUV source. The sync inputs are edge-sensitive; the minimum active length is 1 PIXCLK. Optionally, a real-time control signal RTCI is received from a digital colour decoder.
GENLOCK MODE Horizontal and vertical sync as well as colour are locked on a received CVBS reference signal. The CVBS reference signal generates also a line-locked clock by the SAA7197 clock generator. Auxiliary signals HCL and HSY as well as CSYN or HSN/VSN are generated to trigger the RGB respectively the YUV source providing data and composite blanking CBN.
TEST MODE Like stand-alone mode, but data to be encoded are the contents of the test registers TRER, TREGand TREB. VSN/CSYN and HSN outputs are in 3-state condition.

Relationship between horizontal frequency and colour subcarrier frequency in non-GENLOCK mode

a) Internal subcarrier frequency with n = integer:

PAL: $f_{SC} = f_H (n/4 + 1/625)$ respectively $f_H (n/4 + 1/525)$ NTSC: $f_{SC} = f_H (n/2)$

Necessary conditions: Non-GENLOCK mode; RTCE = 0, FSCO = 00h; phase coupling of the two frequencies is given by definite phase reset every 8th fields at PAL (4th fields at NTSC).

FSCO $\neq$ 00h adjusts the subcarrier frequency, phase reset is disabled and phase between f_{SC} and f_H is not constant.

b) External subcarrier frequency:

f_{SC} is given by RTCI real-time input from a digital colour decoder.

Necessary conditions: Slave mode; RTCE = 1, RTSC = 1. The 8th respectively 4th field reset is enabled at FSCO = 00h (disabled at FSCO $\neq$ 00h). The subcarrier frequency itself is not influenced by FSCO bits, it is given by real-time increment.

c) External HPLL increment:

f_{SC} is calculated by means of RTCI real-time input signal from a digital colour decoder. The frequency of f_{SC} depends on the absolute crystal frequency value used by the digital colour decoder.

Necessary conditions: Slave mode; RTCE = 1, RTSC = 0. The 8th respectively 4th field reset is enabled at FSCO = 00h (disabled at FSCO $\neq$ 00). The subcarrier frequency itself is influenced by FSCO bits.

The absolute phase relationship between sync and subcarrier (colour burst out) can be influenced in all three cases by CHPS(7-0) register byte (index "0C").

Data input formats

One clock cycle equals 12.27 MHz, 13.5 MHz or 14.75 MHz (Cb = (B-Y) equals U; Cr = (R-Y) equals V; (n) = number of pixel).

Table 10 Format 0: DMSD2-compatible YUV 4:1:1 format (FMT-bits in index "00"= 000)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	Cb5(0)	Cb3(0)	Cb1(0)	Cb7(4)	Cb5(4)	Cb3(4)	Cb1(4)
PD3(6)	Cb6(0)	Cb4(0)	Cb2(0)	Cb0(0)	Cb6(4)	Cb4(4)	Cb2(4)	Cb0(4)
PD3(5)	Cr7(0)	Cr5(0)	Cr3(0)	Cr1(0)	Cr7(4)	Cr5(4)	Cr3(4)	Cr1(4)
PD3(4)	Cr6(0)	Cr4(0)	Cr2(0)	Cr0(0)	Cr6(4)	Cr4(4)	Cr2(4)	Cr0(4)
PD3(3-0)	not used							
PD1(7-0)	not used							

Table 11 Format 1: Customized YUV 4:1:1 format (FMT-bits in index "00" = 001)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	-	Cr7(0)	-	Cb7(4)	-	Cr7(4)	-
PD3(6)	Cb6(0)	-	Cr6(0)	-	Cb6(4)	-	Cr6(4)	-
PD3(5)	Cb5(0)	-	Cr5(0)	-	Cb5(4)	-	Cr5(4)	-
PD3(4)	Cb4(0)	-	Cr4(0)	-	Cb4(4)	-	Cr4(4)	-
PD3(3)	Cb3(0)	-	Cr3(0)	-	Cb3(4)	-	Cr3(4)	-
PD3(2)	Cb2(0)	-	Cr2(0)	-	Cb2(4)	-	Cr2(4)	-
PD3(1)	Cb1(0)	-	Cr1(0)	-	Cb1(4)	-	Cr1(4)	-
PD3(0)	Cb0(0)	-	Cr0(0)	-	Cb0(4)	-	Cr0(4)	-
PD1(7-0)	not used							

Table 12 Format 2: DMSD2-compatible YUV 4:2:2 format (FMT-bits in index "00" = 010)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	Cr7(0)	Cb7(2)	Cr7(2)	Cb7(4)	Cr7(4)	Cb7(6)	Cr7(6)
PD3(6)	Cb6(0)	Cr6(0)	Cb6(2)	Cr6(2)	Cb6(4)	Cr6(4)	Cb6(6)	Cr6(6)
PD3(5)	Cb5(0)	Cr5(0)	Cb5(2)	Cr5(2)	Cb5(4)	Cr5(4)	Cb5(6)	Cr5(6)
PD3(4)	Cb4(0)	Cr4(0)	Cb4(2)	Cr4(2)	Cb4(4)	Cr4(4)	Cb4(6)	Cr4(6)
PD3(3)	Cb3(0)	Cr3(0)	Cb3(2)	Cr3(2)	Cb3(4)	Cr3(4)	Cb3(6)	Cr3(6)
PD3(2)	Cb2(0)	Cr2(0)	Cb2(2)	Cr2(2)	Cb2(4)	Cr2(4)	Cb2(6)	Cr2(6)
PD3(1)	Cb1(0)	Cr1(0)	Cb1(2)	Cr1(2)	Cb1(4)	Cr1(4)	Cb1(6)	Cr1(6)
PD3(0)	Cb0(0)	Cr0(0)	Cb0(2)	Cr0(2)	Cb0(4)	Cr0(4)	Cb0(6)	Cr0(6)
PD1(7-0)	not used							

Table 13 Format 3: Customized YUV 4:2:2 format (FMT-bits in index "00" = 011)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7-0)	Cb (0)	-	Cb (2)	-	Cb (4)	-	Cb (6)	-
PD1(7-0)	Cr (0)	-	Cr (2)	-	Cr (4)	-	Cr (6)	-

Table 14 Format 4: YUV 4:4:4 format (FMT-bits in index "00" = 100)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7-0)	Cb (0)	Cb (1)	Cb (2)	Cb (3)	Cb (4)	Cb (5)	Cb (6)	Cb (7)
PD1(7-0)	Cr (0)	Cr (1)	Cr (2)	Cr (3)	Cr (4)	Cr (5)	Cr (6)	Cr (7)

Table 15 Format 5: RGB 4:4:4 format (FMT-bits in index "00" = 101)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD1(7-0)	R(0)	R(1)	R(2)	R(3)	R(4)	R(5)	R(6)	R(7)
PD2(7-0)	G(0)	G(1)	G(2)	G(3)	G(4)	G(5)	G(6)	G(7)
PD3(7-0)	B(0)	B(1)	B(2)	B(3)	B(4)	B(5)	B(6)	B(7)

Table 16 Format 7: Indexed colour format (FMT-bits in index "00" = 111). Input codes 0 to 255 are allowed, output code of CLUTs should preferably be the same as given in Format 5

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	INC(0)	INC(1)	INC(2)	INC(3)	INC(4)	INC(5)	INC(6)	INC(7)

Table 17 Input data levels for formats 0 to 4 and 5; EBU colour bar: 100 % white equals 100 IRE intensity; 75 % colour saturation for formats 1 to 4, 100 % for format 5

INPUT CHANNEL	LEVEL	DIGITAL LEVEL	CODE	CCIR-BIT	FORMAT
Y channel	0 IRE 100 IRE	12 230	offset binary	0	formats 0 to 4
Cb channel	bottom peak colourless top peak	−101 0 100	two's complement	0	formats 0 to 4
Cr channel	bottom peak colourless top peak	−106 0 105	two's complement	0	formats 0 to 4
Y channel	0 IRE 100 IRE	16 235	offset binary	1	formats 0 to 4
Cb channel	bottom peak colourless top peak	44 128 212	offset binary	1	formats 0 to 4
Cr channel	bottom peak colourless top peak	44 128 212	offset binary	1	formats 0 to 4
R, G and B	0 IRE 100 IRE	16 235	offset binary	1	format 5

GENLOCK input data

Table 18 Format 7: CVBS GENLOCK input data format has 8-bit word length. The input data come from an analog-to-digital converter (TDA8708) with gain-controlled and clamped CVBS or VBS signals

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
CVBS7 to CVBS0	CVBS(0)	CVBS(1)	CVBS(2)	CVBS(3)	CVBS(4)	CVBS(5)	CVBS(6)	CVBS(7)

CONDITIONS OF CVBS INPUT SIGNAL	TWO'S COMPLEMENT REPRESENTATION	
sync bottom	coresponding to binary code	−128
0 IRE (black)	coresponding to binary code	−64*
100 IRE (white)	coresponding to binary code	95
top peak of 75 % colour	coresponding to binary code	95
bottom peak of 75 % colour	coresponding to binary code	−100

* If exactly matched levels are wanted in the internal multiplexer, the value 0 IRE should correspond to −68 and 100 IRE to 82.

Encoding data levels

Input data levels are transformed in three stages:

- in the matrix when RGB or indexed colour is applied (formats 5 and 7)
- in the normalizing amplifier depending on 50/60 Hz mode and CCIR-bit (index "00")
- in the modulator

Table 19(a) Y and C output levels in **50 Hz** mode (PAL) for RGB input levels (100/100 colour bar)

SIGNAL	INPUT DATA			MATRIX OUTPUT DATA			NORMALIZER OUTPUT DATA			MODULATOR OUTPUT DATA	
	R	G	B	(R-Y)	Y	(B-Y)	V*	Y	U	Y	C**
white	235	235	235	128	235	128	0	421	0	421	0
yellow	235	235	16	146	210	16	29	387	−132	387	±135
cyan	16	235	235	16	170	166	−184	332	44	332	±189
green	16	235	16	34	145	54	−155	297	−87	297	±178
magenta	235	16	235	221	107	202	152	245	86	245	±175
red	235	16	16	240	82	90	183	211	−45	211	±188
blue	16	16	235	110	41	240	−30	154	131	154	±134
black	16	16	16	128	16	128	0	120	0	120	0
blanking	X	X	X	X	X	X	X	X	X	120	0
burst	X	X	X	X	X	X	45	X	−45	X	±63
top sync	X	X	X	X	X	X	X	X	X	0	X

Table 19(b) Y and C output levels in **60 Hz** mode (NTSC) for RGB input levels (100/100 colour bar)

SIGNAL	INPUT DATA			MATRIX OUTPUT DATA			NORMALIZER OUTPUT DATA			MODULATOR OUTPUT DATA	
	R	G	B	(R-Y)	Y	(B-Y)	V	Y	U	Y	C**
white	235	235	235	128	235	128	0	416	0	416	0
yellow	235	235	16	146	210	16	29	385	−132	385	±135
cyan	16	235	235	16	170	166	−184	335	44	335	±189
green	16	235	16	34	145	54	−155	303	−87	303	±178
magenta	235	16	235	221	107	202	152	256	86	256	±175
red	235	16	16	240	82	90	183	225	−45	225	±188
blue	16	16	235	110	41	240	−30	173	131	173	±134
black	16	16	16	128	16	128	0	142	0	142	0
blanking	X	X	X	X	X	X	X	X	X	120	0
burst	X	X	X	X	X	X	0	X	−64	X	±64
top sync	X	X	X	X	X	X	X	X	X	0	X

X = not defined; * the V component is inverted in the PAL line; ** the ± figures are peak values of the subcarrier signal.

Chrominance filtering in the encoder

1. Decimation for 4:4:4 formats input data (Formats 4, 5 and 7; Fig.4).
2. Interpolation for 4:1:1 input data into 4:2:2 data – also suitable to reduce the bandwidth of 4:2:2 data. This filter is controlled by SCBW-bit (SCWB = 1 means active).
3. Interpolation at 13.5 MHz for 4:2:2 input data into 4:4:4 data before modulating baseband signals onto the colour subcarrier. Figures 5, 6 and 7 show the overall transfer characteristics of chrominance in "standard bandwidth condition" (SCBW = 1). Figures 8 and 9 show the overall transfer characteristics of chrominance in "enhanced bandwidth condition" (SCBW = 0), which is not possible for 4:1:1 input data. The transfer curves are slightly different at 12.27 and 14.75 MHz.

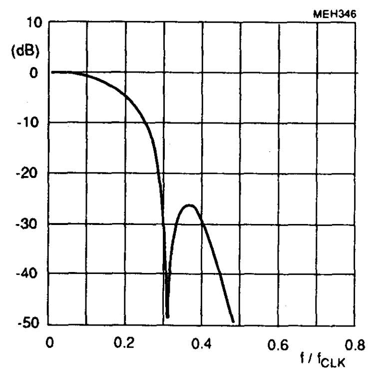


Fig.4 Transfer characteristics of 4:4:4 to 4:2:2 decimator.

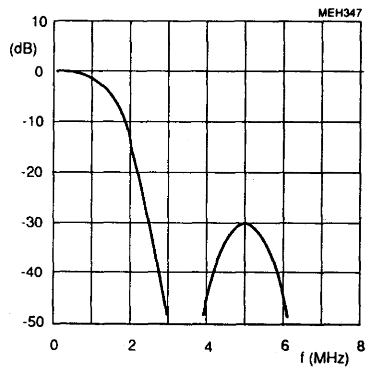


Fig.5 Overall transfer characteristics 4:1:1 input data.

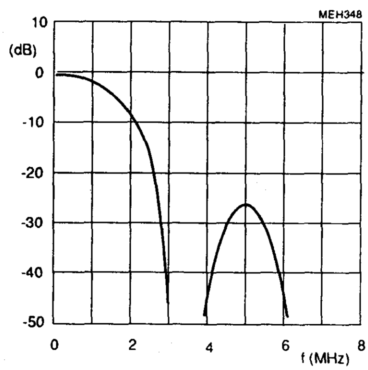


Fig.6 Overall transfer characteristics 4:2:2 input data (SCBW-bit = 1).

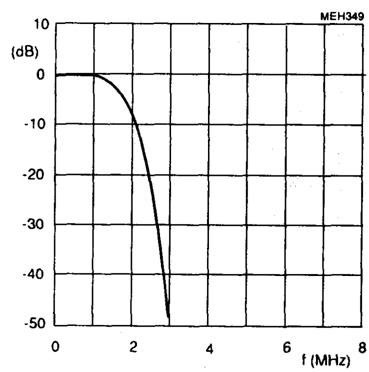


Fig.7 Overall transfer characteristics 4:4:4 input data (SCBW-bit = 1).

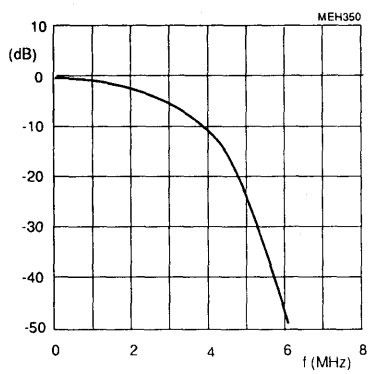


Fig.8 Overall transfer characteristics 4:2:2 input data (SCBW-bit = 0).

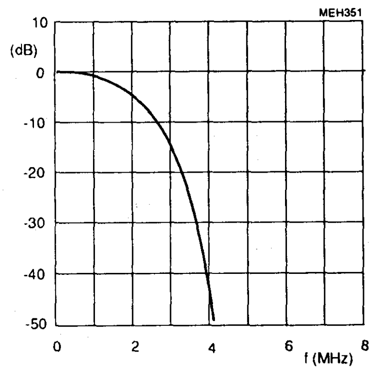


Fig.9 Overall transfer characteristics 4:4:4 input data (SCBW-bit = 0).

Accuracy of matrix

Evaluation of quantization errors.

The RGB to YUV matrix is realized according to the following algorithm:

Y = INT ((NINT(R x 2 x 0.299) + NINT(G x 2 x 0.587) +NINT(B x 2 x 0.114)) / 2)

U = NINT ((B-Y) x 0.57722)

V = NINT ((R-Y) x 0.72955)

Errors can occur in the calculation of Y, which in consequence influence the U and V outputs.
The greatest positive error occurs, if in all of the three for Y calculation used ROMs the values are rounded up to 0.5 LSB, and no truncation error of 0.5 LSB is generated after summation:

(3 x 0,5 LSB) / 2 = +0.75 LSB;
with truncation "error": (3 x 0,5 LSB) / 2 – 0.5 LSB = +0.25 LSB.

The greatest negative error occurs at rounding off in all the three ROMs and by consecutive truncation:

3 x (–0,5 LSB) / 2 – 0.5 LSB = –1.25 LSB.

As a result, the matrix error can be ±1 digit, which corresponds to approximately ±0.5% differential non-linearity.

Estimation of noise by quantization

The sum of all sqared quantization errors is SS normalized to 220^3 input combinations (3-dimensional colour scale).

SS = 0.187545 LSB^2.

Compared with noise energy for ideal quantization, SSI = 1/12 LSB^2 results in a deterioration by the conversion matrix of

D = 10 log (0.187545 x 12) = 3.5 dB (equals 0.5 bit).

If SS is the sum of all sqared quantization errors, normalized to 220 input combinations of a grey-scale (R = G = B), then is
SS = 0.12273 LSB^2.

Compared with noise energy for ideal quantization, SSI = 1/12 LSB^2 results in a deterioration by the conversion matrix of

D = 10 log (0.12273 x 12) = 1.7 dB (equals 0.25 bit).

Normalizing amplifiers in luminance channel

The absolute amplification error for 50 Hz non-set-up signals is 0.375 %; differential non-linearity is −0.333 % (equals −1 LSB).
The absolute amplification error for 60 Hz set-up signals is −1.5 %; differential non-linearity is −0.365 % (equals −1 LSB).

Normalizing amplifiers in chrominance channel

The absolute amplification error is approximately ±0.5 % with a truncation error of −0.5 LSB.

The subcarrier amplitude for standards with luminance set-up is the same as for the standards without luminance set-up.

Modulator

The absolute amplification error is −0.39 %; there is no truncation error.

Functional timing

GENLOCK mode:
The encoded signal can be generated earlier with respect to CVBS(7-0) bits (offset t_{ofs} set by GDC-bits; index "05"). The HSN output signal can be generated early by PSO-bits (index "07") with respect to CBN to compensate for pipelining delay t_{Rint} of the RAM interface (valid also in stand-alone mode).

The horizontal timing is independent of active video at data inputs PDn(7-0). The line blanking period on the outputs is set to approximately 12 µs in 50 Hz standards (11 µs in 60 Hz standards).

Slave mode:
HSN pin is used as an input. The active edge of the input signal is assumed to fit to the incoming CBN signal. Deviations can be compensated in the range of the GCD-bits (index "05").

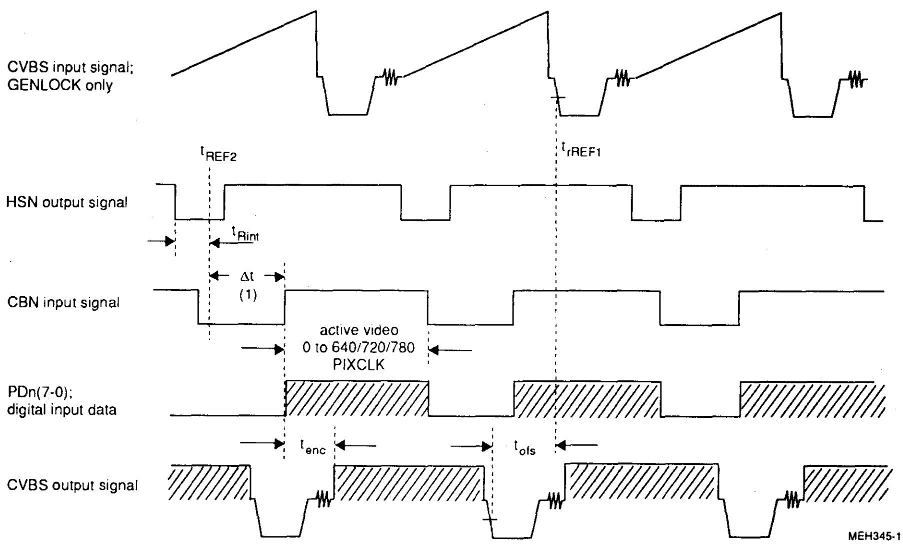


Fig.10 Horizontal timing. t_{Rint} = pipeline delay of RAM interface adjustable from −5 to +58 pixel clocks (PIXCLK); t_{ofs} = propagation delay of external GENLOCK line adjustable from −17 to +46 pixel clocks.

(1) Δt = 125 x PIXCLK at 12.27 MHz
Δt = 163 x PIXCLK at 14.75 MHz
Δt = 134 x PIXCLK at 13.50 MHz / 50 Hz mode
Δt = 122 x PIXCLK at 13.50 MHz / 60 Hz mode

The t_{enc} time is the total delay from data input to analog CVBS output; it is 55 pixel clock periods long (PIXCLK) plus the propagation delay of the LDV input register regardless of mode and colour standard.
The key input signal is delay-compensated with respect to PDn(7-0)data input.
The generated vertical field and burst blanking sequences are shown in Fig.11 (50 Hz PAL) and Fig.12 (60 Hz NTSC).

Reset

Prior to a reset all outputs are undefined. RESN = LOW sets the circuit into the slave mode:
- MOD1 bit = 1; MOD0-bit = 0. All other control register bits are set to zero. The outputs CSYN/VSN, HSN, SLT, HSY and HCL are automatically set to high-impedance state. The I²C-bus interface is set to a slave receiver.

The D(7-0) pins of the MPU interface are inputs during RESN = LOW. As the circuit requires an external clock signal on pin CLKIN in slave mode, the clock select signal CLKSEL (pin 50) must be LOW during RESN = LOW (pin 54). The LOW time of RESN is preliminary at least 50 pixel clock periods long.

Disable chip

All analog outputs are set to zero by DD-bit = 1 (index "08"); while the outputs CSYN/VSN, HSN, HCL, HSY and SLT are set to high-impedance state. The internal clock is divided by 4 at DD-bit = 1.
The circuit can be disabled for any reason. It must be disabled when CLKIN exceeds 32 MHz. After setting DD-bit = 1, the CLKIN input signal can be set to a frequency of < 60 MHz (modification of control registers and RAM tables is not ensured).
To enable the circuit again, CLKIN must be set to a frequency < 32 MHz, a reset (hardware) then is required to set DD-bit to zero.

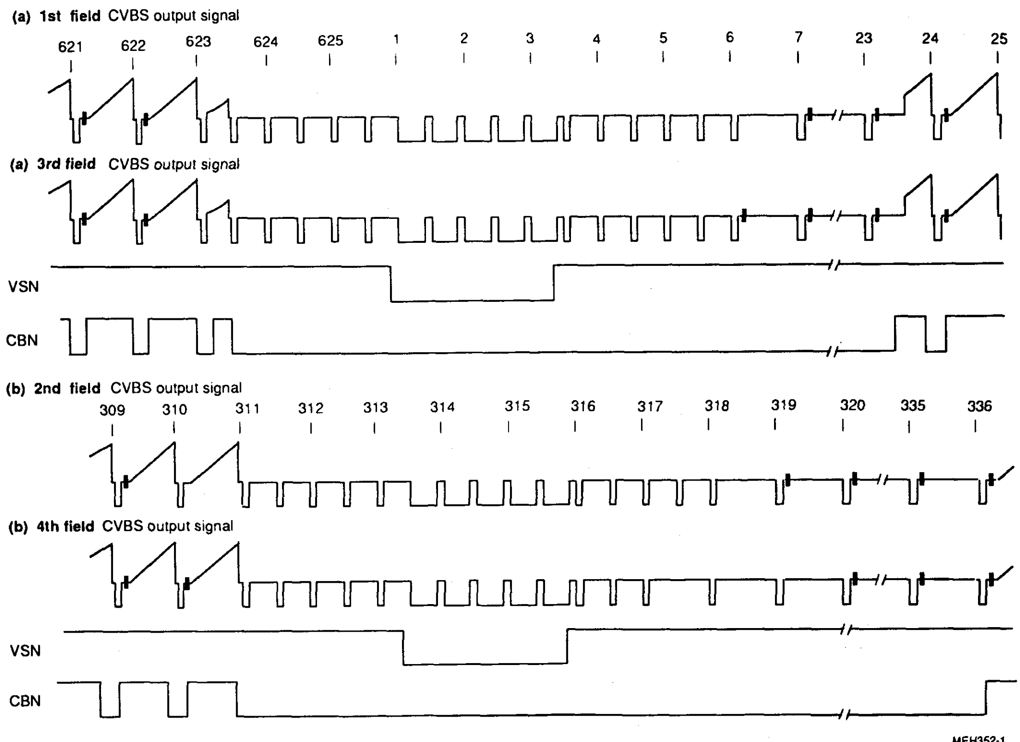


Fig.11 Vertical field and burst blanking sequence for PAL 50 Hz mode.

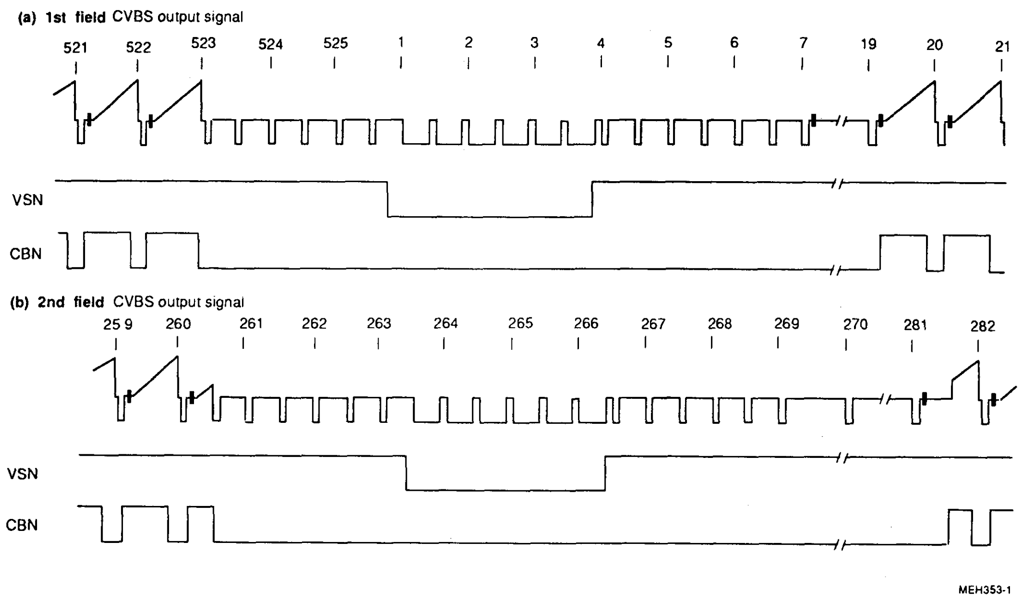


Fig.12 Vertical field and burst blanking sequence for NTSC 60 Hz mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD1}	supply voltage (pin 2)	−0.3	7	V
V_{DDD2}	supply voltage (pin 21)	−0.3	7	V
V_{DDD3}	supply voltage (pin 41)	−0.3	7	V
V_{DDA1}	supply voltage (pin 66)	−0.3	7	V
V_{DDA2}	supply voltage (pin 70)	−0.3	7	V
V_{DDA3}	supply voltage (pin 72)	−0.3	7	V
V_{DDA4}	supply voltage (pin 64)	−0.3	7	V
$V_{diff\ GND}$	difference voltage between digital and analog ground pins ($V_{DDDn} - V_{DDAn}$)	-	±100	mV
V_n	voltage on all pins, grounds excluded	0	V_P	V
P_{tot}	total power dissipation	-	1.1	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through an 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage range (pins 2, 21 and 42)		4.5	5	5.5	V
V_{DDA}	analog supply voltage range (pins 66, 70 and 72)		4.75	5	5.25	V
I_{DDD}	digital supply current I_{DDD1} to I_{DDD3}	40 pF output load	-	-	140	mA
I_{DDA}	analog supply current I_{DDA1} to I_{DDA3}	40 pF output load	-	-	60	mA
Data and control inputs (pins 3 to 20, 23 to 40, 43 to 46, 49, 50, 54 to 56, 59, 73 and 76 to 84)						
V_{IL}	input voltage LOW	note 1	0	-	0.8	V
V_{IH}	input voltage HIGH	note 1	2.0	-	V_{DDD}+ 0.5	V
I_{LI}	input leakage current		-	-	±1	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_I	input capacitance	data inputs	-	-	8	pF
		CLKIN, LLC, LDV	-	-	10	pF
		3-state I/O	-	-	10	pF
LFCO output (pin 61)						
V_o	output signal (peak-to-peak value)		1.4	-	2.6	V
V_{61}	output voltage range		0	-	V_{DDD}	V
Data and other control outputs (pins 3, 51, 52, 57, 58, 60, 74 and 75)						
V_{OL}	output voltage LOW	note 2	0	-	0.6	V
V_{OH}	output voltage HIGH	note 2	2.4	-	V_{DDD}	V
C, Y and CVBS analog outputs (pins 65, 67 and 69)						
V_o	output signal (peak-to-peak value)	without load; V_{DDA} = 5 V	-	2	-	V
$V_{65,67,69}$	minimum output voltage	without load; V_{DDA} = 5 V	-	0.2	-	V
	maximum output voltage	without load; V_{DDA} = 5 V	-	2.2	-	V
$R_{65,67,69}$	internal serial output resistance	not tested	18	25	35	Ω
$R_{L\ 65,67,69}$	output load resistance	recommendation	90	-	-	Ω
B	output signal bandwidth	-3 dB	10	-	-	MHz
ILE	LF integral linearity error	9-bit data	-	-	±1.0	LSB
DLE	LF differential linearity error	9-bit data	-	-	±0.5	LSB
I_{CUR}	input current (pin 71)	Fig.1; $R_{70\text{-}71}$ = 20 kΩ	-	300	-	μA
I^2C-bus SDA and SCL (pins 47 and 48)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3.0	-	V_{DDD}+0.5	V
I_I	input current	V_I = LOW or HIGH	-	-	±10	μA
V_{OL}	SDA output voltage (pin 47)	I_{47} = 3 mA	-	-	0.4	V
I_{47}	output current	during acknowledge	3	-	-	mA
Crystal oscillator		Fig.14				
f_n	nominal frequency	3rd harmonic; Table 1	-	24.576	-	MHz
		3rd harmonic; Table 1	-	26.8	-	MHz
$\Delta f / f_n$	permissible deviation f_n		-	50	-	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	-	70	°C
	load capacitance C_L		8	-	-	pF
	series resonance resistance R_S		-	40	80	Ω
	motional capacitance C_1		-	1.5±20%	-	fF
	parallel capacitance C_0		-	3.5±20%	-	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LLC and LDV timing (pins 55 and 20)		Fig.16				
t_{LLC}	cycle time	note 3	31.5	-	44.5	ns
t_{CH}	pulse width		40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
t_{LDV}	cycle time		63	-	89	ns
t_{SUL}	LDV set-up time		4	-	-	ns
t_{HDL}	LDV hold time		10	-	-	ns
PIXCLK and CLKO timing (pins 51 and 52)		Fig.16				
t_{DCK}	PIXCLK and CLKO delay time		-	-	25	ns
PD1(7-0), PD2(7-0), PD3(7-0), CBN, MPK, KEY and RTCI input timing (pins 4 to 19, 23 to 32, 57 and 73)						
t_{SUD}	input data set-up time	Fig.16	4	-	-	ns
t_{HDD}	input data hold time		6	-	-	ns
CVBS (7-0), VSN/CSYN and HSN timing (pins 76 to 83, 3 and 84)						
t_{SU}	input data set-up time	Fig.17	10	-	-	ns
t_{HD}	input data hold time		5	-	-	ns
CREF timing (pin 56)		Fig.17				
t_{SUC}	input set-up time		10	-	-	ns
t_{HDC}	input hold time		2	-	-	ns
MPU timing A1, A0, R/WN, CSN, D(7-0) (pins 33 to 36, 37 to 40 and 43 to 46); Fig.18						
t_{SA}	A1 and A0 address set-up time (pins 33, 34)		4	-	-	ns
t_{HA}	A1 and A0 address hold time		25	-	-	ns
t_{SR}	R/WN set-up time (pin 35)		4	-	-	ns
t_{HR}	R/WN hold time		25	-	-	ns
t_{CL} ,t_{CH}	CSN pulse width LOW and HIGH	note 4	95	-	-	ns
t_{SW}	data set-up time (D7 to D0)	write	80	-	-	ns
t_{HW}	data hold time (D7 to D0)	write	5	-	-	ns
t_{HDR}	data output hold time (D7 to D0)	read	5	-	-	ns
t_{ZR}	delay to driven ports (D7 to D0)	read	5	-	-	ns
t_{DR}	delay to ports valid (D7 to D0)	read; note 5	-	-	275	ns
t_{RZ}	port outputs disable time (D7 to D0)	read	-	-	25	ns
Output timing (pins 3, 74, 75 and 84)		Fig.17				
t_{OD}	output delay time	minimum clock period; note 6	-	20	40	ns

Notes to the characteristics

1. XTAL, XTALI and TP are not characterized with respect to levels; CLKO is characterized up to 32 MHz and PIXCLK up to 16 MHz
2. Levels are measured with load circuit. LFCO output with 10 kΩ in parallel to 15 pF and other outputs with 1.2 kΩ in parallel to 40 pF at 3V (TTL load).
3. t_{LLC} has to be in the range 63 to 89 ns at CREF = HIGH (pin 56); t_{LLC} = 16.5 ns is allowed only if the multiplexer clock is active.
4. $t_{PIXCLK(min)} + 5$ ns.
5. 3 x ($t_{PIXCLK(min)}$ + 5 ns).
6. 40 ns at low supply voltage (4 V) and high temperature (70 °C).

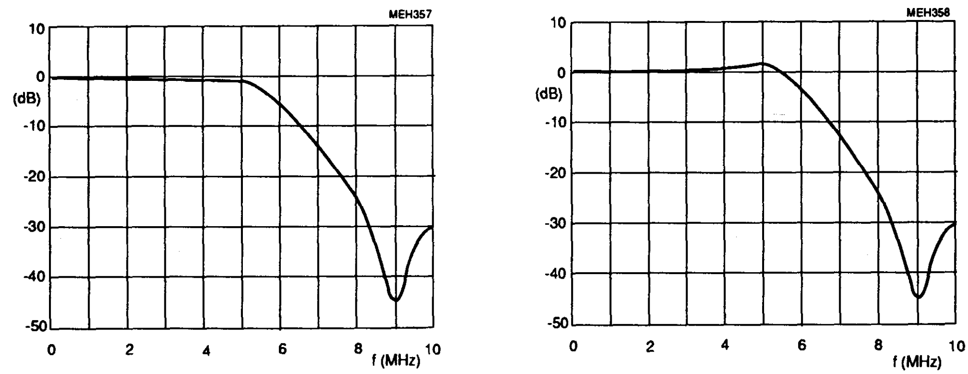


Fig.13 Characteristics of low-pass post-filters. Left: without compensation of DC hold characteristic. Right: with compensation of DC hold characteristic.

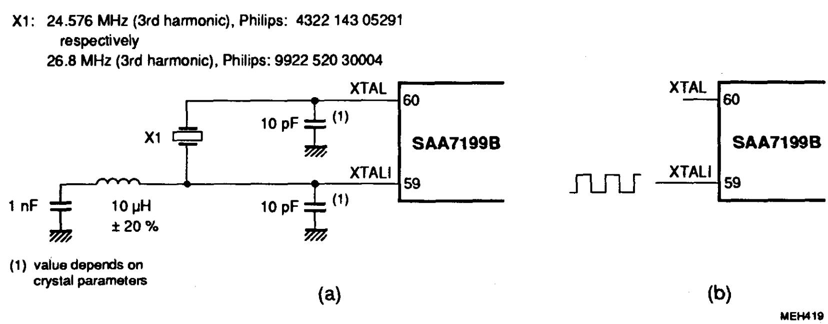
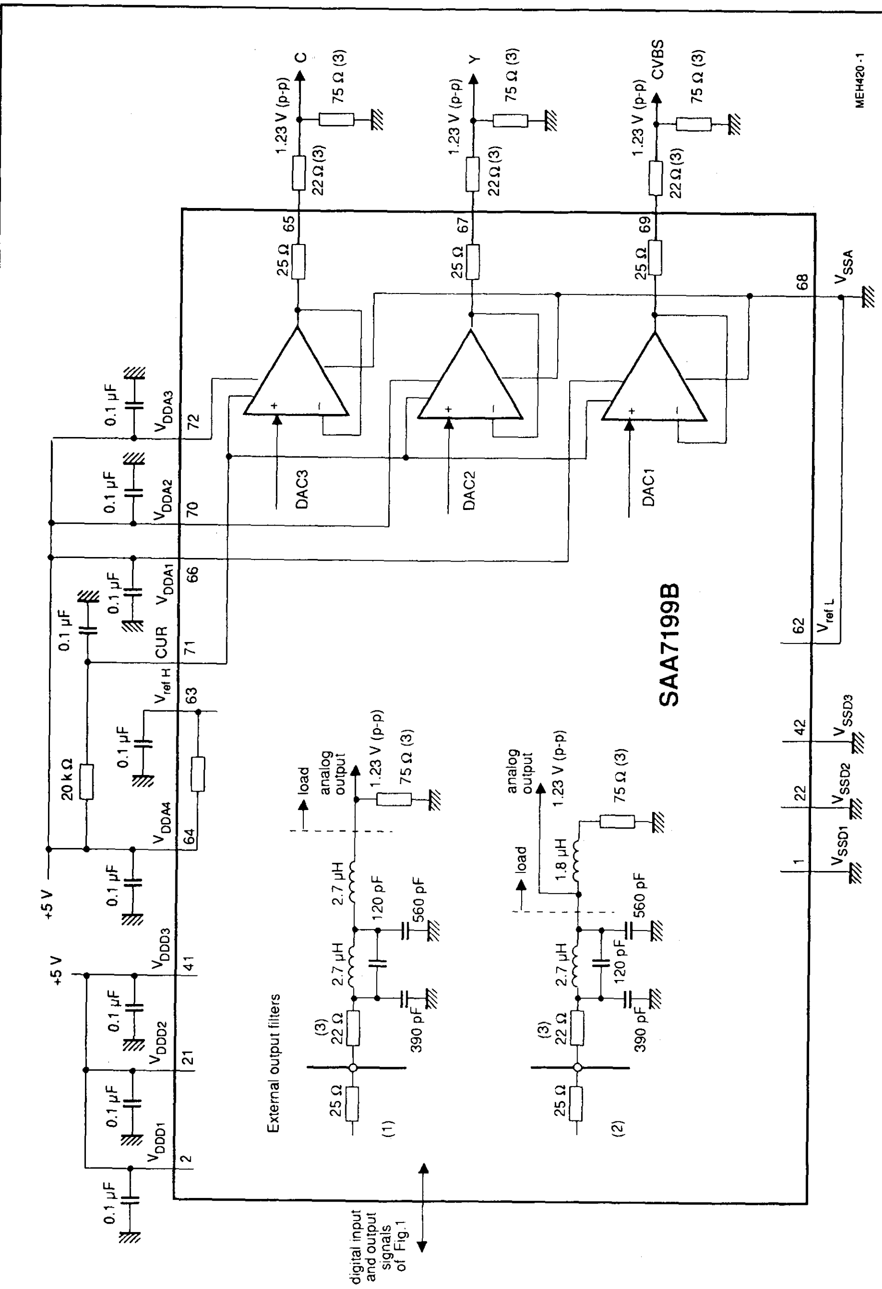


Fig.14 Oscillator application (a) and optional external clock sync (b).



(1) without compensation of the DAC hold characteristic (Fig.14).

(2) with compensation of the DAC hold characteristic (sin(x)/ x correction, Fig.14).

(3) output amplitude determined by load resistors $R_L > 90\ \Omega$.

Fig.15 Application details due to Fig.1. Proposals of analog low-pass post-filtering of output signals.

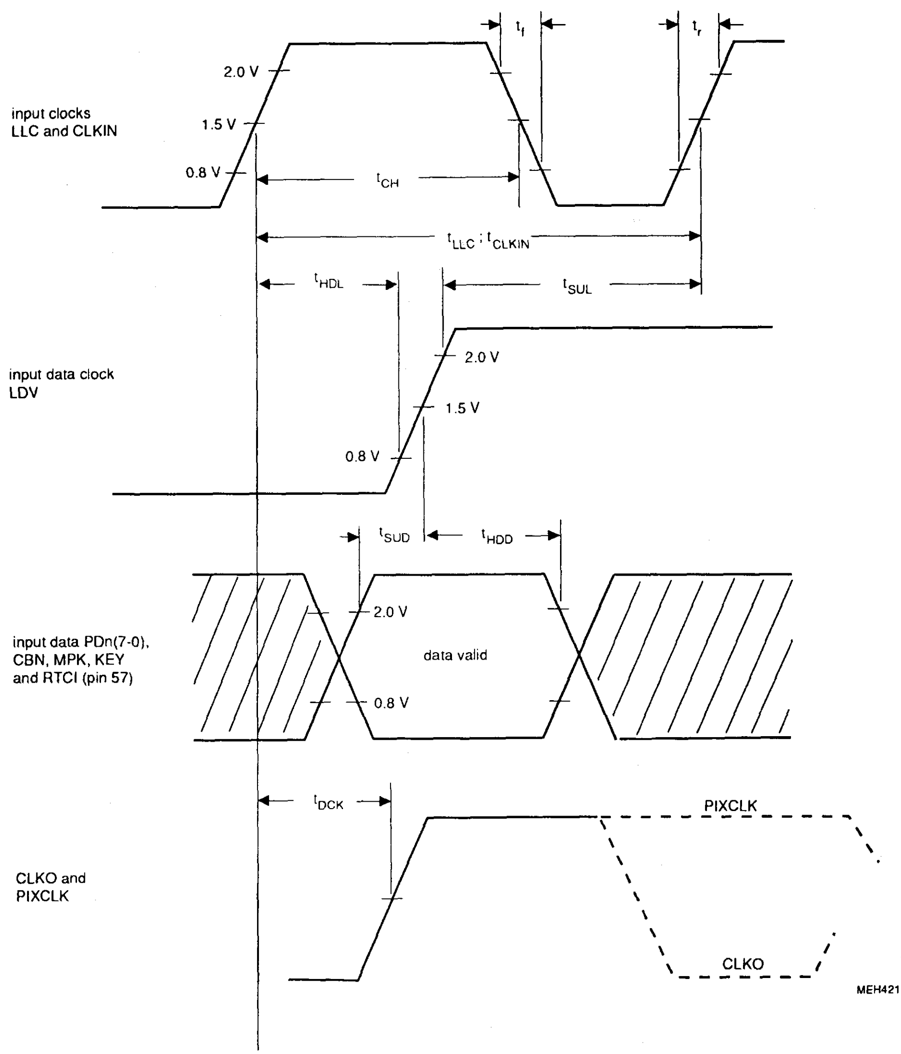


Fig.16 LDV input data timing.

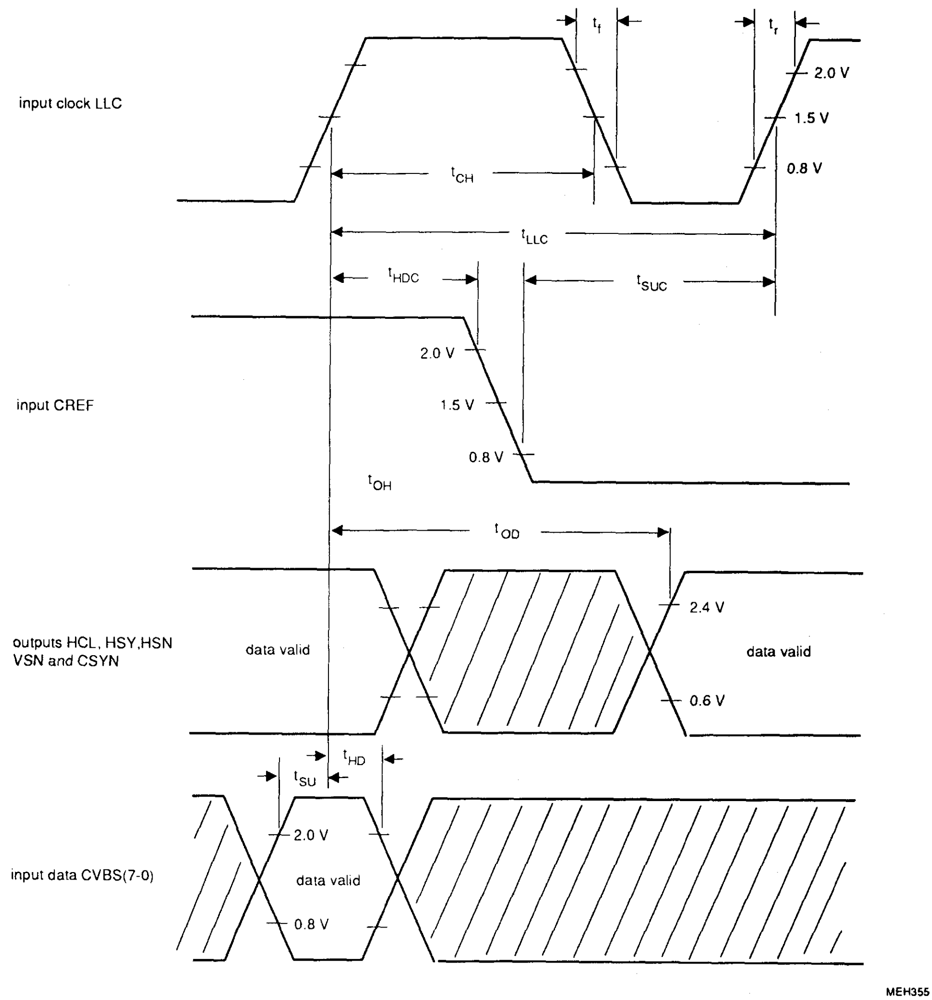


Fig.17 Clock and data timing.

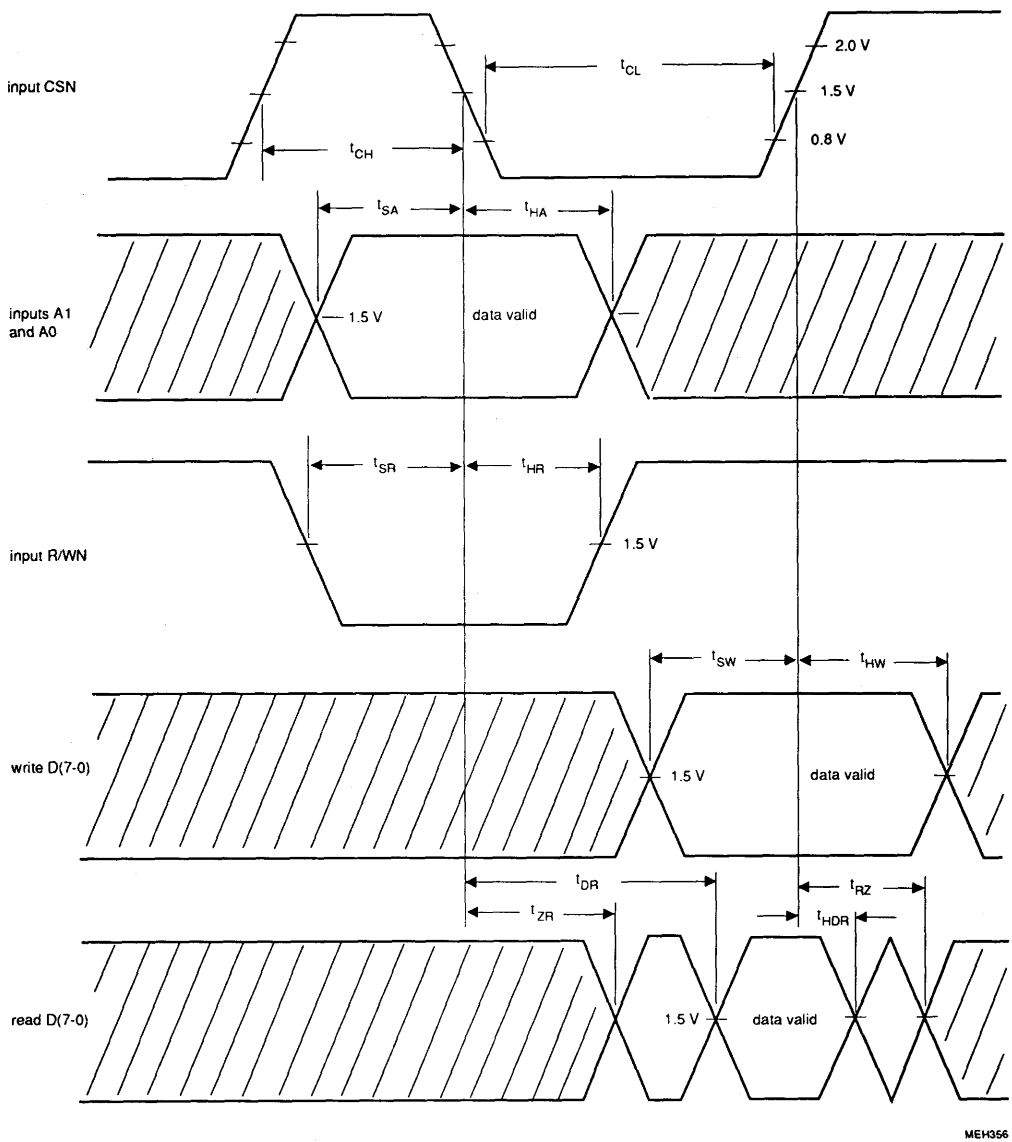


Fig.18 MPU-bus timing.

12. UPDATE HISTORY

DATE OF ISSUE	UPDATES COMPARED TO PREVIOUS VERSION PAGE	CHANGES
April 1992	25	LIMITING VALUES new line $V_{diff\ GND}$ = maximum ±100 mV
October 1992	1	Additional feature: "Line 21 data insertion possible"
	5	HSN description (pin 84)
	8	Formatting corrected (between tables)
	11	IDEL7 to IDEL 0: Table 5, data "43" hex recommended.
	13	Note to Table 6 corrected.
	14	FFOS: an new status bit
	15	Text: Relationship between... corrected a), b) and c).
	26	minimum and maximum output voltages on pins 65, 67 and 69 are typical values
	27	t_{SUL}, t_{HDL}, t_{HDR} t_{DR}, and t_{OD} corrected.
	28	Note 6 added.
April 1993	29	hold times for lines PD1, PD2..... and for CVBS ..... have been changed.

Digital multistandard TV decoder SAA9051

FEATURES

- All operations based on a sampling frequency of 13.5 MHz, providing:
  - full adaptability to all transmission standards
  - capability for memory-based features
- Separate chrominance and luminance input (Y/C)
- CVBS input for standard applications
- CVBS throughput capability for SECAM application
- Luminance signal processing for all TV standards (PAL, NTSC, SECAM, B/W)
- Horizontal and vertical synchronization detection for all standards
- Chrominance signal processing for all quadrature amplitude modulated colour-carrier signals
- Requires only one crystal
- Controlled via the I^{2}C-bus
- User-programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Cross-colour reduction by chrominance comb-filter (NTSC)
- Wide range hue control

GENERAL DESCRIPTION

The SAA9051 digital multistandard decoder (S-DMSD) performs demodulation and decoding of all quadrature modulated colour TV standards, as well as performing luminance processing for all TV standards with CVBS or Y/C input signals.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9051	68	PLCC	plastic	SOT188AGA, CG

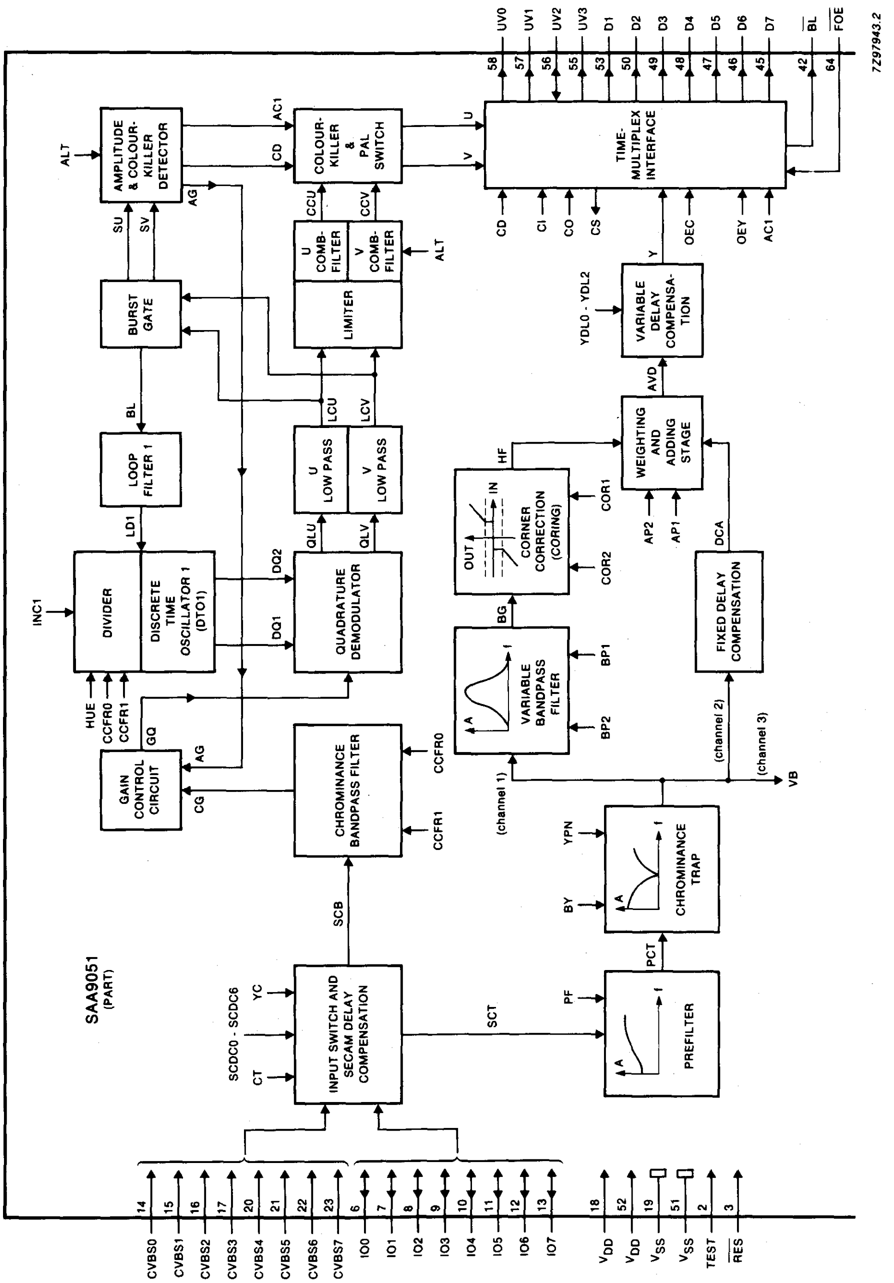


Fig.1 Block diagram; continued in Fig.2

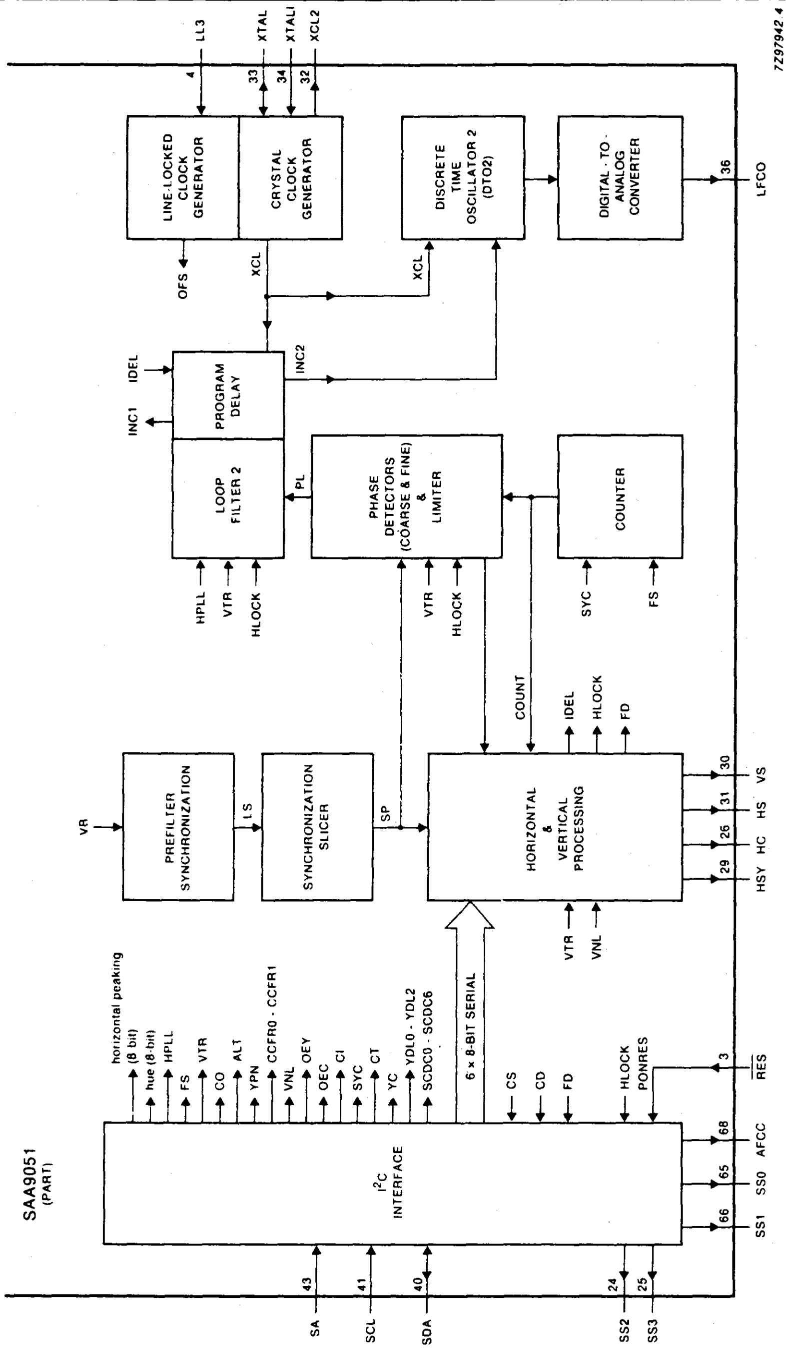


Fig.2 Block diagram; from Fig.1

Digital multistandard TV decoder SAA9051

PIN CONFIGURATION

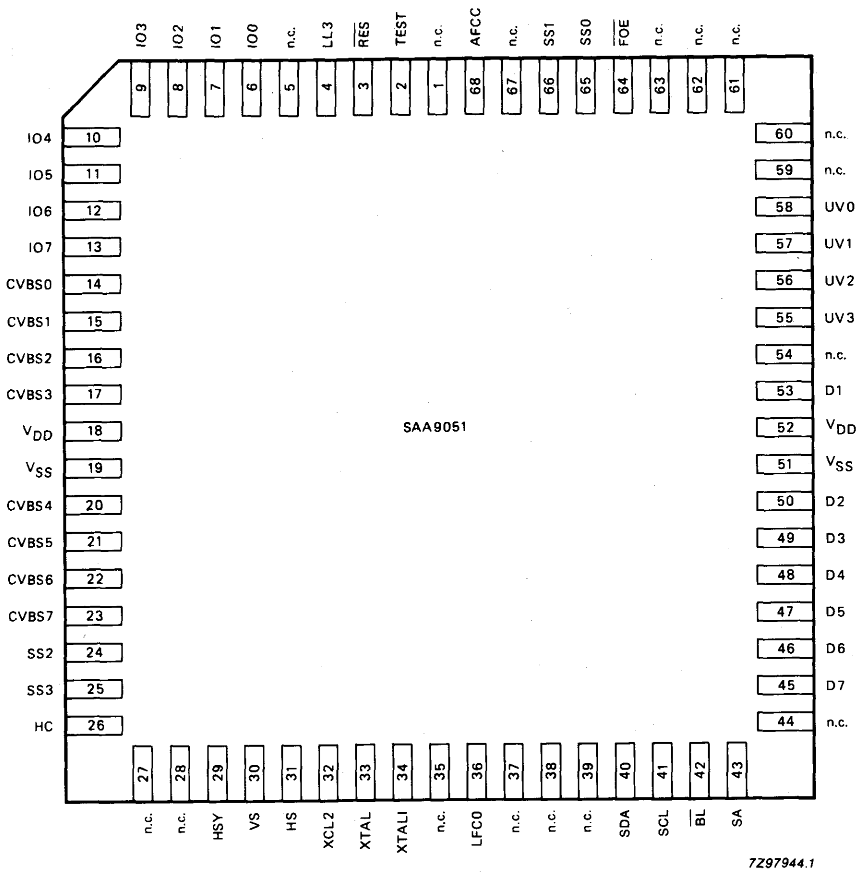


Fig.3 Pinning configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
TEST	2	test input (active HIGH); when HIGH enables scan-test mode, always connected to ground
$\overline{RES}$	3	reset input (active LOW); results in the I²C-bus control registers 1 to 3 and internal stages being reset during the reset phase. The minimum LOW period of $\overline{RES}$ is 120 LL3 clock cycles
LL3	4	13.5 MHz line-locked system clock
n.c.	5	not connected
IO0 (LSB) - IO7 (MSB)	6 - 13	bidirectional data path; chrominance input for separate luminance and chrominance input (Y/C) or CVBS output for SECAM decoder SAA9056. Two's complement format (IO0 is only used internally for CVBS throughput)
CVBS0 (LSB) - CVBS7 (MSB)	14 - 17, 20 - 23	digitalized composite video blanking and synchronization signals; containing luminance, chrominance and all synchronization information or luminance, blanking and synchronization signals in the event of separate luminance and chrominance (Y/C) input. Two's complement format (CVBS0 is only used internally for CVBS throughput)
V_{DD}	18	positive supply voltage (+5 V)
V_{SS}	19	ground (0 V)
SS2 - SS3	24 - 25	source select output signals; I²C-bus controlled, TTL compatible switches
HC	26	programmable horizontal output pulse; when used in conjunction with input circuits (e.g. ADC) indicates the black-level position before analog-to-digital conversion. The start and stop times are programmable, between −9.4 µs and +9.5 µs in steps of 74 ns, via the I²C-bus
n.c.	27 - 28	not connected
HSY	29	programmable horizontal output pulse; when used in conjunction with input circuits (e.g. an ADC). It indicates the synchronization pulse position before analog-to-digital conversion The start and stop times are programmable, between −14.2 µs and +4.7 µs in steps of 74 ns, via the I²C-bus
VS	30	vertical synchronization output; indicates the vertical position of the picture for 50/60 Hz field frequency

PINNING (continued)

SYMBOL	PIN	DESCRIPTION
HS	31	horizontal synchronization pulse output (duration = 64 LL3 clock cycles). HS is programmable, between −32 μs and +32 μs in steps of 300 ns, via the I²C-bus
XCL2	32	clock output; half of the crystal clock frequency (12.288 MHz). In phase with crystal (pin 33)
XTAL	33	crystal oscillator input/inverting amplifier output; input to the internal clock generator from an external oscillator or output of the inverting amplifier to an external crystal (24.576 MHz)
XTALI	34	input to the inverting amplifier from an external crystal (24.576 MHz); connect to ground if an external oscillator is used
n.c.	35	not connected
LFCO	36	line frequency control; analog output representing a multiple of the line frequency (6.75 MHz) with 4-bit resolution, the phase of which is compared to the system clock by the CGC (SAA9057A)
n.c.	37 - 39	not connected
SDA	40	I²C-bus serial data input/output
SCL	41	I²C-bus serial clock input
$\overline{BL}$	42	blanking signal output (active LOW); indicates the active video and line blanking periods. $\overline{BL}$ also synchronizes the data multiplexers/demultiplexers
SA	43	I²C-bus select address; input for selection of the appropriate I²C-bus slave address
D7 (MSB) - D1 (LSB)	45 - 50, 53	luminance data output
V_{SS}	51	ground (0 V)
V_{DD}	52	positive supply voltage (+5 V)
n.c.	54	not connected
UV3 - UV0	55 - 58	multiplexed PAL or NTSC colour difference signal output or SECAM CS input signal from the SECAM decoder. Output data format is two's complement. The multiplexer is synchronized to the rising-edge of $\overline{BL}$
n.c.	59 - 63	not connected
$\overline{FOE}$	64	fast output enable signal (active LOW); sets D1 - D7 and UV0 - UV3 outputs to the HIGH-impedance Z-state
SS0 - SS1	65 - 66	source select output signals, set via the I²C-bus; used to control the input switch (e.g. TDA8708)
n.c.	67	not connected
AFCC	68	additional output for circuit control; activated via the I²C-bus

FUNCTIONAL DESCRIPTION (see Fig.1)

The S-DMSD performs the demodulation and decoding for all quadrature modulated colour TV standards (PAL-B, G, H, I, M, N, NTSC 4.43 MHz and NTSC-M), as well as performing luminance, and parts of the synchronization, processing for TV standards (PAL, NTSC and SECAM). All of the controllable functions, user as well as factory adjustments, are accessed via I²C-bus thereby enhancing the adaptability of the digital TV concept.

Operation is based on a line-locked sampling frequency of 13.5 MHz, thus making the system fully adaptable to all line frequencies. Only one crystal is required for all TV standards.

The S-DMSD is designed to operate in conjunction with the SAA9057A Clock Generating Circuit (CGC). If the CGC is not utilized the designer must ensure:

- a reset pulse is applied to the S-DMSD after a power failure

Y/C processing

In the Y/C mode:

- The chrominance signal is input at the IO port (IO0 - IO7) and transmitted via the input switch/SECAM delay compensation circuit (multiplexer) to the chrominance bandpass filter, 'see section Chrominance path'.
- The other components, Y signal and synchronization pulse, are input via inputs CVBS0 - CVBS7 and transmitted via the input switch/SECAM delay compensation circuit to the luminance prefilter.

CVBS processing

In the CVBS mode:

- The CVBS signal is separated into its luminance (VBS) and chrominance (CG) parts by the chrominance trap and bandpass circuits. These circuits can be switched by the standard identification signals (CCFR0, CCFR1/YPN) according to the detected colour-carrier frequency, 3.58 MHz or 4.43 MHz.
- On reception of a SECAM signal the signal is transmitted to the SECAM decoder (SAA9056) via the IO port (IO0 - IO7). Bit CT enables the 3-state buffer between both parts.

Luminance path

After the chrominance trap stage (see Fig.1), the luminance path is separated into three Channels as follows:

CHANNEL 1 SIGNAL

The Channel 1 signal is transmitted to the programmable bandpass filter where the high luminance frequencies are removed (centre frequency is programmable via bits BP1 and BP2). The BC signal is transmitted to the coring (corner correction) stage where low amplitude noise is removed (amount of low amplitude noise removal is programmable via bits COR1 and COR2). The HF signal is transmitted to the weighting and adding stage, see section 'Combining Channel 1 and Channel 2 signals'.

CHANNEL 2 SIGNAL

The Channel 2 signal is transmitted to the fixed delay compensation stage where delay compensation and black-level adjustment occurs. The DCA signal is transmitted to the weighting and adding stage, see section 'Combining Channel 1 and Channel 2 signals'.

COMBINING CHANNEL 1 AND CHANNEL 2 SIGNALS

The Channel 1 HF signal is weighted and added to the Channel 2 DCA signal. The combined signals are matched to the specified amplitude and the word size is reduced to 7 bits. The AVD signal is transmitted to the variable delay compensation stage where compensation for IF group delays occurs, the amount of delay is programmable (from −4 to +3 LL3 clock cycles, see note) via bits YDL0 - YDL2. The Y signal is transmitted to the time multiplexed interface where the signal is output via D1 - D7.

CHANNEL 3 SIGNAL

The Channel 3 VB signal is transmitted to the prefilter synchronization stage, see section 'Synchronization path'.

Note

Differences in the delay compensation required for PAL and NTSC are catered for by identification signal YPN which switches the chrominance trap to the appropriate colour-carrier frequency 3.58 MHz or 4.43 MHz.

Chrominance path (see Fig.1)

The chrominance CG signal is transmitted from the chrominance bandpass stage to the gain control circuit (see note 1). The gain control stage ensures that the chrominance signal has constant burst amplitude. The GQ signal is transmitted to the quadrature demodulator, where demodulation of the quadrature modulated chrominance GQ signal to colour difference signals occurs.

The QLU and QLV signals are transmitted to a low-pass filter. The LCU and LCV signals are transmitted to the limiter and comb-filter stage. The comb-filter stage (see note 2) separates the remaining vertically correlated luminance components for NTSC (for PAL, the signals are phase corrected). The CCU and CCV signals are transmitted to the colour-killer and PAL switch stage (see note 3). At this stage signals which do not comply with the selected standard are removed. In the PAL mode this stage restores the correct phase of the V signal. The signals are then transmitted to the time multiplexed interface and output via UV0 - UV3.

Notes

1. The gain control stage is controlled by the AG signal which is derived from the amplitude and colour-killer detector stage (ACKD). A non-standard burst-to-amplitude ratio results in the automatic colour-leveling stage functioning as an amplitude detector to ensure correct amplitude and avoid overflow/limiter defects.
2. The comb-filter can be altered from alternate to non-alternate mode by the ALT signal.
3. The colour-killer and PAL switching stages are controlled by the amplitude and colour-killer detection circuit using the AC1 and CD signals.

COLOUR-CARRIER FREQUENCY REGENERATION

The regeneration of the colour-carrier frequency is performed by the phase-locked-loop (PLL) which comprises a quadrature demodulator, low-pass filter, burst gate, loop filter 1 and divider/discrete time oscillator (DTO1). The DTO1 is controlled by the standard identification signals CCFR0 - CCFR1 and the Hue signal which influences the demodulation phase of the chrominance signal.

Synchronization path

In the synchronization circuit, prefilter synchronization is implemented to normalize the synchronization pulse slopes. A synchronization-slicer provides the detected synchronization pulses (SP) to the horizontal and vertical processing and phase detector stages.

HORIZONTAL AND VERTICAL PROCESSING

The horizontal and vertical processing comprises part of a PLL circuit for regeneration of the horizontal synchronization (HS) and an adaptive filter for detection of the vertical synchronization (VS). The horizontal and vertical processing also generates:

- coincidence signal (HLOCK) which controls the mute function
- standard identification signal (FD) which identifies nominal 525 or 625 lines per picture.

PHASE DETECTORS

The phase detectors that receive the SP signal, also part of the PLL, control the generation of the line-locked clock (PL). Loop filter 2, which has a variable bandwidth, dependent on the time constant signal (VTR), generates two increment signals (INC1 and INC2) with different delays. INC2 is programmable via the increment delay signal (IDEL). INC1 corrects the regenerated subcarrier frequency at DTO1 and INC2 performs phase incrementing of DTO2. The crystal clock generator provides a stable 24.576 MHz clock input to DTO2 which in turn supplies the 4-bit DAC with a digital control signal of 432 or 429 times the line frequency. The analog output LFCO, from the DAC, is transmitted to the SAA9057A (CGC).

Output interface

The signals OEY, OEC, CO, CI and CD control the output interface (see Fig.6). All but one of these signals are received via the I²C-bus, except the CD signal which is detected in the S-DMSD. A power-ON reset results in these signals being set to zero.

Table 1 Vertical Noise limiter (VNL) signal

VNL	OUTPUT
0	VNL bypassed
1	VNL active

Table 2 CO, CI and CD signals

CO	CI	CD	OUTPUTS	OUTPUT STATUS
0	X	X	UV0 - UV3	colour OFF (zero)
1	0	0	UV0 - UV3	colour OFF (controlled by CD)
1	0	1	UV0 - UV3	colour ON (controlled by CD)
1	1	X	UV0 - UV3	colour forced ON

Where:

X = don't care.

Table 3 OEC, OEY, $\overline{FOE}$, $\overline{BL}$, D1 - D7 and UV0 - UV3 signals

OEC	OEY	$\overline{FOE}$	$\overline{BL}$, VS, HS	D1 - D7	UV0 - UV3	REMARKS
0	0	X	HIZS	HIZS	HIZS	status after power-ON reset
1	1	1	active	HIZS	HIZS	
1	1	0	active	active	active	
0	1	1	active	HIZS	HIZS	
0	1	0	active	active	active	

Where:

X = don't care
HIZS = HIGH-impedance Z-state.

Note to Table 3

Combinations other than those shown in Table 3 are not allowed.

$\overline{FOE}$ signal

In PIPCO (picture-in-picture controller, SAA9068) applications, the PIPCO requires access to the digital YUV-bus on a pixel time-base. This requirement is catered for by PIPCO generated signal $\overline{FOE}$, which forces all data output of the S-DMSD and DSD (SAA9056) into the HIGH-impedance Z-state. The $\overline{FOE}$ signal does not affect the synchronization data lines (HS and VS) or the blanking data line ($\overline{BL}$), see Fig.7.

CS signal

The CS signal is transmitted from the digital SECAM decoder (DSD) during the horizontal-blanking period and is received via the UV2 input (see Fig.6). The CS bit is read by the S-DMSD once per line at LL3 clock cycle number 748 (see Fig.8).

I²C bus interface (see Tables 1 to 3)

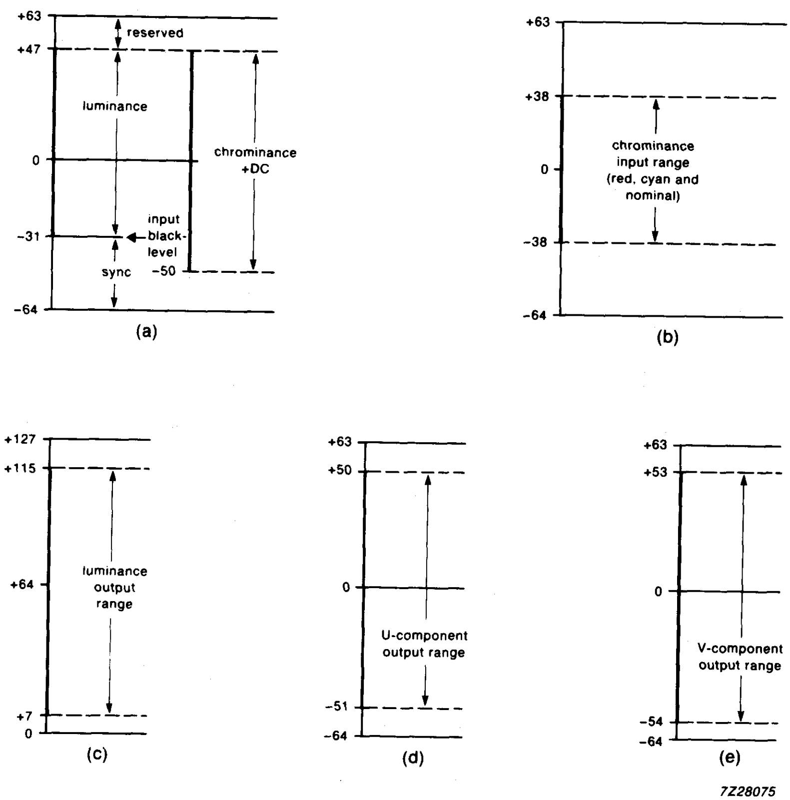
The following control signals are received via the I²C bus interface:

- standard identification signals (CCFR0, CCFR1, ALT, FS, YPN)
- video recorder/TV time constant (VTR)
- hue control (HUE)
- delay programming of the horizontal signals (HS, HC, HSY)

- increment-delay (IDEL)
- luminance aperture-correction control (BY, PF, BP1, BP2, COR2, COR1, AP2, AP1)
- luminance delay compensation (YDL0, YDL1, YDL2)
- fixed clock generation command (HPLL)
- internal colour ON/OFF (CO)
- internal colour forced ON, test purposes only (CI)
- vertical noise limiter (VNL) active/bypassed
- luminance and sync output enable (OEY)
- chrominance output enable (OEC)
- switch signals (source select signals SS0, SS1, SS2, SS3)
- additional output for circuit control (AFCC)
- chrominance source select CVBS/chrominance input/output (CT/YC).
- SECAM chrominance delay compensation (SCDC0, SCDC1, SCDC2, SCDC3, SCDC4, SCDC5, SCDC6).
- horizontal sync (HSY) and clamp (HC) pulse disable (SYC).

Signals transmitted from the S-DMSD via the I^2C bus are:

- standard identification signals (FD, CS)
- colour-killer status signal (CD)
- coincidence information (HLOCK)
- power-on-reset of S-DMSD (PONRES).



(a) CVBS1 to CVBS7 input range

(b) IO1 to IO7 input range

(c) Y output range

(d) U output range (B–Y)

(e) V output range (R–Y)

Fig.4 Diagram showing input/output range of the S-DMSD; all levels in EBU colour bar, values in binary, 100% luminance and 75% chrominance amplitude.

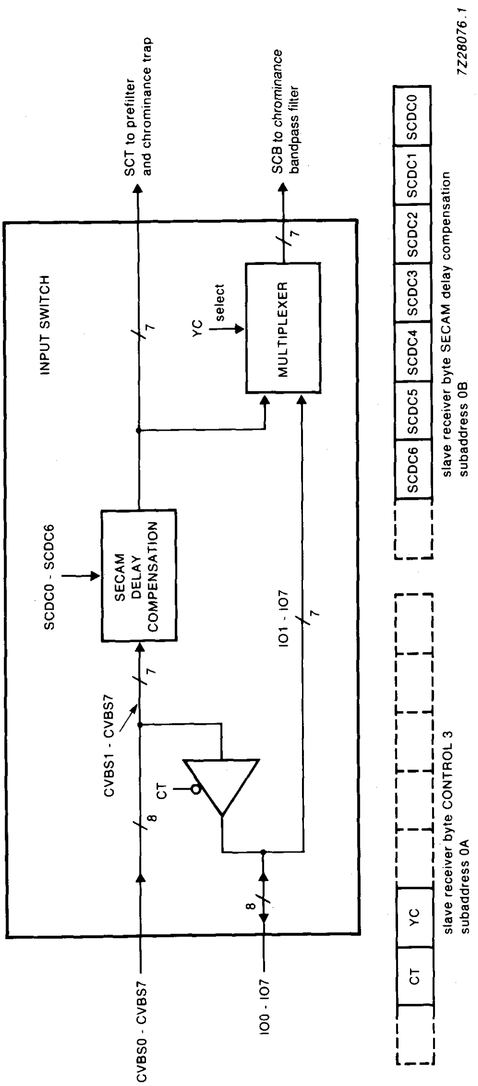


Fig.5 Schematic diagram of the input switch.

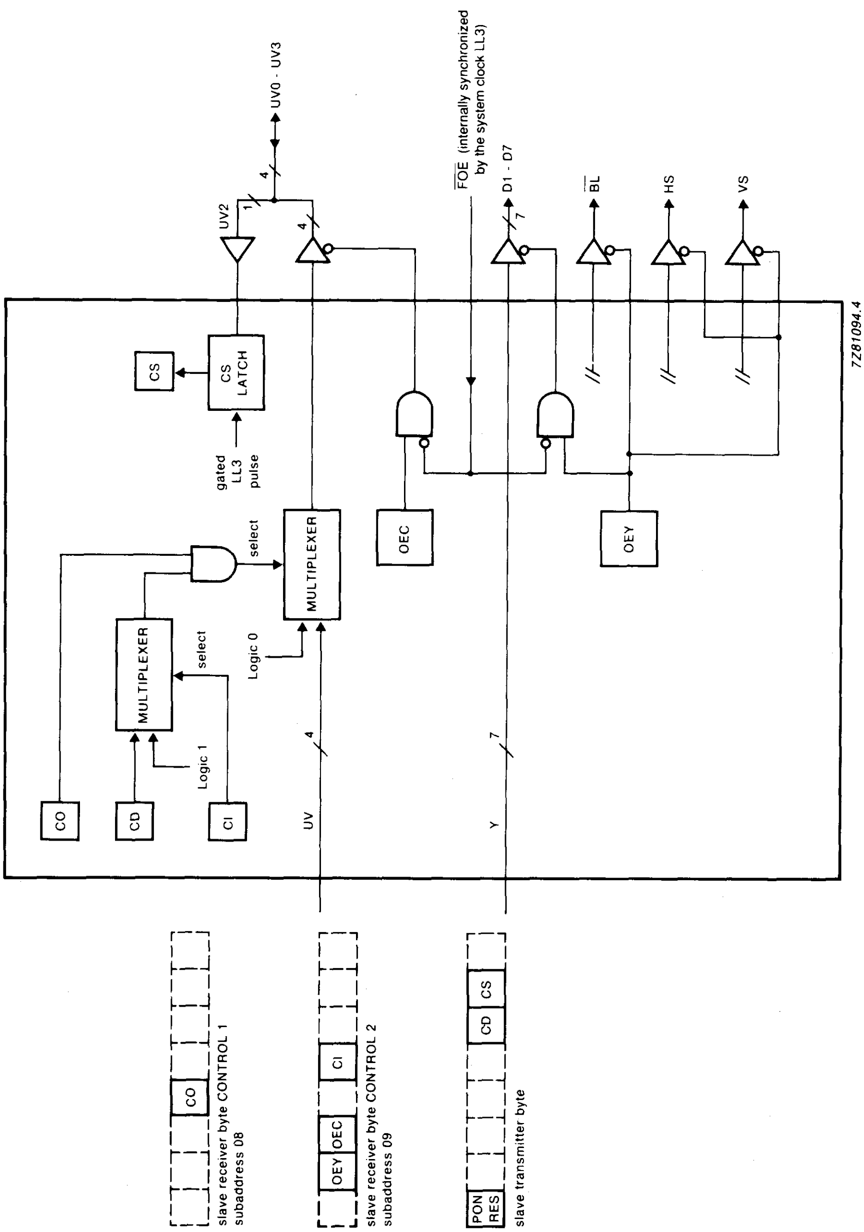


Fig.6 Schematic diagram of control signals at the output interface.

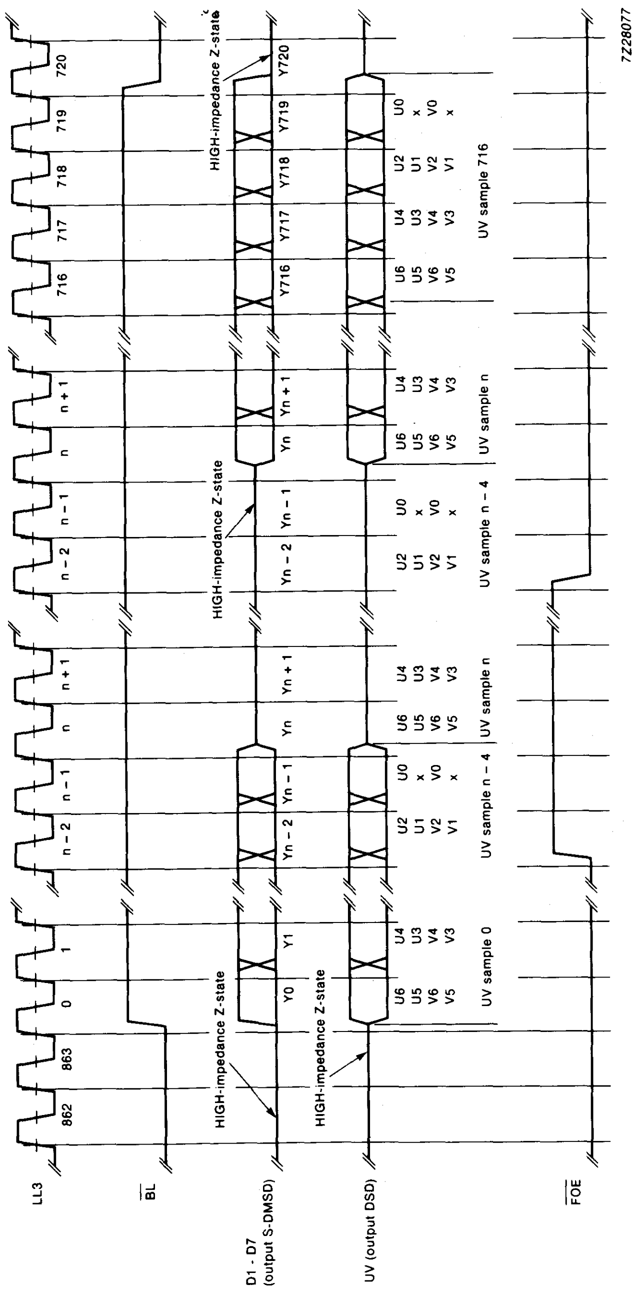
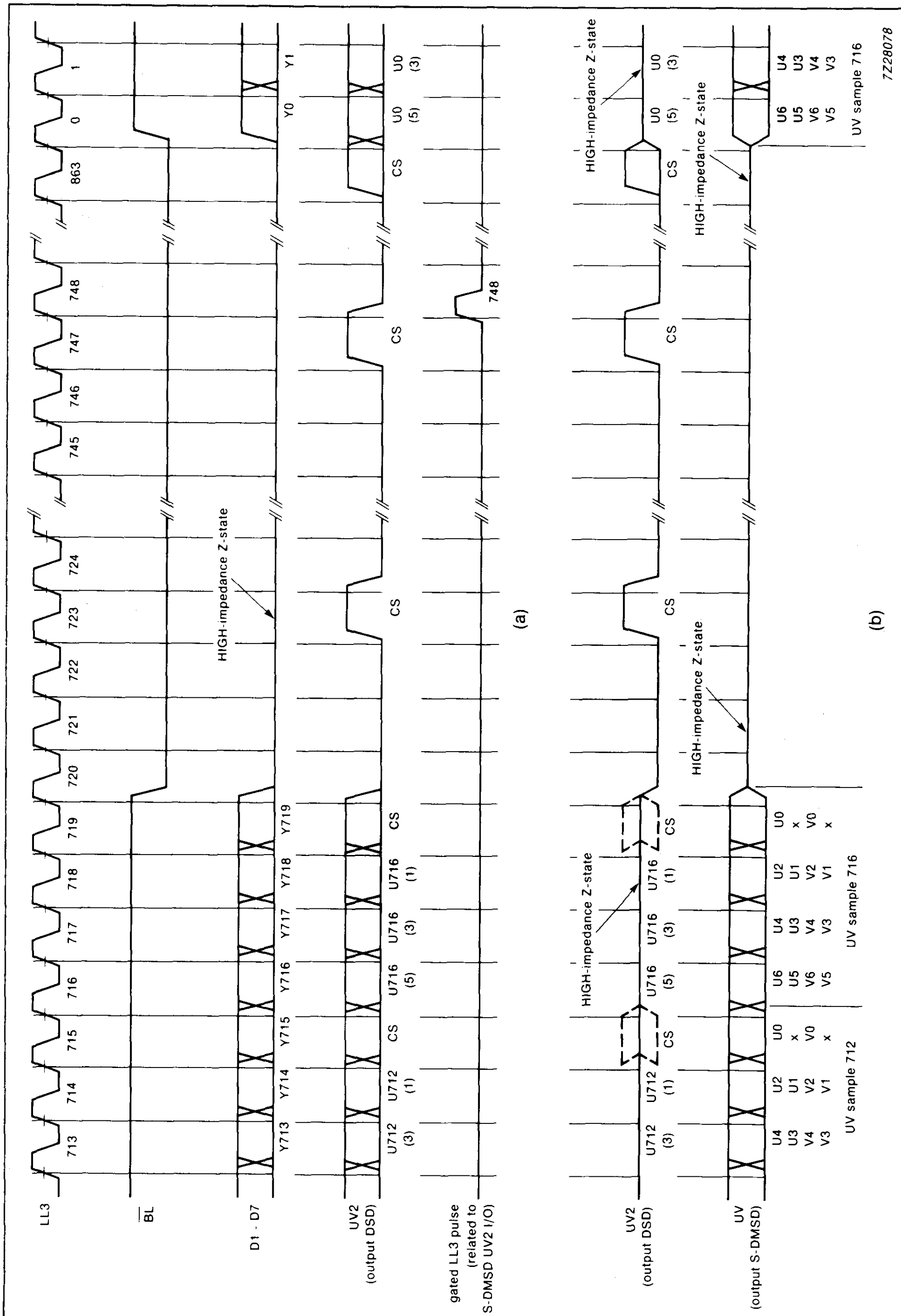


Fig.7 Timing waveform of the output data and $\overline{FOE}$ signals.



(a) SECAM decoder active.
(b) PAL/NTSC decoder active.

Fig.8 Position of the CS signal read by the S-DMSD.

Table 4 Slave addresses

SLAVE RECEIVER ADDRESS									REMARKS
SA	A6	A5	A4	A3	A2	A1	A0	*	
0	1	0	0	0	1	0	1	0	binary value (8A hex)
1	1	0	0	0	1	1	1	0	binary value (8E hex)

Where:

* = logic 0, receiver mode
* = logic 1, transmitter mode.

SLAVE RECEIVER ORGANIZATION

Slave address and receiver format

There are two slave addresses, programmable via input SA, which determine the operating mode of the S-DMSD, see Table 4.

Table 5 Subaddress byte and data byte formats

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Increment delay IDEL	00	A07	A06	A05	A04	A03	A02	A01	A00
HSY start time	01	A17	A16	A15	A14	A13	A12	A11	A10
HSY stop time	02	A27	A26	A25	A24	A23	A22	A21	A20
HC start time	03	A37	A36	A35	A34	A33	A32	A31	A30
HC stop time	04	A47	A46	A45	A44	A43	A42	A41	A40
HS start time (after PHI1)	05	A57	A56	A55	A54	A53	A52	A51	A50
Horizontal peaking	06	BY	PF	BP2	BP1	COR2	COR1	AP2	AP1
Hue control	07	A77	A76	A75	A74	A73	A72	A71	A70
Control 1	08	HPLL	FS	VTR	CO	ALT	YPN	CCFR1	CCFR0
Control 2	09	VNL	OEY	OEC	X	CI	AFCC	SS1	SS0
Control 3	0A	SYC	CT	YC	SS3	SS2	YDL2	YDL1	YDL0
SECAM delay compensation	0B	X	SCDC6	SCDC5	SCDC4	SCDC3	SCDC2	SCDC1	SCDC0
Reserved	0C - 0F	X	X	X	X	X	X	X	X

Where:

X = don't care.

Notes to Table 5

1. The subaddress is automatically incremented. This enables quick initialization, within one transmission, by the I²C-bus controller.
2. The subaddresses shown are acknowledged by the device. Subaddresses 10 to 1F (reserved for the SECAM decoder SAA9056) are not acknowledged. The subaddress counter wraps-around from 1F to 00. Subaddresses 20 to FF are not allowed.
3. After power-on-reset the control registers 1 to 3 (subaddresses 08, 09 and 0A) are, with the exception of bits YDL0 - YDL2 of counter 3, set to logic 0. All other registers are undefined.
4. Prior to a reset of the IC all outputs are undefined.
5. The least significant bit of an analog control or alignment register is defined as AX0.

SUBADDRESS 00

Table 6 Increment delay control IDEL (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/13.5 MHz = 148 ns)	CONTROL BITS*							
		A07	A06	A05	A04	A03	A02	A01	A00
−1	−148 ns (min. value)	1	1	1	1	1	1	1	1
to									
−110	−16.3 μs (outside available range)	1	0	0	1	0	0	1	0
−111	−16.44 μs	1	0	0	1	0	0	0	1
to									
−214	−31.7 μs (max. value if FS = logic 1)	0	0	1	0	1	0	1	0
−215	−31.85 μs (outside central counter range if FS = logic 1)**	0	0	1	0	1	0	0	1
−216	−32 μs (max. value if FS = logic 0)**	0	0	1	0	1	0	0	0
−217	−32.148 μs (outside central counter if FS = logic 0)**	0	0	1	0	0	1	1	1
to									
−256	−37.9 μs (outside central counter)**	0	0	0	0	0	0	0	0

Where:

* A sign bit, designated A08 and internally set to HIGH, indicate values are always negative.

** The horizontal PLL does not operate in this condition. The system clock frequency is set to a value fixed by the last update and is within ± 7.1% of the nominal frequency.

SUBADDRESS 01

Table 7 Horizontal synchronization HSY start time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 1/13.5 MHz = 74 ns)	CONTROL BITS							
		A17	A16	A15	A14	A13	A12	A11	A10
+191	−14.2 µs (max. negative value)	1	0	1	1	1	1	1	1
to									
+1	−0.074 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
−1	+0.074 µs	1	1	1	1	1	1	1	1
to									
−64	+4.7 µs (max. positive value)	1	1	0	0	0	0	0	0

SUBADDRESS 02

Table 8 Horizontal synchronization HSY stop time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 1/13.5 MHz = 74 ns)	CONTROL BITS							
		A27	A26	A25	A24	A23	A22	A21	A20
+191	−14.2 µs (max. negative value)	1	0	1	1	1	1	1	1
to									
+1	−0.074 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
−1	+0.074 µs	1	1	1	1	1	1	1	1
to									
−64	+4.7 µs (max. positive value)	1	1	0	0	0	0	0	0

SUBADDRESS 03

Table 9 Horizontal clamp HC start time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 1/13.5 MHz = 74 ns)	CONTROL BITS							
		A37	A36	A35	A34	A33	A32	A31	A30
+127	−9.4 µs (max. negative value)	0	1	1	1	1	1	1	1
to									
+1	−0.074 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
−1	+0.074 µs	1	1	1	1	1	1	1	1
to									
−128	+9.5 µs (max. positive value)	1	0	0	0	0	0	0	0

SUBADDRESS 04

Table 10 Horizontal clamp HC stop time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 1/13.5 MHz = 74 ns)	CONTROL BITS							
		A47	A46	A45	A44	A43	A42	A41	A40
+127	−9.4 μs (max. negative value)	0	1	1	1	1	1	1	1
to									
+1	−0.074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+0.074 μs	1	1	1	1	1	1	1	1
to									
−128	+9.5 μs (max. positive value)	1	0	0	0	0	0	0	0

SUBADDRESS 05

Table 11 Horizontal synchronization HS start time after PHI1 (application dependent); 50 Hz; 625 lines (FS = 0)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 4/13.5 MHz = 296 ns)	CONTROL BITS							
		A57	A56	A55	A54	A53	A52	A51	A50
+127	forbidden; outside available central counter range	0	1	1	1	1	1	1	1
to									
+109	forbidden; outside available central counter range	0	1	1	0	1	1	0	1
+108	−32 μs (max. negative value)	0	1	1	0	1	1	0	0
to									
+1	−0.296 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+0.296 μs	1	1	1	1	1	1	1	1
to									
−107	+31.7 μs (max. positive value)	1	0	0	1	0	1	0	1
−108	forbidden; outside available central counter range	1	0	0	1	0	1	0	0
to									
−128	forbidden; outside available central counter range	1	0	0	0	0	0	0	0

Table 12 Horizontal synchronization start time after PHI1 (application dependent); 60 Hz; 525 lines (FS = 1)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 4/13.5 MHz = 296 ns)	CONTROL BITS							
		A57	A56	A55	A54	A53	A52	A51	A50
+127	forbidden; outside available central counter range	0	1	1	1	1	1	1	1
to									
+107	forbidden; outside available central counter range	0	1	1	0	1	0	1	1
+106	−31.8 µs (max. negative value)	0	1	1	0	1	0	1	0
to									
+1	−0.294 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
−1	+0.294 µs	1	1	1	1	1	1	1	1
to									
−107	+31.5 µs (max. positive value)	1	0	0	1	0	1	0	1
−108	forbidden; outside available central counter range	1	0	0	1	0	1	0	0
to									
−128	forbidden; outside available central counter range	1	0	0	0	0	0	0	0

Programming IDEL, HSY, HC and HS

The variables IDEL, HSY, HC and HS are programmed using data words via the I²C-bus. In the following examples a decrease in value corresponds to an increase in time.

IDEL (SEE FIG.9)

The IDEL data word compensates for the time delays in data processing between loop filter 2, quadrature demodulator and internal/external (system) signal paths. The internal delay (t_{REF}) is the period required for INC1 to pass from loop filter 2, through the divider and DTO1. This delay corrects the relationship between the subcarrier frequency and the line frequency. The external path is a result of the following time delays (time delay is given in term of LL3 clock cycles):

- t_{IDEL}; programmable delay time
- t_a; processing time of DTO2 and the DAC
- t_b; chrominance bandpass and gain control stage delay times
- t_{CGC}; clock generator circuit delay time
- t_{ADC}; analog-to-digital converter delay time
- t_{INP}; input switch delay time.

As delay t_a and t_b are known constants, t_{IDEL} is programmed in the range of −115 to −214/216 LL3 clock cycles, as follows:

- $t_{IDEL} = -115 - 0.5$ $(* - t_{CGC} - t_{ADC} - t_{INP})$.

* Value to be fixed.

HSY

Referring to Fig.10 point (1) and periods a and b:

- HSY start time = $t_{(1)} - a$ (LL3 clock cycles)
- HSY stop time = $t_{(1)} - b$ (LL3 clock cycles)

Programming range of HSY start/stop time: +191 to −64 (LL3 clock cycles).

HC

Referring to Fig.10 point (1) and periods c and d:

- HC start time = $t_{(1)} - c$ (LL3 clock cycles)
- HC stop time = $t_{(1)} - d$ (LL3 clock cycles)

Programming range of HC start/stop time: +127 to −128 (LL3 clock cycles).

HS

The HS reference positions in PAL and NTSC modes are shown in Fig.10 at points (3) and (4) respectively. To move the HS pulse to the centre of blanking pulse $\overline{BL}$ the following equation is used:

- HS (NTSC);

  position of HS relative to the zero point (LL3 clock cycles) 4 LL3 clock cycles
- HS (PAL);

  position of HS relative to the zero point (LL3 clock cycles) 4 LL3 clock cycles

The length of HS is 64 LL3 clock cycles.

Programming of the luminance path of the S-DMSD

The VBS (without chrominance) or CVBS input signal enters the prefilter (a high-pass transfer function with maximum gain of 9.5 dB). The control bit PF switches the filter into the bypass mode. The next stage is the chrominance trap which can be programmed (zero point) to 4.43 MHz (PAL) or 3.58 MHz (NTSC) by the control bit YPN. Bit BY activates the bypass function for the Y/G mode of the S-DMSD. The chrominance trap output signal is then divided into three Channels as described in section 'Luminance path'.

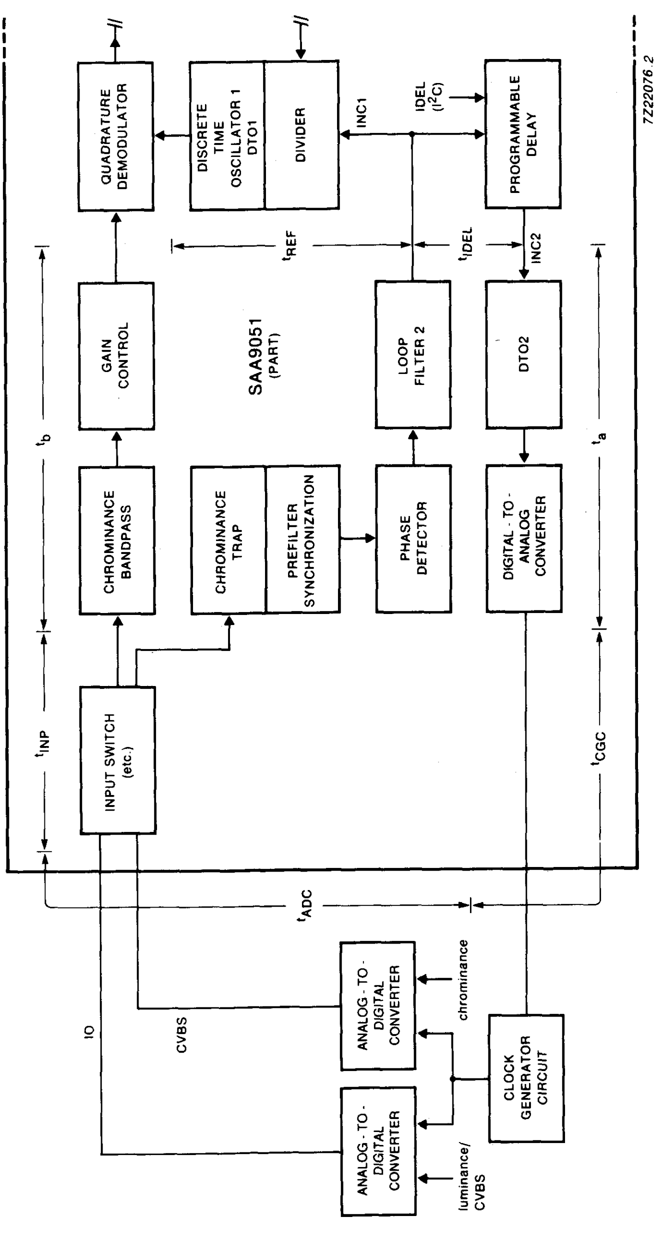
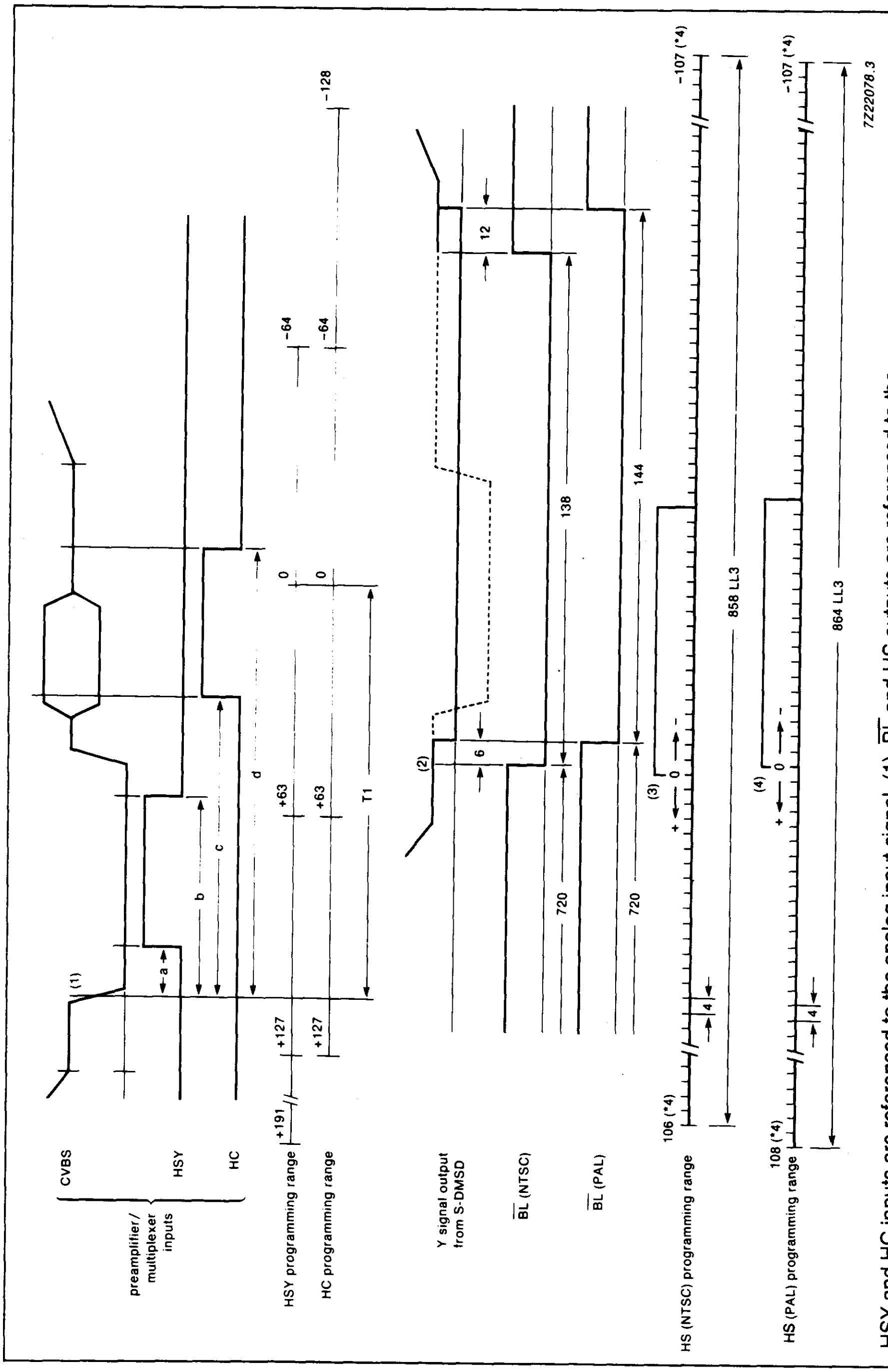


Fig.9 Compensation of delay times by incrementing delay control IDEL.



HSY and HC inputs are referenced to the analog input signal (1). $\overline{BL}$ and HS outputs are referenced to the S-DMSD output (2). Waveform timing is indicated in numbers (n) of LL3 clock cycles (n x $1/f_{LL3}$), where n = 1 for HSY, HC, $\overline{BL}$ and CVBS inputs to the S-DMSD and n = 4 for HS.

Data delay T1 input to output at subaddress SA06 = C0

SA0B = 00 : 63 x $1/f_{LL3}$

SA0B = 3C : 123 x $1/f_{LL3}$

Fig.10 Signal correction.

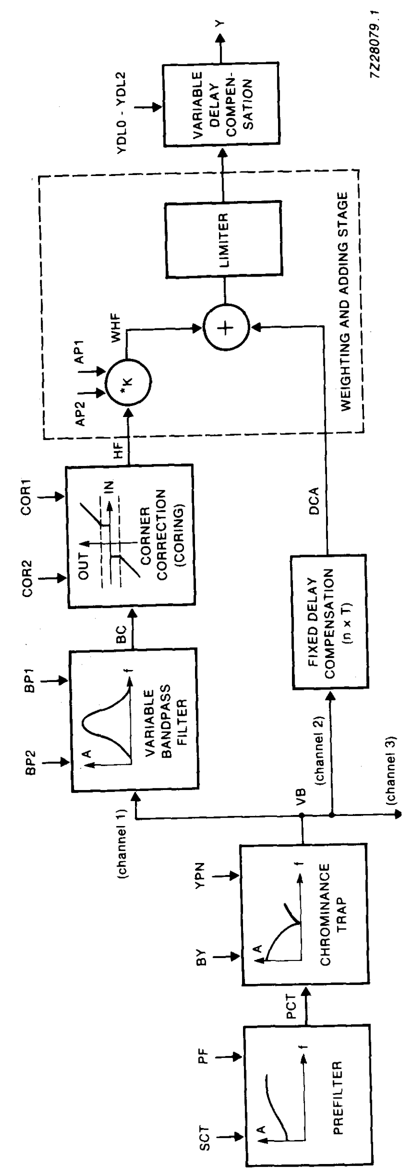


Fig.11 Luminance path of the S-DMSD.

SUBADDRESS 06

Table 13 Chrominance trap select (BY switches the chrominance trap to the bypass mode; YPN selects the notch-frequency)

CHROMINANCE TRAP	CONTROL BITS	
	BY (SA06, D7)	YPN (SA08, D2)
PAL (4.43 MHz)	0	0
NTSC (3.58 MHz)	0	1
bypass	1	X

Table 14 Disconnecting the luminance prefilter (user dependent)

PREFILTER	CONTROL BIT PF (SA06, D6)
ON	0
OFF	1

Table 15 Bandpass control (BP1 and BP2 control the centre frequency of the bandpass filter, see Figs 13 to 16)

BANDPASS TYPE (CENTRE FREQUENCY)	CONTROL BITS	
	BP2 (SA06, D5)	BP1 (SA06, D4)
type 1 (4.1 MHz)	0	0
type 2 (3.8 MHz)	0	1
type 3 (2.6 MHz)	1	0
type 4 (2.9 MHz)	1	1

Table 16 Coring threshold level (COR1 and COR2 control the suppression of low amplitude and high frequency signal components, see Fig.12)

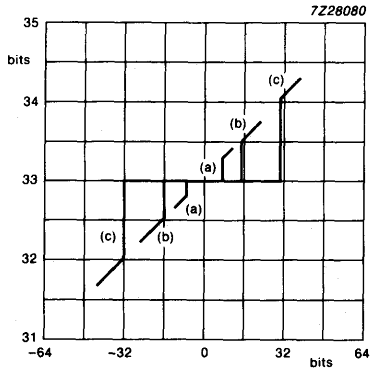
THRESHOLD	Fig.12	CONTROL BITS	
		COR2 (SA06, D3)	COR1 (SA06, D2)
coring off		0	0
coring on (4 bits of 12 bits)	a	0	1
coring on (5 bits of 12 bits)	b	1	0
coring on (6 bits of 12 bits)	c	1	1

Note

The thresholds are related the word width of the bandpass filter (12 bits).

Table 17 Aperture correction factor (AP1 and AP2 select the weighting factor K of the high frequency (HF) luminance components, see Fig.11)

WEIGHTING FACTOR K	CONTROL BITS	
	AP2 (SA06, D1)	AP1 (SA06, D0)
0	0	0
0.25	0	1
0.5	1	0
1	1	1



(a) for COR2 = 0 and COR1 = 1
(b) for COR2 = 1 and COR1 = 0
(c) for COR2 = 1 and COR1 = 1

Fig.12 Coring stage response.

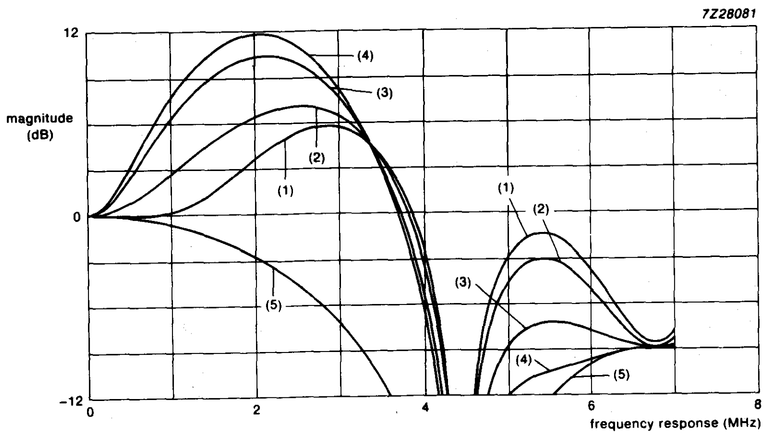


Fig.13 Magnitude of the frequency response of the unlimited summation signal (combining Channel 1 and Channel 2); PAL mode; prefilter OFF; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

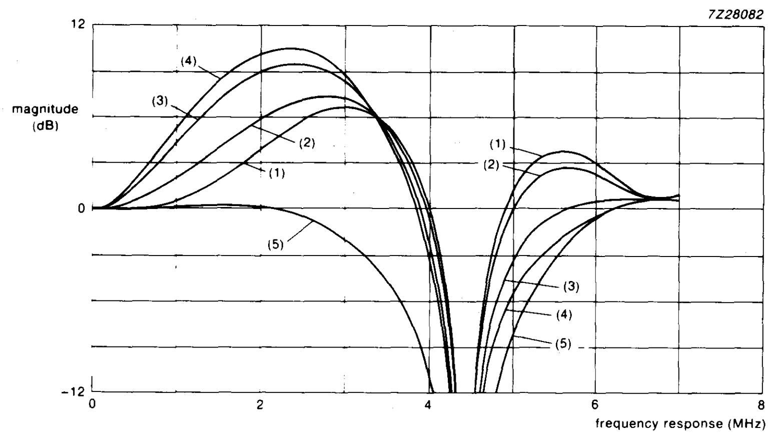


Fig.14 Magnitude of the frequency response of the unlimited summation signal (combining Channel 1 and Channel 2); PAL mode; prefilter ON; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

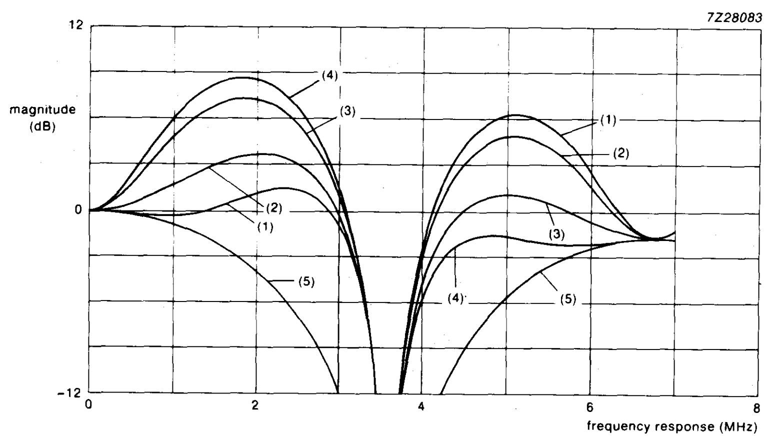


Fig.15 Magnitude of the frequency response of the unlimited summation signal (combining Channel 1 and Channel 2); NTSC mode; prefilter OFF; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

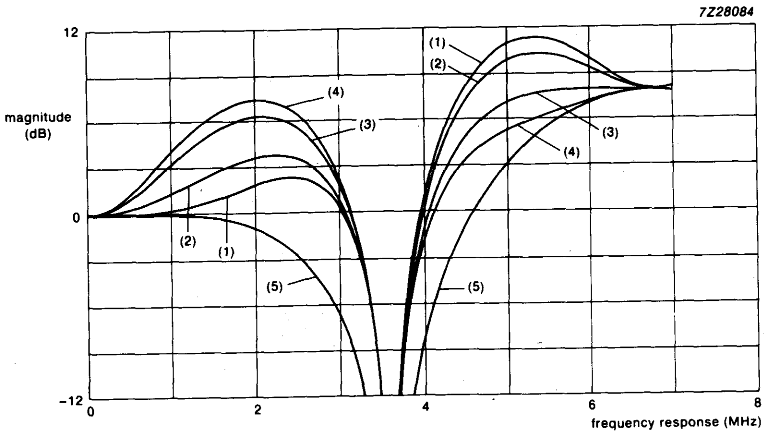


Fig.16 Magnitude of the frequency response of the unlimited summation signal (combining Channel 1 and Channel 2); NTSC mode; prefilter ON; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

SUBADDRESS 07

Table 18 Hue phase (user dependent, see notes 1 to 3)

HUE PHASE (deg)	CONTROL BITS							
	A77	A76	A75	A74	A73	A72	A71	A70
+178.6 to 0	1	1	1	1	1	1	1	1
0	1	0	0	0	0	0	0	0
0 to −180	0	0	0	0	0	0	0	0

Notes to Table 18

1. Step size per least significant bit (A70) = 1.4 degree.
2. Reference point for positive colour difference signals = 0 degree.
3. The hue phase may be shifted ±180 degrees from the reference point using bit A77, the colour difference signals are then switched from normally positive to negative polarity.

SUBADDRESS 08

Table 19 Horizontal clock PLL (application dependent)

FUNCTION	HPLL CONTROL BIT (SA08, D7)
horizontal clock PLL open, horizontal frequency fixed	1
horizontal clock PLL closed	0

Table 20 Field frequency select (system mode dependent)

FUNCTION	CONTROL BIT FS (SA08, D6)
60 Hz; 525-line mode	1
50 Hz; 625-line mode	0

Table 21 VTR/TV mode select (system mode dependent)

FUNCTION	CONTROL BIT VTR (SA08, D5)
VTR mode	1
TV mode	0

Table 22 Colour on control (system mode dependent)

FUNCTION	CONTROL BIT CO (SA08, D4)
colour ON	1
colour OFF (all colour output samples zero)	0

Table 23 Alternate/non–alternate mode (system mode dependent)

FUNCTION	CONTROL BIT ALT (SA08, D3)
alternate mode (PAL)	1
non-alternate mode (NTSC)	0

Table 24 Chrominance trap select and amplitude matching (system mode dependent)

CHROMINANCE TRAP	CONTROL BIT YPN (SA08, D2)
3.58 MHz	1
4.43 MHz	0

Table 25 Colour carrier frequency control (system mode dependent)

COLOUR CARRIER FREQUENCY	CONTROL BITS	
	CCFR1 (SA08, D1)	CCFR0 (SA08, D0)
4 433 618.75 Hz (PAL-B, G, H, 1; NTSC 4.43)	0	0
3 575 611.49 Hz (PAL-M)	0	1
3 582 056.25 Hz (PAL-N)	1	0
3 579 545 Hz (NTSC-M)	1	1

SUBADDRESS 09

Table 26 Vertical noise limiter.

FUNCTION	CONTROL BIT VNL (SA09, D7)
VNL active	1
VNL bypassed	0

Table 27 Y-output enable (system mode dependent)

FUNCTION	CONTROL BIT OEY (SA09, D6)
outputs D1 - D7 and $\overline{BL}$ active	1
outputs D1 - D7 and $\overline{BL}$ HIGH-impedance Z-state	0

Table 28 Chrominance output enable (system mode dependent)

FUNCTION	CONTROL BIT OEC (SA09, D5)
outputs UV0 - UV3 active; if CD = logic 1, chrominance signal output; if CD = logic 0, zero signal	1
outputs UV0 - UV3 HIGH-impedance Z-state	0

Table 29 Internal colour forced ON/OFF (test purposes only)

FUNCTION	CONTROL BIT CI (SA09, D3)
colour forced ON, if CO = logic 1 (CD = X) or colour OFF, if CO = logic 0 (CD = X)	1
colour OFF, if CO = logic 0 (CD = X) or colour controlled by CD, if CO = logic 1	0

Where:

X = don't care.

Table 30 Additional output for circuit control

FUNCTION	CONTROL BIT AFCC
output AFCC = HIGH	1
output AFCC = LOW	0

Table 31 Source-select (system mode dependent)

FUNCTION	CONTROL BIT SS0 - SS3
output SS0 - SS3 = HIGH	1
output SS0 - SS3 = LOW	0

Table 32 Source select (pin and subaddress)

CONTROL BIT	PIN	SUBADDRESS
AFCC	68	09, D2
SS3	25	0A, D4
SS2	24	0A, D3
SS1	66	09, D1
SS0	65	09, D0

SUBADDRESS 0A

Table 33 Disabling of HSY and HC pulses (system mode dependent)

FUNCTION	CONTROL BIT SYC (SA0A, D7)
HSY and HC output pulses disabled	1
HSY and HC output pulses enabled	0

Table 34 Chrominance input/output 3-state control

FUNCTION	CONTROL BIT CT (SA0A, D6)
CVBS output active	1
output HIGH-impedance Z-state	0

Table 35 Chrominance source select

FUNCTION	CONTROL BIT YC (SA0A, D5)
Y/C separate inputs	1
CVBS input	0

Table 36 Variable delay compensation of the luminance path (YDL0 - YDL2 control the luminance delay in order to compensate different chrominance delays throughout the system)

DELAY (N =)	CONTROL BITS (SA0A, D2 .. D0)		
	YDL2	YDL1	YDL0
0	0	0	0
+1	0	0	1
+2	0	1	0
+3	0	1	1
–4	1	0	0
–3	1	0	1
–2	1	1	0
–1	1	1	1

Notes to Table 36

1. The delay is given in terms of clock cycles:
2. 13.5 MHz = N x 74 ns.

SUBADDRESS 0B

Table 37 SECAM chrominance delay compensation (system mode dependent)

PROGRAMMABLE DELAY*	CONTROL BITS						
	SCDC6	SCDC5	SCDC4	SCDC3	SCDC2	SCDC1	SCDC0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.
4	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.
8	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.
16	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.
32	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.
63	0	1	1	1	1	1	1
64	1	1	1	0	0	0	0
65	1	1	1	0	0	0	1
. .	.	.	.	.	.	.	.
79	1	1	1	1	1	1	1
Maximum delay selected by single control bit							
	16	32	16	8	4	2	1

Notes to Table 37

1. * = Delay in number of LL3 clock cycles.
2. SA0B, D7 don't care.

SLAVE TRANSMITTER ORGANIZATION

Slave transmitter format

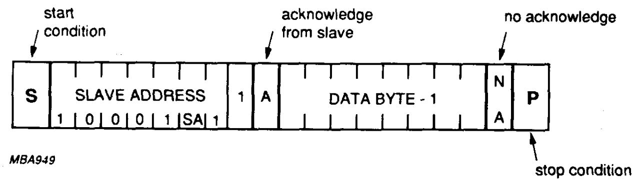


Fig.17 Slave transmitter format (a general call address is not acknowledged).

The format of data byte 1 is:

Table 38

D7	D6	D5	D4	D3	D2	D1	D0
PONRES	HLOCK	1	FD	0	CD	CS	0

Data bits D0, D3 and D5 are fixed in slave transmitter byte.

Table 39 Description of data byte 1

BIT	DESCRIPTION
PONRES	Status bit for power-on-reset ($\overline{RES}$) and after a power failure. logic 1 after the first power-on-reset and after a power failure. Also set to logic 1 after a severe voltage dip that may have disturbed slave receiver data in the PAL/NTSC decoder (SAA9051). PONRES sets all data bits of control registers 1 and 2 to zero. logic 0 after a successful read of the PAL/NTSC decoder status byte
HLOCK	Status bit for horizontal frequency lock (transmitter identification, stop or mute bit): logic 1 if horizontal frequency is not locked (no transmitter available); logic 0 if horizontal frequency is locked (transmitter received)
FD	Detected field frequency status bit: logic 1 when received signal has 60 Hz synchronization pulses; logic 0 when received signal has 50 Hz synchronization pulses
CD	PAL/NTSC colour-detected status bit: logic 1 when PAL/NTSC colour signal is detected; logic 0 when no PAL/NTSC colour signal is detected
CS	SECAM colour-detected status bit: logic 1 when SECAM colour signal is detected; logic 0 when no SECAM colour signal is detected.

Default coefficients set for the S-DMSD and SAA9056

The default coefficients are set for operation with the TDA8703 or TDA8708, these devices are analog-to-digital converters. The 3-state outputs of the chrominance ADC are controlled by the SS3 switch in this example (all numbers are hex values).

The slave addresses are as follows:

- S-DMSD; 8A or 8E
- SAA9056; 8A or 8E

Table 40 Slave address (SAA9051 part)

SUBADDRESS	FUNCTION	SHORT DELAY	LONG DELAY
00	inc. delay	5E	7E
01	HSY start	37	73
02	HSY stop	07	43
03	HC start	F6	32
04	HC stop	C7	03
05	HS start	FF	FF
06	H-peaking	02 (62 NTSC)	02 (62 NTSC)
07	HUE control	00	00
08	control 1	38 (77 NTSC)	38 (77 NTSC)
09	control 2	E3	E3 (D3 SECAM)
0A	control 3	58 (28 Y/C mode)	58 (28 Y/C mode)
0B	SECAM delay	00	3C

Notes to Table 40

1. Subaddress 05; application dependent.
2. Subaddress 08; HPLL is in the VTR mode. Hex value for TV mode is 18 (57 for NTSC).

Table 41 Slave address (SAA9056 part)

SUBADDRESS	FUNCTION	VALUE
10	luminance delay	C0 - FF
11	$\overline{BL}$ delay	00
12	burst gate start	42
13	burst gate stop	56
14	sensitivity	20
15	filter	24
16	control	04 (02 active)

Table 42 Operating modes of the S-DMSD

INPUT	CT	YC	SS3	CE	SCDC	IDEL	YPN	BY	FS	ALT	CCFR1	CCFR0	REMARKS
PAL B, G, H, I													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	1	0	0	
Y/C	0	1	0	0	A	A	0 (1)	1	0	1	0	0	
PAL M													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	1	0	1	1	0	1	
Y/C	0	1	0	0	A	A	1 (0)	1	1	1	0	1	
PAL N													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	1	1	0	
Y/C	0	1	0	0	A	A	0 (1)	1	0	1	1	0	
SECAM													
CVBS	1	0 (1)	1	1	B	B	0	0	0	0 (1)	0 (1)	0 (1)	
Y/C	0	1 (0)	0	1	B	B	0 (1)	1	0	0 (1)	0 (1)	0 (1)	
NTSC 4.43 MHz													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	0	0	0	use FS = 1 for 60 Hz vertical frequency
Y/C	0	1	0	0	A	A	0 (1)	1	1	0	0	0	use FS = 1 for 60 Hz vertical frequency
NTSC M													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	1	0	1	0	1	1	
Y/C	0	1	0	0	A	A	1 (0)	1	1	0	1	1	

Notes to Table 42

1. SS3 is assumed to control the 3-state output of the chrominance ADC (active LOW).
2. To avoid data collision care must be taken with the programming of CT and SS3 (in this equal they are always equal).

Where:

A = short time delay.
B = long time delay.

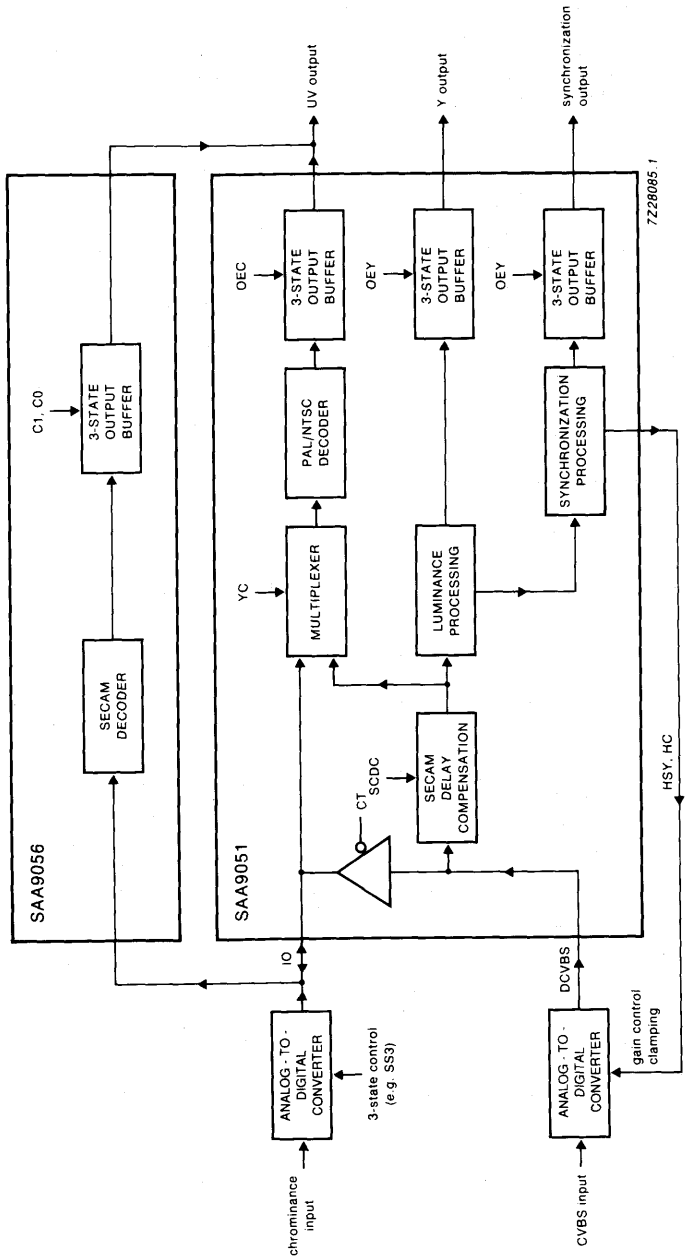


Fig.18 SAA9051 signal flow when used in conjunction with SAA9056.

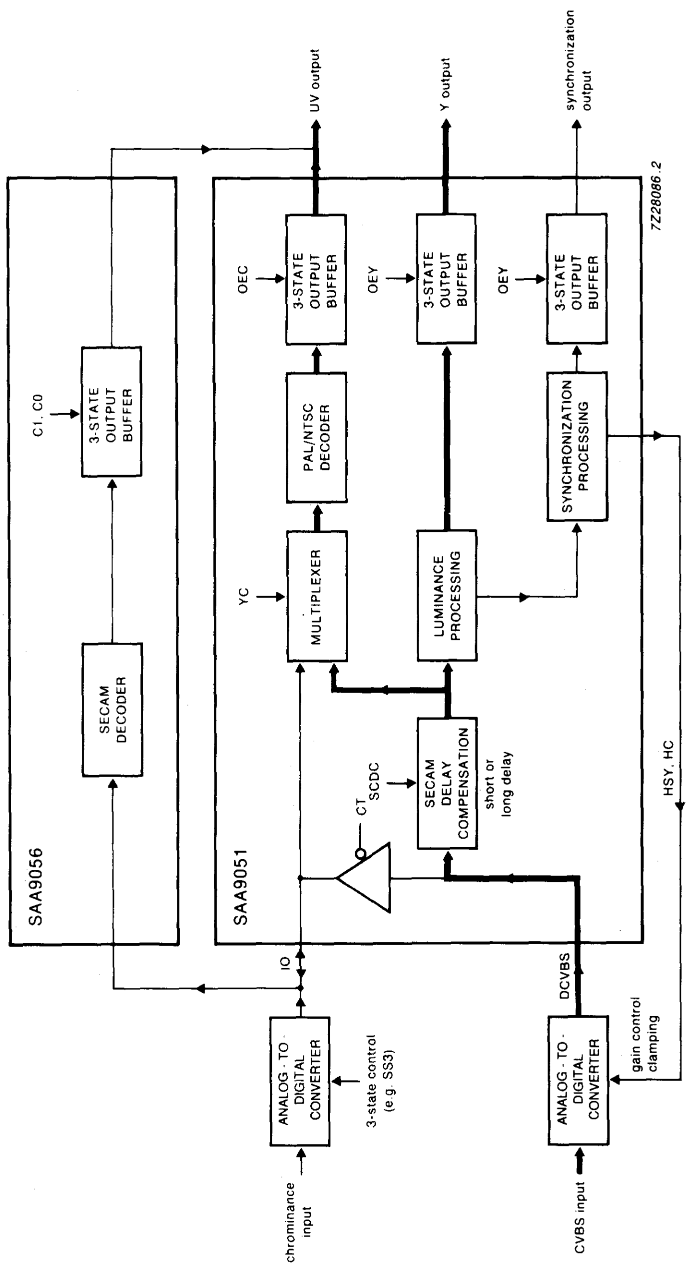


Fig.19 Signal flow - PAL or NTSC with CVBS input signal.

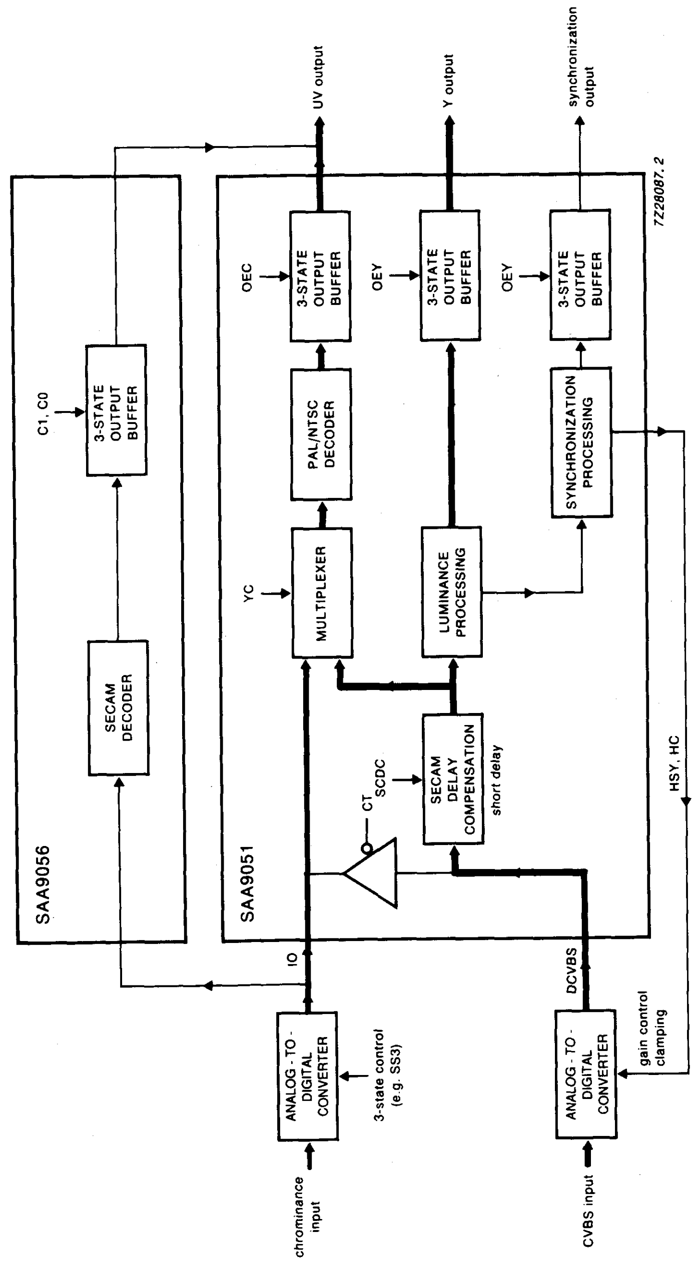


Fig.20 Signal flow - PAL or NTSC with Y/C input signal.

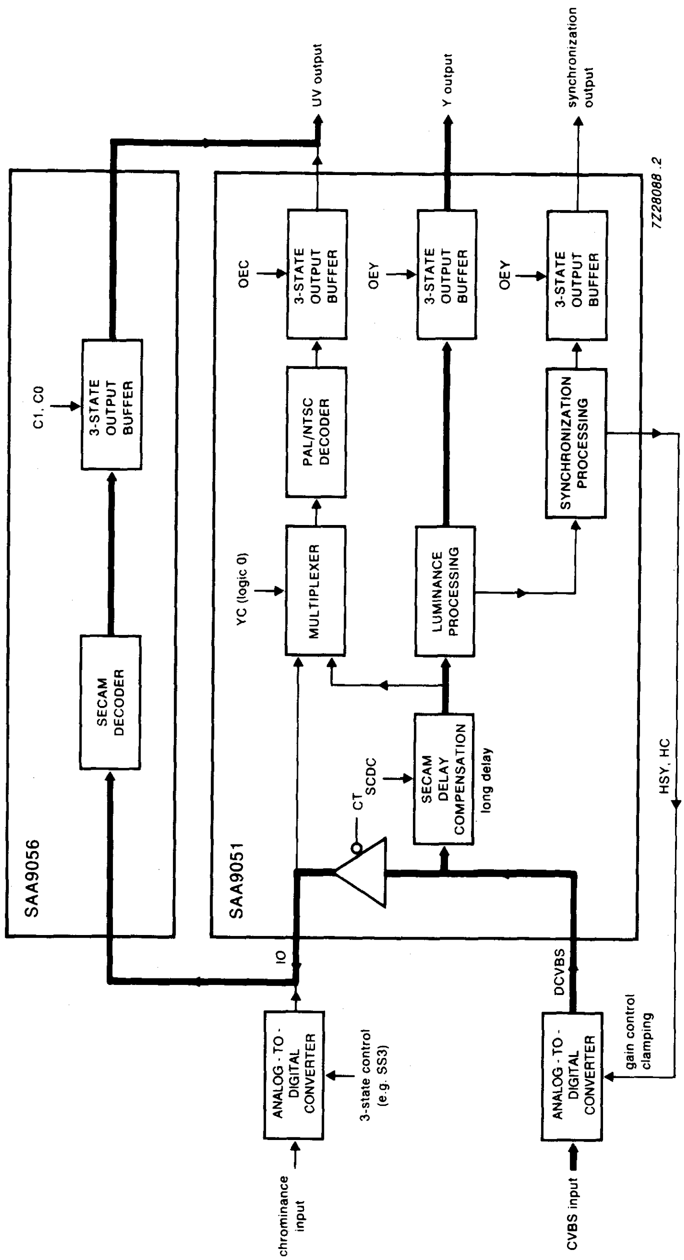


Fig.21 Signal flow - SECAM with CVBS input signal.

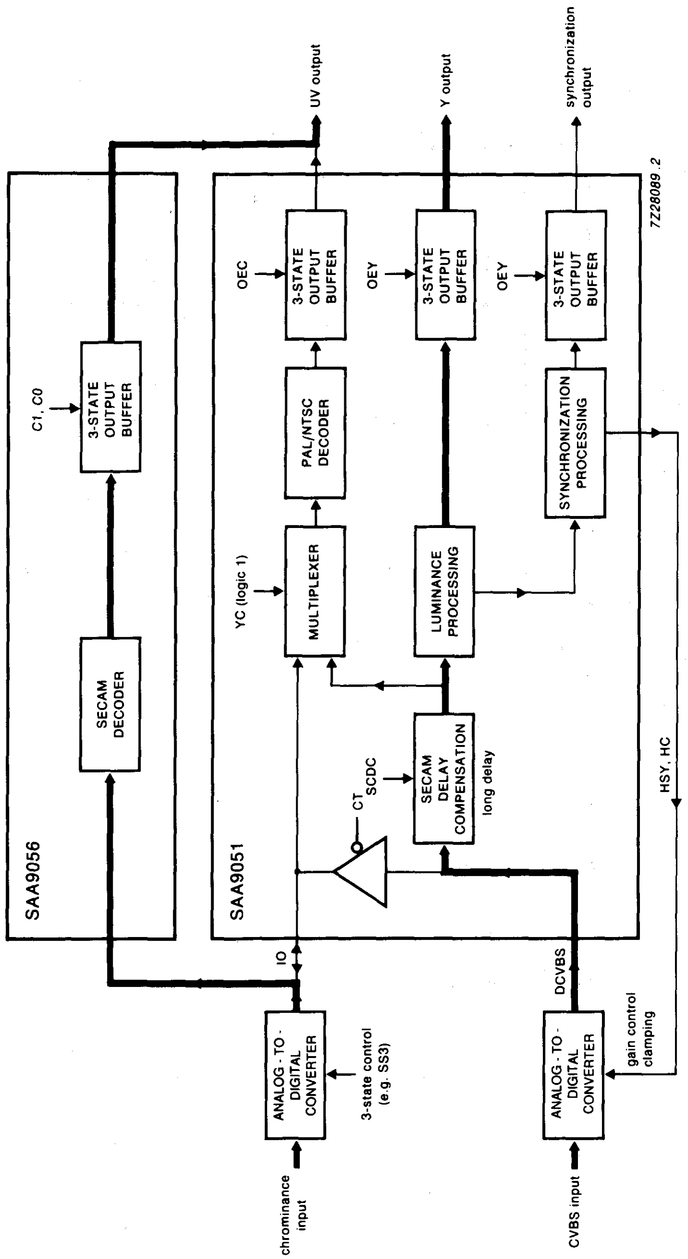


Fig.22 Signal flow - SECAM with Y/C input signal.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		−0.5	+7	V
V_I	input voltage range		−0.5	+7	V
V_O	output voltage range	I_{Omax} = 20 mA	−0.5	+7	V
P_{tot}	maximum power dissipation per package		-	2750	mW
T_{amb}	operating ambient temperature range		0	+70	°C
T_{stg}	storage temperature range		−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 4.5 V to 5.5 V; T_{amb} = 0 to +70 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	5	5.5	V
I_{DD}	supply current	note 1	-	370	500	mA
Inputs						
INPUT VOLTAGE LOW						
V_{IL}	pins 2 - 4, 6 - 17, 20 - 23, 33, 43, 56 and 64		−0.5	-	+0.8	V
V_{IL}	pins 40 and 41		−0.5	-	+1.5	V
INPUT VOLTAGE HIGH						
V_{IH}	pins 2 - 4, 6 - 17, 20 - 23, 43, 56 and 64		2	-	V_{DD}	V
V_{IH}	pins 33, 40 and 41		3	-	V_{DD}	V
INPUT LEAKAGE CURRENT						
I_I	pins 2 - 4, 6 - 17, 20 - 23, 40 - 41, 43 and 64		-	-	10	µA
INPUT CAPACITANCE						
C_I	pin 4		2	-	10	pF
C_I	pins 2 - 3, 14 - 17, 20 - 23, 43 and 64		2	-	7.5	pF
C_I	pins 6 - 13	HIGH-impedance Z-state	2	-	7.5	pF
Outputs						
OUTPUT VOLTAGE LOW						
V_{OL}	pins 6 - 13, 24 - 26, 29 - 32, 42, 45 −50, 53, 55 - 58, 65 - 66 and 68	I_{OL} = 2.0 mA	0	-	0.6	V
V_{OL}	pins 40 and 41	I_{OL} = 5.0 mA	0	-	0.45	V
OUTPUT VOLTAGE HIGH						
V_{OH}	pins 6 - 13, 24 - 26, 29 - 32, 42, 45 - 50, 53, 55 - 58, 65 - 66 and 68	I_{OH} = −0.5 mA	2.2	-	V_{DD}	V
OUTPUT CAPACITANCE						
C_O	pins 45 - 50, 53 and 55 - 58		-	-	7.5	pF
LFCO OUTPUT (NOTE 2)						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	$R_L \geq 10$ kΩ; $C_L < 15$ pF	1.0	-	-	V
$V_{o(p-p)}$	output voltage (peak-to-peak value)	$R_L \geq 1$ kΩ; $C_L < 15$ pF	0.5	-	-	V
Timing (see Fig.23)						
t_{C3}	LL3 cycle time		69	-	80	ns
t_{C3H}/t_{C3}	LL3 duty factor		43	-	57	%
t_r, t_f	LL3 rise and fall times	note 3	-	-	6	ns
$t_{SU;\,DAT}$	input data set-up time		12	-	-	ns

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Timing (see Fig.23)						
$t_{HD;DAT}$	input data hold time		5	-	-	ns
t_{HD}	output data hold time		5	-	-	ns
t_D	output data delay time	except HSY and HC; C_L = 25 pF; I_{OL} = 2.0 mA; V_{OH} = 2.2 V	-	-	50	ns
t_D	HSY and HC output delay time	C_L = 25 pF; I_{OL} = 2.0 mA; V_{OH} = 2.6 V	-	-	80	ns
C_L	output data load capacitance		7.5	-	25	pF
Crystal oscillator (see Fig.20)						
f_n	nominal frequency	third harmonic	-	24.576	-	MHz
$\Delta f/f_n$	permissible deviation of f_n		-	$\pm 50 \times 10^{-6}$	-	
$\Delta T/f_n$	temperature deviation from f_n		-	$\pm 20 \times 10^{-6}$	-	
T_{XTAL}	temperature range		0	-	+70	°C
C_{LXTAL}	load capacitance		8	-	-	pF
R_r	maximum resonance resistance		-	40	80	Ω
C_1	motional capacitance		-	1.5 ±20%	-	fF
C_0	parallel capacitance		-	3.5 ±20%	-	pF

Notes to the characteristics

1. Inputs LOW and outputs not connected, V_{DD} = 5 V.
2. 4-bit triangular waveform clocked at 24.576 MHz, AC coupled at pin 36.
3. Rising and falling edges of the clock signal are assumed to be smooth e.g. due to roll-off low-pass filtering.

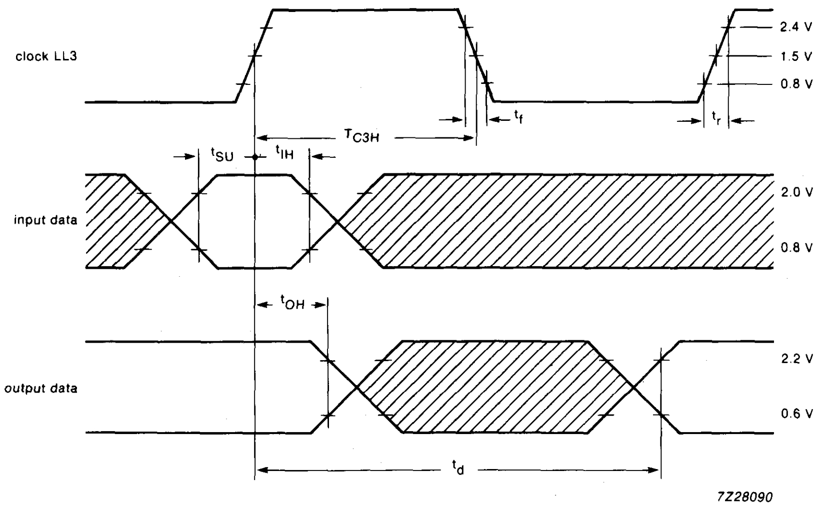


Fig.23 Timing diagram.

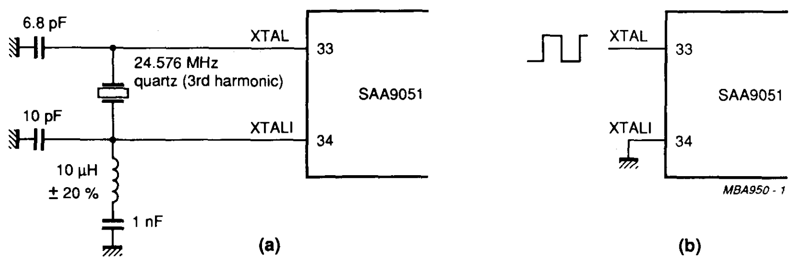


Fig.24 Oscillator circuit requirements; (a) with quartz crystal; (b) with external clock.

Clock signal generator circuit for digital TV systems (CGC)

SAA9057B

FEATURES

- Clock generation suitable for digital TV systems (line-locked)
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LL1.5, LL3 and LL3T (4th and 2nd multiples of input frequency)
- Reset control and power fail detection

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	3	-	9	mA
I_{DDD}	digital supply current	10	-	40	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_i	input frequency range	6.25	-	7.25	MHz
V_I	input voltage LOW input voltage HIGH	0 2.4	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA9057B generates all clock signals required for a digital TV system suitable for the SAA90xx family. Optional extras (feature box etc.) can be driven via external buffers, adventageous for a digital TV system based on display standard conversion concepts.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9057B	20	DIL	plastic	SOT146
SAA9057BT	20	mini-pack (SO20)	plastic	SOT163A

Clock signal generator circuit for digital TV systems (CGC)

SAA9057B

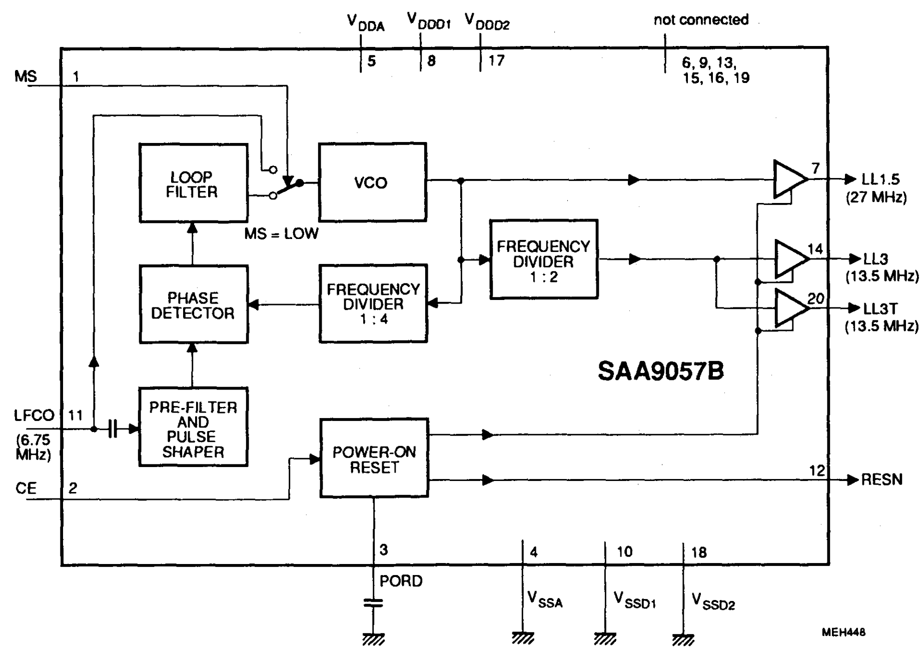


Fig.1 Block diagram.

FUNCTION DESCRIPTION

The SAA9057B generates all clock signals required for a digital TV system suitable for the SAA90xx family. Optional extras (feature box etc.) can be driven via external buffers, advantageous for a digital TV system based on display standard conversion concepts.
The 6.75 MHz input signal LFCO, coming from SAA 9051, is multiplied to 27 MHz by the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LL1.5 (pin7). 13.5 MHz frequency is also generated by 1:2 divider and output on LL3 and LL3T (pins 14 and 20).
The rectangular output signals have 50 % duty factor.

Mode select MS

The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit operates as an oscillator and frequency divider. MS function is not tested.

Chip enable CE

The buffer outputs are enabled and power-on reset is set to HIGH by CE = HIGH (Fig.4).
CE = LOW sets the clock outputs HIGH and RESN output LOW.

Power-on reset

Power-on reset is activated at power-on, when the supply voltage decreases below 3.5 V (Fig.4) or when chip enable is done. The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuit of this digital TV system.
The LFCO input signal has to be applied before RESN becomes HIGH.

PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode)
CE	2	chip enable /reset (HIGH = outputs enabled)
PORD	3	power-on reset delay dependent on external capacitor
V_{SSA}	4	analog ground (0 V)
V_{DDA}	5	analog supply voltage (+5 V)
n.c.	6	not connected
LL1.5	7	line-locked clock output signal (4 times f_{LFCO})
V_{DDD1}	8	digital supply voltage 1 (+5 V)
n.c.	9	not connected
V_{SSD1}	10	digital ground 1 (0 V)
LFCO	11	line-locked input frequency
RESN	12	reset output (active-LOW)
n.c.	13	not connected
LL3	14	line-locked clock output signal (2 times f_{LFCO})
n.c.	15	not connected
n.c.	16	not connected
V_{DDD2}	17	digital supply voltage 2 (+5 V)
V_{SSD2}	18	digital ground 2 (0 V)
n.c.	19	not connected
LL3T	20	line-locked clock output signal (2 times f_{LFCO})

PIN CONFIGURATION

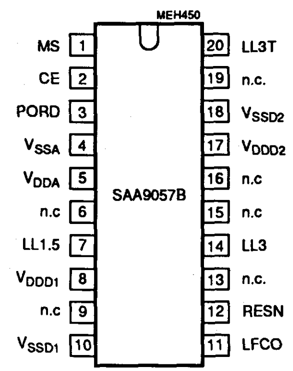


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	−0.5	7.0	V
V_{DDD}	digital supply voltage (pins 8 and 17)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{DDA} - V_{DDD}$	-	±100	mV
V_O	output voltage (I_{OM} = 20 mA)	−0.5	V_{DDD}	V
P_{tot}	total power dissipation	0	1.1	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	tbf	V

* Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices ".

CHARACTERISTICS

V_{DDA} = V_{DDD} = 4.5 to 5.5 V; f_{LFCO} = 6.25 to 7.25 MHz and T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
I_{DDA}	analog supply current (pin 5)		3	-	9	mA
I_{DDD}	digital supply current (I_8 + I_{17})	note 1	10	-	40	mA
V_{reset}	power-on reset threshold voltage	Fig.4	-	3.5	-	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	-	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	-	V_{DDA}	V
f_{LFCO}	input frequency range		6.25	-	7.25	MHz
C_{11}	input capacitance		-	-	10	pF
Inputs MS and CE (pins 1 and 2)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}	V
I_{LI}	input leakage current		-	-	10	µA
C_I	input capacitance		-	-	5	pF
Output RESN (pin 12)						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.4	-	V_{DDD}	V
I_{LI}	output leakage current		-	-	±10	µA
t_d	RESN delay time	C_3 = 0.1µF; Fig.4	20	-	200	ms
Output signals LL1.5, LL3 and LL3T (pins 7, 14 and 20)						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.6	-	V_{DDD}	V
I_{LI}	output leakage current	high-impedance	-	-	±10	µA
t_{comp}	composite rise time	note 1; note 2	-	-	9	ns
f_{LL}	output frequency LL1.5	Figures 3 and 6	-	4 f_{LFCO}	-	MHz
	output frequency LL3		-	2 f_{LFCO}	-	MHz
	output frequency LL3T		-	2 f_{LFCO}	-	MHz
t_{LL}	duty factor LL1.5	note 1; Fig.3	40	50	60	%
	duty factor LL3 and LL3T	note 1; Fig.3	43	50	57	%
t_r, t_f	rise and fall times	note 1; Fig.3	-	-	6	ns

Notes to the characteristics

1. f_{LFCO} = 7.0 MHz and output load 40 pF. VSSA and VSSD short connected together.
2. t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Fig.3) including rise time, skew and jitter components. Measurements taken between 0.6 V and 2.6 V.
3. MS function is not tested.

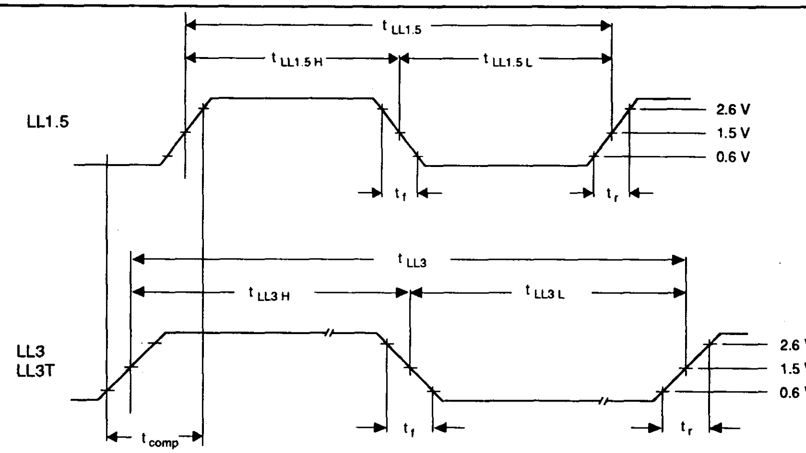


Fig.3 Output timing.

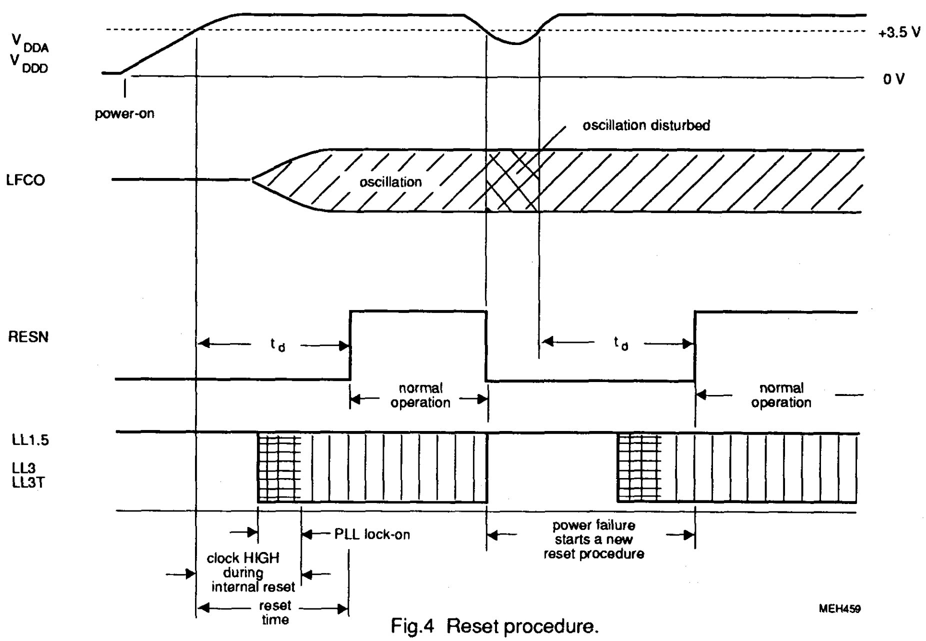
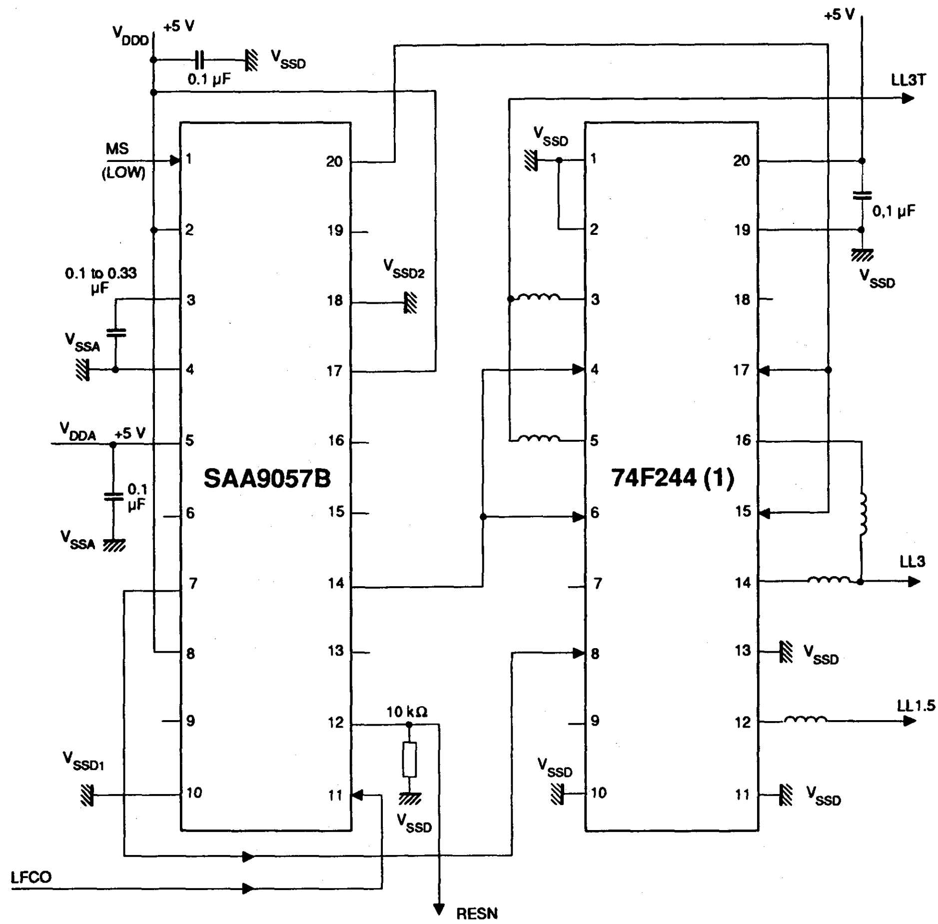


Fig.4 Reset procedure.



(1) buffer circuit optionally

MEH449

Fig.5 Application circuit.

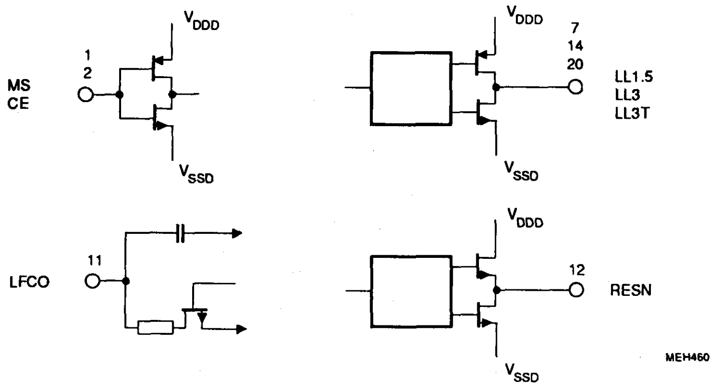


Fig.6 Internal circuit.

Video enhancement and D/A processor (VEDA)

SAA9065

1. FEATURES

- CMOS circuit to enhance video data and to convert luminance and colour-difference signals from digital-to-analog
- 16-bit parallel input for 4:1:1 and 4:2:2 YUV data
- Data clock input LLC (line-locked clock) for a data rate up to 30 MHz
- 8-bit luminance and 8-bit multiplexed colour-difference formats (optional 7-bit formats)
- MC input to support various clock and pixel rates
- Formatter for YUV input data; 4:2:2 format, 4:1:1 format and filter characteristics selectable
- HREF input to determine the active line (number of pixels)
- Controllable peaking of luminance signal
- Coring stage with controllable threshold to eliminate noise in luminance signal
- Interpolation filter suitable for both formats to increase the data rate in chrominance path
- Polarity of colour-difference signals selectable
- Separate digital-to-analog converters (9-bit resolution for Y; 8-bit for colour-difference signals)
- 1 V (p-p)/ 75 Ω outputs realized by two resistors
- No external adjustments
- All functions controlled via I^2C-bus

2. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage digital part	4.5	5	5.5	V
V_{DDA}	supply voltage analog part	4.75	5	5.25	V
I_{DD}	total supply current	-	tbf	-	mA
V_{IL}	input voltage LOW on YUV-bus	−0.5	-	0.8	V
V_{IH}	input voltage HIGH on YUV-bus	2	-	V_{DDD}+0.5	V
f_{LLC}	input data rate	-	-	30	MHz
$V_{o\,Y,CD}$	output signal Y, ±(R−Y) and ±(B−Y) (peak-to-peak value)	-	2	-	V
$R_{L\,Y,CD}$	output load resistance	125	-	-	Ω
ILE	DC integral linearity error in output signal (8-bit data)	-	-	1	LSB
DLE	DC differential error in output signal (8-bit data)	-	-	0.5	LSB
T_{amb}	operating ambient temperature range	0	-	70	°C

3. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9065	44	PLCC	plastic	SOT187

4. BLOCK DIAGRAM

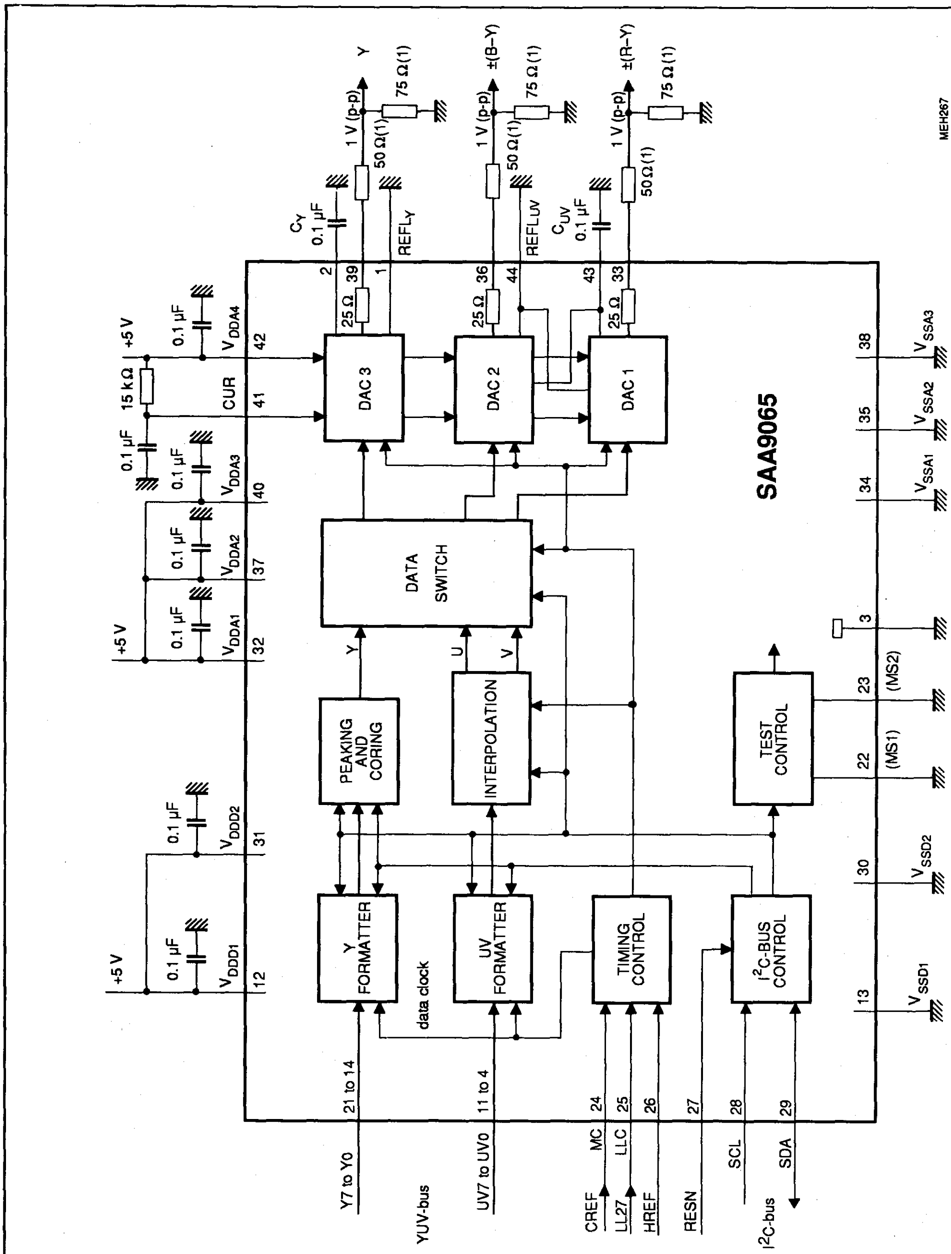


Fig.1 Block diagram and application circuit.

(1) output amplitude determined by resistors ($R_L > 125 \Omega$)

5. PINNING

SYMBOL	PIN	DESCRIPTION
$REFL_Y$	1	low reference of luminance DAC (connected to V_{SSA1})
C_Y	2	capacitor for luminance DAC (high reference)
SUB	3	substrate (connected to V_{SSA1})
UVO	4	UV signal input bits UV7 to UV0 (digital colour-difference signal)
UV1	5	
UV2	6	
UV3	7	
UV4	8	
UV5	9	
UV6	10	
UV7	11	
V_{DDD1}	12	+5 V digital supply voltage 1
V_{SSD1}	13	digital ground 1 (0 V)
Y0	14	Y signal input bits Y7 to Y0 (digital luminance signal)
Y1	15	
Y2	16	
Y3	17	
Y4	18	
Y5	19	
Y6	20	
Y7	21	
MS2	22	mode select 2 input for testing chip
MS1	23	mode select 1 input for testing chip
MC	24	data clock CREF (13.5 MHz e. g.); at MC = HIGH the LLC divider-by-two is inactive
LLC	25	line-locked clock signal (LL27 = 27 MHz)
HREF	26	data clock for YUV data inputs (for active line 768Y or 640Y long)
RESN	27	reset input (active LOW)
SCL	28	I^2C-bus clock line
SDA	29	I^2C-bus data line
V_{SSD2}	30	digital ground 2 (0 V)
V_{DDD2}	31	+5 V digital supply voltage 2
V_{DDA1}	32	+5 V analog supply voltage for buffer of DAC 1
(R–Y)	33	±(R–Y) output signal (analog signal)
V_{SSA1}	34	analog ground 1 (0 V)

SYMBOL	PIN	DESCRIPTION
V_{SSA2}	35	analog ground 2 (0 V)
(B–Y)	36	±(B–Y) output signal (analog colour-difference signal)
V_{DDA2}	37	+5 V analog supply voltage for buffer of DAC 2
V_{SSA3}	38	analog ground 3 (0 V)
Y	39	Y output signal (analog luminance signal)
V_{DDA3}	40	+5 V analog supply voltage for buffer of DAC 3
CUR	41	current input for analog output buffers
V_{DDA4}	42	supply and reference voltage for the three DACs
C_{UV}	43	capacitor for chrominance DACs (high reference)
$REFL_{UV}$	44	low reference of chrominance DACs (connected to V_{SSA1})

PIN CONFIGURATION

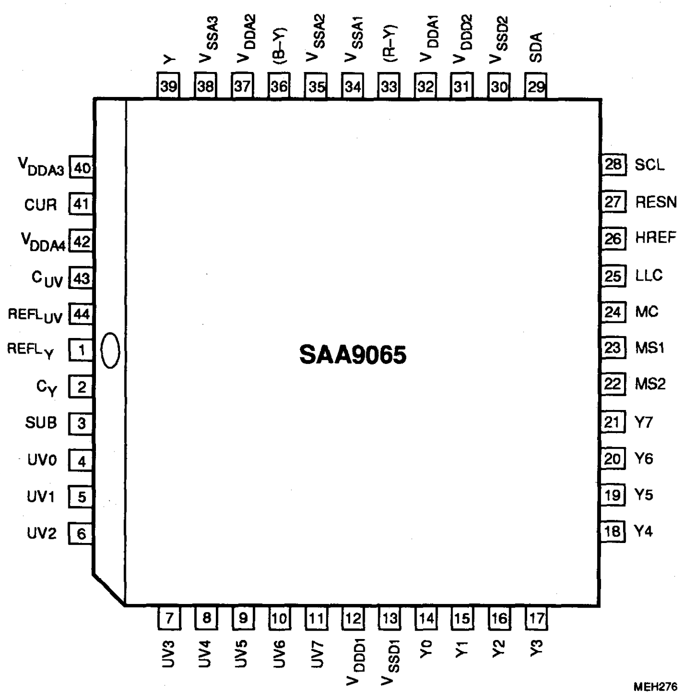


Fig.2 Pin configuration.

6. FUNCTIONAL DESCRIPTION

The CMOS circuit SAA9065 processes digital YUV-bus data up to a data rate of 30 MHz. The data inputs Y7 to Y0 and UV7 to UV0 (Fig.1) are provided with 8-bit data. The data of digital colour-difference signals U and V are in a multiplexed state (serial in 4:2:2 or 4:1:1 format; Tables 2 and 3).

Data is read with the rising edge of LLC (line-locked clock) to achieve a data rate of LLC at MC = HIGH only. If MC is supplied with the frequency CREF (LLC/2 for example), data is read only at every second rising edge (Fig.3).The 7-bit YUV input data are also supported by means of the R78-bit (R78 = 0). Additionally, the luminance data format is converted for internal use into a two´s complement format by inverting MSB. The Y input byte (bits Y7 to Y0) represent luminance information; the UV input byte (bits UV7 to UV0) one of the two digital colour-difference signals in 4:2:2 format (Table 2).

The HREF input signal (HREF = HIGH) determines the start and the end of an active line (Fig.3) the number of pixels respectively . The analog output Y is blanked at HREF = LOW, the (B–Y) and (R–Y) outputs are in a colourless state. The blanking level can be set by the BLV-bit.
The SAA9065 is controllable via the I²C-bus.

Y and UV formatters

The input data formats are formatted into the internally used processing formats (separate for 4:2:2 and 4:1:1 formats). The IFF, IFC and IFL bits control the input data format and determine the right interpolation filter (Figures 10 to 13).

Peaking and coring

Peaking is applied to the Y signal to compensate several bandwidth reductions of the external pre-processing. Y signals can be improved to obtain a better sharpness.
There are the two switchable bandpass filters BF1 and BF 2 controlled via the I²C-bus by the bits BP1, BP0 and BFB. Thus, a frequency response is achieved in combination with the peaking factor K (Figures 5 to 9; K is determined by the bits BFB, WG1 and WG0).

The coring stage with controllable threshold (4 states controlled by CO1 and CO0 bits) reduces noise disturbances (generated by the bandpass gain) by suppressing the amplitude of small high-frequent signal components. The remaining high-frequent peaking component is available for a weighted addition after coring.

Table 1 LLC and MC configuration modes in DMSD applications

PIN	INPUT SIGNAL	COMMENT
LLC MC	LLC (LL27) CREF	The data rate on YUV-bus is half the clock rate on pin LLC, e. g. in SAA7151B, SAA7191 and SAA7191B single scan operation.
LLC MC	LLC (LL27) MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. in double scan applications.
LLC MC	LLC2/LL3 MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. SAA9051 single scan operation.
Note: YUV data are only latched with the rising edge of LLC at MC = HIGH.		

Table 2 Data format 4 : 2 : 2. (Fig.3)

INPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Interpolation

The chrominance interpolation filter consists of various filter stages, multiplexers and de-multiplexers to increase the data rate of the colour-difference signals by a factor of 2 or 4. The switching of the filters by the bits IFF, IFC and IFL is described previously. Additional signal samples with significant amplitudes between two consecutive signal samples of the low data rate are generated. The time-multiplexed U and V samples are stored in parallel for converting.

Data switch

The digital signals are adapted to the conversation range. U and V data have 8-bit formats again; Y can have 9 bits dependent on peaking. Blanking and switching to colourless level is applied here. Bits can be inverted by INV-bit to change the polarity of colour-difference output signals.

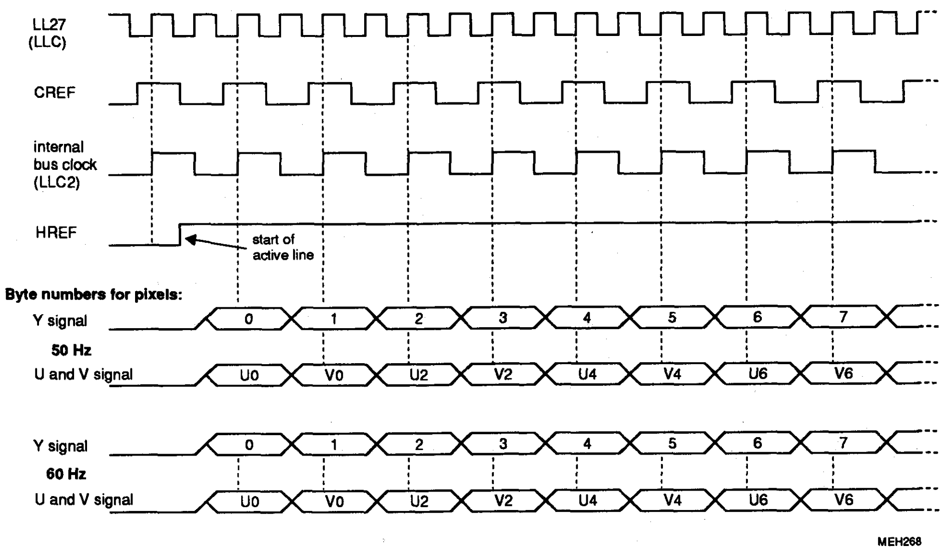
Digital-to-analog converters

Conversion is separate for Y, U and V. The converters use resistor chains with low-impedance output buffers. The minimum output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V floating. An application for 1 V/ 75 Ω on outputs is shown in Fig.1.

Each digital-to-analog converter has its own supply and ground pins suitable for decoupling. The reference voltage, supplying the resistor chain of all three DACs, is the supply voltage V_{DDA4}. The current into pin 41 is 0.3 mA ; a larger current improves the bandwidth but increases the integral non-linearity.

Table 3 Data format 4 : 1 : 1

INPUT	PIXEL BYTE SEQUENCE							
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			



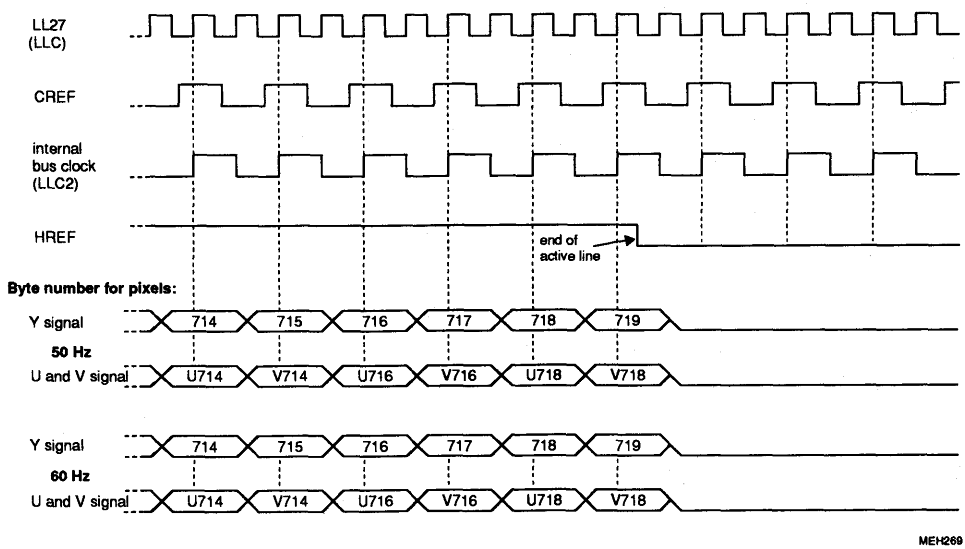


Fig.3 Line control by HREF for 4 : 2 : 2 format, CREF = 13.5 MHz; HREF = 720 pixel; 50 Hz and 60 Hz field.

7. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	−0.3	7	V
V_{DDD2}	supply voltage range (pin 31)	−0.3	7	V
V_{DDA1}	supply voltage range (pin 32)	−0.3	7	V
V_{DDA2}	supply voltage range (pin 37)	−0.3	7	V
V_{DDA3}	supply voltage range (pin 40)	−0.3	7	V
V_{DDA4}	supply voltage range (pin 42)	−0.3	7	V
$V_{diff\ GND}$	difference voltage $V_{SSD} - V_{SSA}$	-	±100	mV
V_n	voltage on all input pins 4 to 11, 14 to 27 and 41	−0.3	V_{DDD}	V
V_n	voltage on analog output pins 33, 36 and 39	−0.3	V_{DDD}	V
P_{tot}	total power dissipation	0	tbf	mW
T_{stg}	storage temperature range	−55	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

8. THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction-to-ambient in free air	46 K/W

9. CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; LLC = LL27; MC = CREF = 13.5 MHz; T_{amb} = 0 to 70 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	for digital part	4.5	5	5.5	V
V_{DDD2}	supply voltage range (pin 31)	for digital part	4.5	5	5.5	V
V_{DDA1}	supply voltage range (pin 32)	for buffer of DAC 1	4.75	5	5.25	V
V_{DDA2}	supply voltage range (pin 37)	for buffer of DAC 2	4.75	5	5.25	V
V_{DDA3}	supply voltage range (pin 40)	for buffer of DAC 3	4.75	5	5.25	V
V_{DDA4}	supply voltage range (pin 42)	DAC reference voltage	4.75	5	5.25	V
I_{DDD}	supply current (I_{DDD1} + I_{DDD2})	for digital part	-	tbf	tbf	mA
I_{DDA}	supply current (I_{DDA1} to I_{DDA4})	for DACs and buffers	-	tbf	tbf	mA
YUV-bus inputs (pins 4 to 11 and 14 to 21)		Figures 3 and 4				
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	µA
Inputs MS1, MS2, MC, LLC, HREF and RESN (pins 22 to 27)						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	µA
V_{24}	MC input voltage for LL27	27 MHz data rate	2.0	-	V_{DDD}+0.5	V
	CREF signal on MC input	CREF data rate; note 1	-	-	-	V
I²C-bus SCL and SDA (pins 28 and 29)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3.0	-	V_{DDD}+0.5	V
I_I	input current	V_I = LOW or HIGH	-	-	±10	µA
V_{OL}	SDA output voltage LOW (pin 29)	I_{29} = 3 mA	-	-	0.4	V
I_{29}	output current	during acknowledge	3	-	-	mA
Digital-to-analog converters (pins 1, 2, 41, 42, 43 and 44)						
V_{DAC}	input reference voltage for internal resistor chains (pin 42)		4.75	5	5.25	V
I_{CUR}	input current (pin 41)	R_{41-42} = 15 kΩ	-	300	-	µA
$V_{1,44}$	reference voltage LOW	pin connected to V_{SSA1}	-	0	-	V
C_L	external blocking capacitor to V_{SSA1} for reference voltage HIGH (pins 2 and 43)		-	0.1	-	µF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LLC}	data conversation rate (clock)	Fig.3	-	-	30	MHz
Res	resolution	luminance DAC	-	9	-	bit
		chrominance DACs	-	8	-	bit
ILE	DC integral linearity error	8-bit data	-	-	1.0	LSB
DLE	DC differential error	8-bit data	-	-	0.5	LSB
Y, ±(R–Y) and ±(B–Y) analog outputs (pins 39, 33 and 36)						
V_o	output signal voltage (peak-to-peak value)	without load	-	2	-	V
$V_{33,36,39}$	output voltage range	without load; note 2	0.2	-	2.2	V
V_{39}	output blanking level	Y output; note 3	-	16	-	LSB
$V_{33,36}$	output no-colour level	±(R–Y), ±(B–Y); note 4	-	128	-	LSB
$R_{33,36,39}$	internal serial output resistance		-	25	-	Ω
$R_{L\ 33,36,39}$	output load resistance	external load	125	-	-	Ω
B	output signal bandwidth	-3 dB	20	-	-	MHz
t_d	signal delay from input to Y output		-	tbf	-	ns
LLC timing (pins 25)		LLC; Fig.3				
t_{LLC}	cycle time		33	37	41	ns
$t_{p\ H}$	pulse width		40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
YUV-bus timing (pins 4 to 11 and 14 to 21)		Fig.5				
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
MC timing (pin24)		Fig.5				
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
RESN timing (pin 27)						
t_{SU}	set-up time after power-on or failure	active LOW; note 5	4 x t_{LLC}	-	-	ns

Notes to the characteristics

1. YUV-bus data is read at MC = HIGH (pin 24) clocked with LLC (Fig.5) . Data is read only with every second rising edge of LLC when CREF = LLC/2 on MC-pin 24.
2. 0.2 to 2.2 V ouput voltage range at 8-bit DAC input data. The data word can increase to 9-bit dependent on peaking factor.
3. The luminance signal is set to the digital black level: 16 LSB for BLV-bit = 0; 0 LSB for BLV-bit = 1.
4. The chrominance amplitudes are set to the digital colourless level of 128 LSB.
5. The circuit is prepared for a new data initialization.

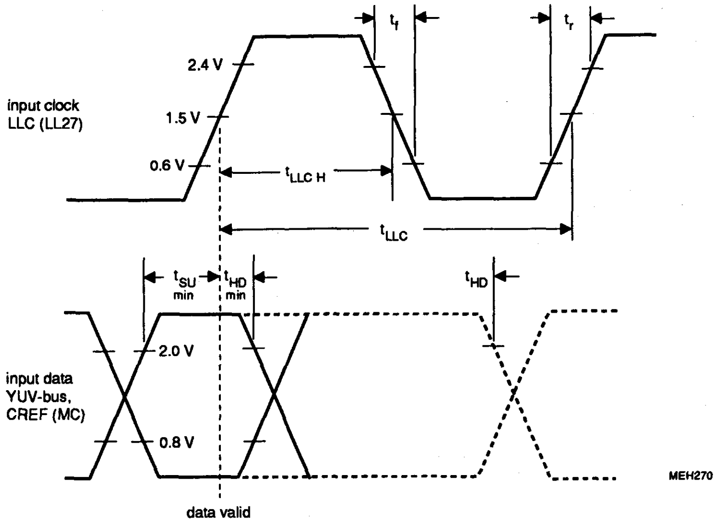


Fig.4 YUV-bus data and CREF timing.

PROCESSING DELAY	LLC CYCLES	REMARKS
YUV digital input to YUV analog output	44	at MC = "1"
	88	at MC = LLC/2

10. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A	------	DATAn	A	P

S = start condition
SLAVE ADDRESS = **1011 111X**
A = acknowledge, generated by the slave
SUBADDRESS* = subadress byte (Table 4)
DATA = data byte (Table 4)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I²C-bus transmission

FUNCTION	SUBADDRESS	DATA D7	D6	D5	D4	D3	D2	D1	D0
Peaking and coring	01	0	CO1	CO0	BP1	BP0	BFB	WG1	WG0
Input formats; interpolation	02	IFF	IFC	IFL	0	0	0	0	0
Input/output setting	03	0	0	0	0	DRP	BLV	R78	INV

Bit functions in data bytes:

CO1 to CO0	Control of coring threshold:	CO1	CO0		
		0	0		coring off
		0	1		small noise reduction
		1	0		medium noise reduction
		1	1		high noise reduction
BP1, BP0 and BFB	Bandpass filter selection:	BP1	BP0	BFB	
		0	0	0	characteristic Fig.5
		0	1	0	characteristic Fig.6
		1	0	0	characteristic Fig.7
		1	1	0	characteristic Fig.8
		0	0	1	BF1 filter bypassed Fig.9
		X	X	1	not recommended

BFB, WG1 and WG0	Peaking factor K:	BFB	WG1	WG0	
		0	0	0	K = 1/8; minimum peaking
		0	0	1	K = 1/4
		0	1	0	K = 1/2
		0	1	1	K = 1; maximum peaking
		1	0	0	K = 0; peaking off
		1	0	1	K = 1/4; minimum peaking
		1	1	0	K = 1/2
		1	1	1	K = 1; maximum peaking
IFF, IFC, IFL	Input format and filter control at 13.5 MHz data rate:	IFF	IFC	IFL	
		0	0	0	4 : 1 : 1 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
		0	0	1	4 : 1 : 1 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
		0	1	0	4 : 1 : 1 format; –3 dB attenuation at 1.2 MHz video frequency; Fig.12
		1	0	0	4 : 2 : 2 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
		1	0	1	4 : 2 : 2 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
		1	1	X	4 : 2 : 2 format; –3 dB attenuation at 2.5 MHz video frequency; Fig.13
DRP	UV input data code:	0 = two's complement; 1 = offset binary			
BLV	Blanking level on Y output:	0 = 16 LSB; 1 = 0 LSB			
R78	YUV input data solution:	0 = 7-bit data; 1 = 8-bit data			
INV	Polarity of colour-difference output signals:	0 = normal polarity equal to input signal 1 = inverted polarity			

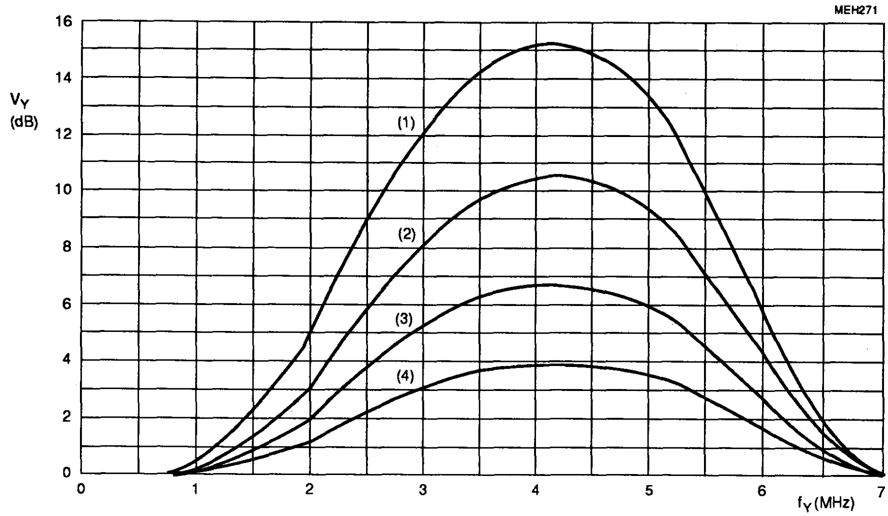


Fig.5 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 0:
(1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

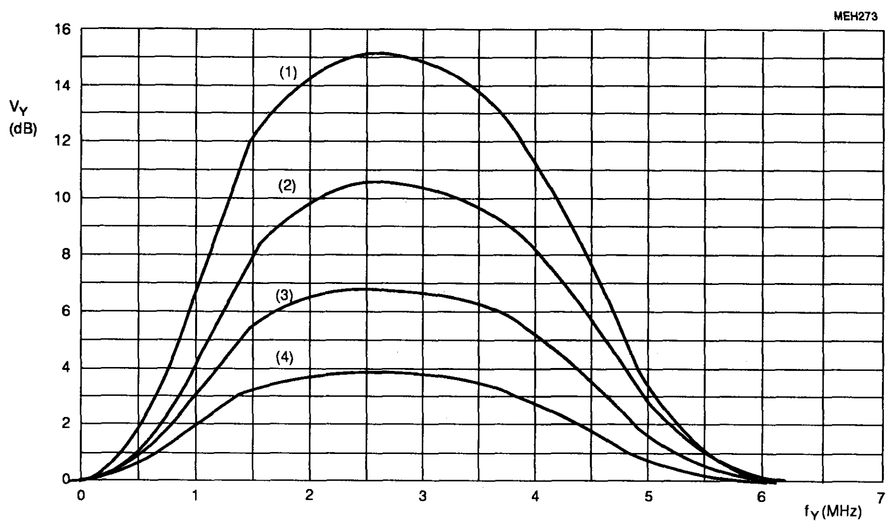


Fig.6 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 1 and BFB = 0:
(1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

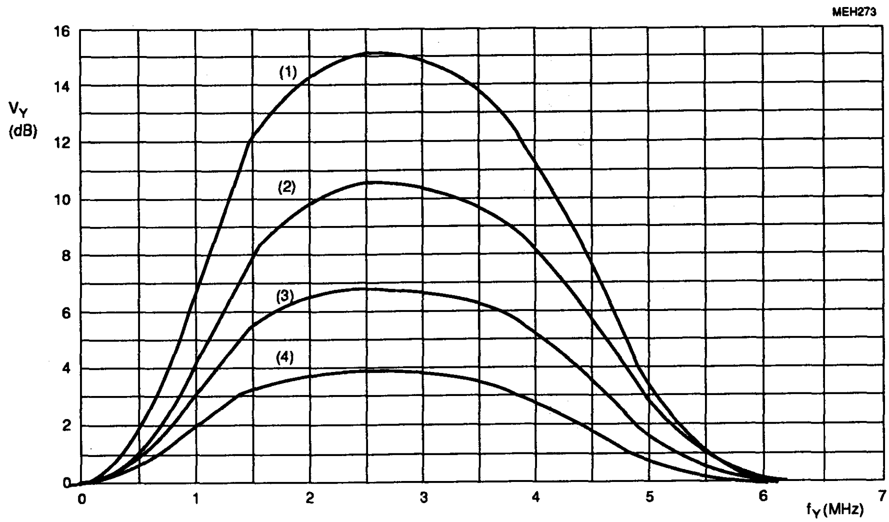


Fig.7 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 0 and BFB = 0:
(1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

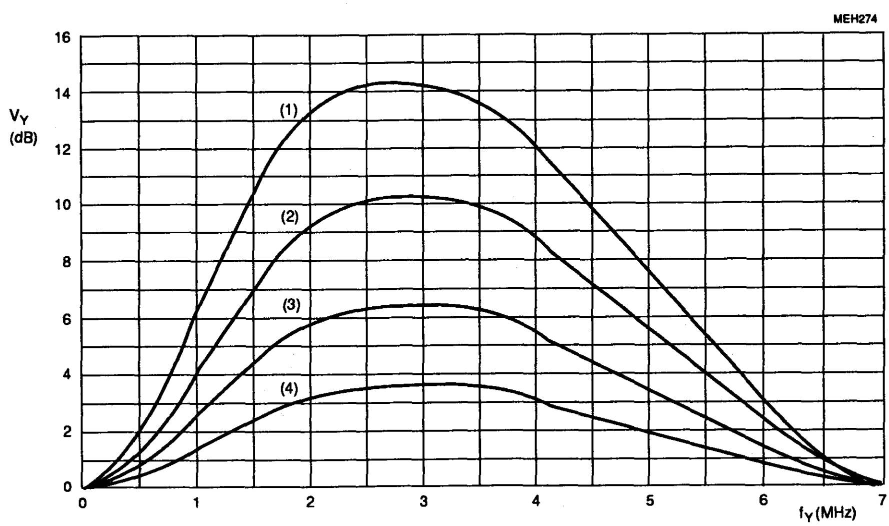


Fig.8 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 1 and BFB = 0:
(1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

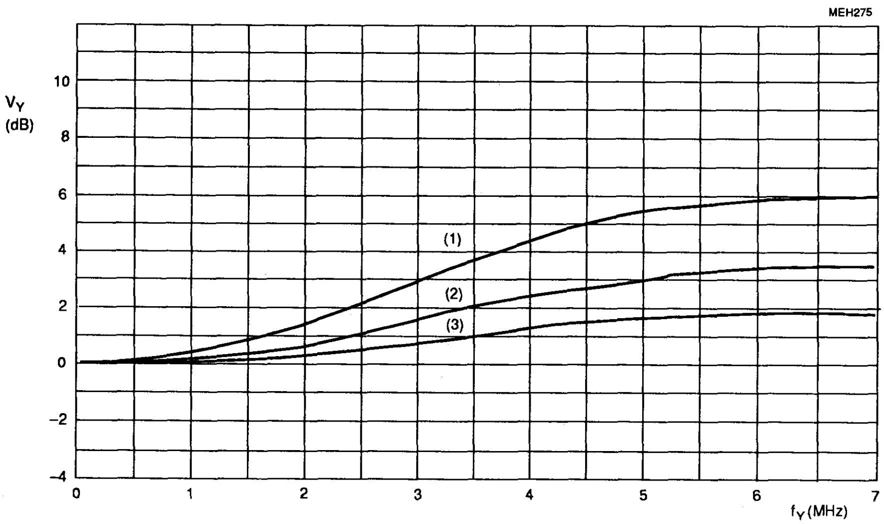


Fig.9 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 1; bandpass filter BF1 bypassed and peaking off; (1) K = 1; (2) K = 1/2; (3) K = 1/4.

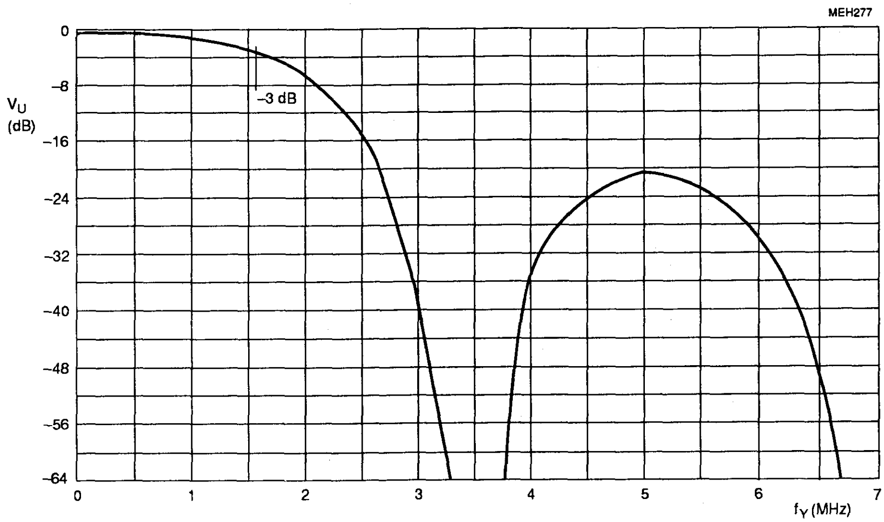


Fig.10 Interpolation filter with I2C-bus control bits IFF = 0; IFC = 0 and IFL = 0 in 4:1:1 format, and control bits IFF = 1; IFC = 0 and IFL = 0 in 4:2:2 format; 13.5 MHz data rate.

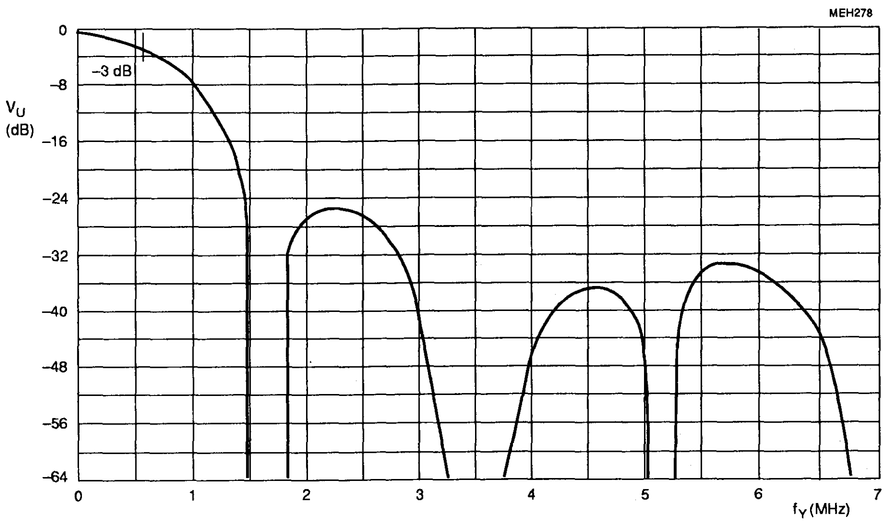


Fig.11 Interpolation filter with I2C-bus control bits IFF = 0; IFC = 0 and IFL = 1 in 4:1:1 format, and control bits IFF = 1; IFC = 0 and IFL = 1 in 4:2:2 format; 13.5 MHz data rate.

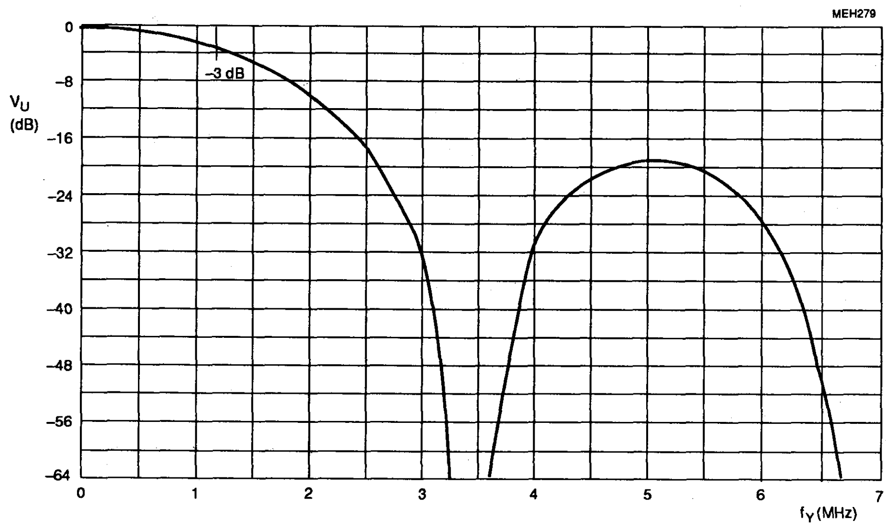


Fig.12 Interpolation filter with I²C-bus control bits IFF = 0; IFC = 1 and IFL = 0 in 4:1:1 format; 13.5 MHz data rate.

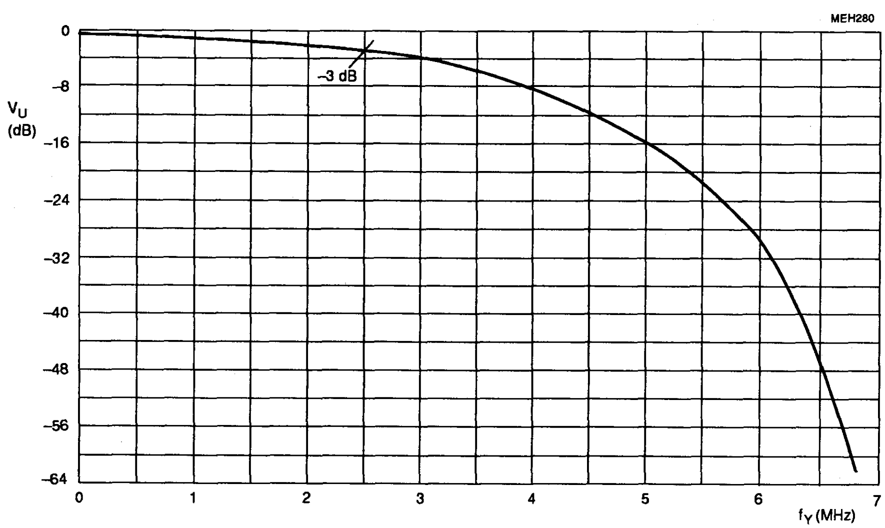


Fig.13 Interpolation filter with I²C-bus control bits IFF = 1; IFC = 1 and IFL = X in 4:2:2 format; 13.5 MHz data rate.

Horizontal combination

TDA2595

GENERAL DESCRIPTION

The TDA2595 is a monolithic integrated circuit intended for use in colour television receivers.

FEATURES

- Positive video input; capacitively coupled (source impedance < 200Ω)
- Adaptive sync separator; slicing level at 50% of sync amplitude
- Internal vertical pulse separator with double slope integrator
- Output stage for vertical sync pulse or composite sync depending on the load; both are switched off at muting
- φ_1 phase control between horizontal sync and oscillator
- Coincidence detector φ_3 for automatic time-constant switching; overruled by the VCR switch
- Time-constant switch between two external time-constants or loop-gain; both controlled by the coincidence detector φ_3
- φ_1 gating pulse controlled by coincidence detector φ_3
- Mute circuit depending on TV transmitter identification
- φ_2 phase control between line flyback and oscillator; the slicing levels for φ_2 control and horizontal blanking can be set separately
- Burst keying and horizontal blanking pulse generation, in combination with clamping of the vertical blanking pulse (three-level sandcastle)
- Horizontal drive output with constant duty cycle inhibited by the protection circuit or the supply voltage sensor
- Detector for too low supply voltage
- Protection circuit for switching off the horizontal drive output continuously if the input voltage is below 4V or higher than 8V
- Line flyback control causing the horizontal blanking level at the sandcastle output continuously in case of a missing flyback pulse
- Spot-suppressor controlled by the line flyback control

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{15-5} = V_P$	Supply voltage (Pin 15)		12		12V
$V_{i(p-p)}$	Sync pulse amplitude (positive video)	50			50mV
I_4	Horizontal output current	50			50mA

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

Horizontal combination | TDA2595

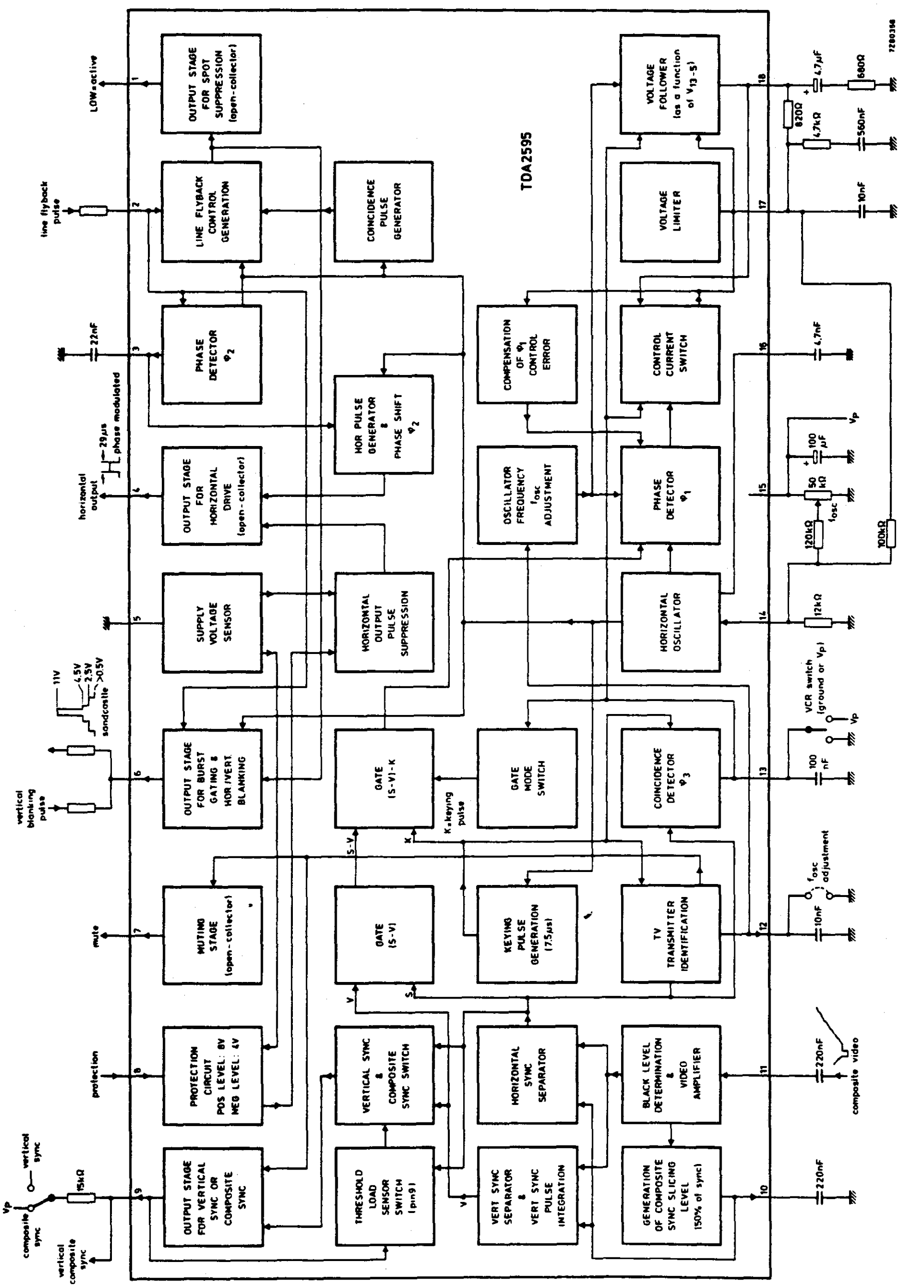


Figure 1. Block Diagram

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (Pin 15)	$V_{15-5} = V_P$	MAX.	13.2	V
Voltages at:				
Pins 1, 4 and 7	$V_{1;4;7-5}$	MAX.	18	V
Pins 8, 13 and 18	$V_{8;13;18-5}$	MAX.	V_P	V
Pin 11 (range)	V_{11-5}	−0.5 to +6		V
Currents at:				
Pin 1	I_1	MAX.	10	mA
Pin 2 (peak value)	$\pm I_{2M}$	MAX.	10	mA
Pin 4	I_4	MAX.	100	mA
Pin 6 (peak value)	$\pm I_{6M}$	MAX.	6	mA
Pin 7	I_7	MAX.	10	mA
Pin 8 (range)	I_8	−5 to +1		mA
Pin 9 (range)	I_9	−10 to +3		mA
Pin 18	$\pm I_{18}$	MAX.	10	mA
Total power dissipation	P_{tot}	MAX.	800	mW
Storage temperature range	T_{stg}	−25 to +125		°C
Operating ambient temperature range	T_{amb}	0 to +70		°C

CHARACTERISTICS

V_P = 12V; T_{amb} = +25°C; measured in Figure 1; unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Composite video input and sync separator (pin 11)					
$V_{11-5(p-p)}$	Input signal (positive video; standard signal; peak-to-peak value)	0.2	1	3	V
$V_{11-5(p-p)}$	Sync pulse amplitude (independent of video content)	50	—	—	mV
R_G	Generator resistance	—	—	200	Ω
	Input current during:				
I_{11}	video	—	5	—	μA
$-I_{11}$	sync pulse	—	40	—	μA
$-I_{11}$	black level	—	25	—	μA
Composite sync generation (pin10) horizontal slicing level at 50% of the sync pulse amplitude for $V_{11-5(p-p)}$ < 1.5V					
	Capacitor current during:				
I_{10}	video	—	16	—	μA
$-I_{10}$	sync pulse	—	170	—	μA
Vertical sync pulse generation slicing level at 30% (60% between black level and horizontal slicing level); pin 9					
V_{9-5}	Output voltage	10	—	—	V
t_p	Pulse duration	—	190	—	μs
t_d	Delay with respect to the vertical sync pulse (leading edge)	—	45	—	μs
	Pulse-mode control				
	output current for vertical sync pulse (dual integrated)	no current applied at pin 9			
	output current for horizontal and vertical sync pulse (non-integrated separated signal)	current applied via a resistor of 15kΩ from V_p to pin 9			
Horizontal oscillator (pins 14 and 16)					
f_{OSC}	Frequency; free running	—	15625	—	Hz
V_{14-5}	Reference voltage for f_{OSC}	—	6	—	V
$\Delta f_{OSC}/\Delta I_{14}$	Frequency control sensitivity	—	31	—	Hz/μA
Δf_{OSC}	Adjustment range of circuit Figure 1	—	±10	—	%
Δf_{OSC}	Spread of frequency	—	—	5	%
	Frequency dependency (excluding tolerance of external components)				
$\frac{\Delta f_{OSC}/f_{OSC}}{\Delta V_{15-5}/V_{15-5}}$	with supply voltage (V_P = 12V)	—	±0.05	—	
Δf_{OSC}	with supply voltage drop of 5V	—	—	10	%
TC	with temperature	—	—	$\pm10^{-4}$	K^{-1}
	Capacitor current during:				
$+I_{16}$	discharging	—	1024	—	μA
$-I_{16}$	charging	—	313	—	μA
	Sawtooth voltage timing (pin 14)				
t_r	rise time	—	49	—	μs
t_f	fall time	—	15	—	μs

CHARACTERISTICS (Continued)

V_P = 12V; T_{amb} = +25°C; measured in Figure 1; unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Horizontal output pulse (pin 4)					
V_{4-5}	Output voltage LOW at I_4 = 50mA	—	—	0.5	V
t_p	Pulse duration (HIGH)	—	29 ± 15	—	µs
V_P	Supply voltage for switching off the output pulse (pin 15)	—	4	—	V
ΔV_P	Hysteresis for switching on the output pulse	—	250	—	mV
Phase comparison φ_1 (pin 17)					
V_{17-5}	Control voltage range	3.55	—	8.3	V
I_{17}	Leakage current at V_{17-5} = 3.55 to 8.3V	—	—	1	µA
$\pm I_{17}$	Control current for external time-constant switch	1.8	2	2.2	mA
$\pm I_{17}$	Control current at $V_{18-5} = V_{15-5}$ and V_{13-5} < 2 or V_{13-5} > 9.5V	—	8	—	mA
$\pm I_{17}$	Control current at $V_{18-5} = V_{15-5}$ and V_{13-5} = 2 to 9.5V	1.8	2	2.2	mA
	Horizontal oscillator control				
$S\varphi$	control sensitivity	6	—	—	kHz/µs
$\pm\Delta f_{OSC}$	catching and holding range	—	680	—	Hz
$\pm\Delta f_{OSC}$	spread of catching and holding range	—	10	—	%
t_p	Internal keying pulse at V_{13-5} = 2.9 to 9.5V	—	7.5	—	µs
	Time-constant switch				
V_{13-5}	slow time-constant at	9.5	—	2	V
V_{13-5}	fast time-constant at	2	—	9.5	V
$\pm V_{17-18}$	Impedance converter offset voltage (slow time-constant)	—	—	3	mV
	Output resistance				
R_{18-5}	slow time-constant	—	—	10	Ω
R_{18-5}	fast time-constant	high impedance			
I_{18}	Leakage current	—	—	1	µA
Coincidence detector φ_3 (pin 13)					
	Output voltage				
V_{13-5}	without coincidence with composite video signal	—	—	1	V
V_{13-5}	without coincidence without composite video signal (noise)	—	—	2	V
V_{13-5}	with coincidence with composite video signal	—	6	—	V
	Output current				
I_{13}	without coincidence with composite video signal	—	50	—	µA
$-I_{13}$	with coincidence with composite video signal	—	300	—	µA
	Switching current				
I_{13}	at $V_{13-5} = V_P - 0.5V$	—	—	100	µA
$I_{13(av)}$	at V_{13-5} = 0.5V (average value)	—	—	100	µA

CHARACTERISTICS (Continued)

V_P = 12V; T_{amb} = +25°C; measured in Figure 1; unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Phase comparison φ_2 (pins 2 and 3) — SEE NOTE 1					
Input for line flyback pulse (pin 2)					
V_{2-5}	Switching level for φ_2 comparison and flyback control	—	3	—	V
V_{2-5}	Switching level for horizontal blanking	—	0.3	—	V
V_{2-5}	Input voltage limiting	—	−0.7	—	V
	or:	—	+4.5	—	V
	Switching current				
I_2	at horizontal flyback	0.01	1	—	mA
I_2	at horizontal scan	—	—	2	µA
$-I_2$	Maximum negative input current	—	—	500	µA
Phase detector output (pin 3)					
$\pm I_3$	Control current for φ_2	—	1	—	mA
$\Delta t\varphi_2$	Control range	—	19	—	µs
$\Delta t/\Delta t_d$	Static control error	—	—	0.2	%
I_3	Leakage current	—	—	5	µA
Δt	Phase relation between middle of the horizontal sync pulse and the middle of the line flyback pulse at t_{fp} = 12µs (NOTE 2)	—	2.6 ± 0.7	—	µs
$\Delta I/\Delta t$	If additional adjustment is required, it can be arranged by applying a current at pin 3	—	30	—	µA / µs
Burst gating pulse (pin 6) (NOTE 3)					
V_{6-5}	Output voltage	10	11	—	V
t_p	Pulse duration	3.7	4	4.3	µs
$t\varphi_6$	Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse at V_{6-5} = 7V	2.15	2.65	3.15	µs
I_6	Output trailing edge current	—	2	—	mA
Horizontal blanking pulse (pin 6) (NOTE 3)					
V_{6-5}	Output voltage	4.1	4.5	4.9	V
I_6	Output trailing edge current	—	2	—	mA
V_{6-5sat}	Saturation voltage at horizontal scan	—	—	0.5	V
Clamping circuit for vertical blanking pulse (pin 6) (NOTE 3)					
V_{6-5}	Output voltage at I_6 = 2.8mA	2.15	2.5	3	V
I_{6min}	Minimum output current at V_{6-5} > 2.15V	—	2.3	—	mA
I_{6max}	Maximum output current at V_{6-5} < 3V	—	3.3	—	mA
TV-transmitter identification (pin 12) (NOTE 4)					
	Output voltage				
V_{12-5}	no TV transmitter	—	—	1	V
V_{12-5}	TV transmitter identified	7	—	—	V

CHARACTERISTICS (Continued)

V_P = 12V; T_{amb} = +25°C; measured in Figure 1; unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Mute output (pin 7)					
V_{7-5}	Output voltage at I_7 = 3mA; no TV transmitter	—	—	0.5	V
R_{7-5}	Output resistance at I_7 = 3mA; no TV transmitter	—	—	100	Ω
I_7	Output leakage current at V_{12-5} > 3V; TV transmitter identified	—	—	5	μA
Protection circuit (beam-current/EHT voltage protection) (pin 8)					
V_{8-5}	No-load voltage for I_8 = 0 (operative condition)	—	6	—	V
V_{8-5}	Threshold at positive-going voltage	—	8 ± 0.8	—	V
V_{8-5}	Threshold at negative-going voltage	—	4 ± 0.4	—	V
$\pm I_8$	Current limiting for V_{8-5} = 1 to 8.5V	—	60	—	μA
R_{8-5}	Input resistance for V_{8-5} > 8.5V	—	3	—	kΩ
t_d	Internal response delay of threshold switch	—	10	—	μs
Control output of line flyback pulse control (pin 1)					
V_{1-5sat}	Saturation voltage at standard operation; I_1 = 3mA	—	—	0.5	V
I_1	Output leakage current in case of disturbance of line flyback pulse	—	—	5	μA

NOTES TO THE CHARACTERISTICS:

1. Phase comparison between horizontal oscillator and the line flyback pulse. Generation of a phase modulated (φ_2) horizontal output pulse with constant duration.
2. t_{fp} is the line flyback pulse duration.
3. Three-level sandcastle pulse.
4. If pin 12 is connected to V_P the vertical output is active independent of synchronization state.

GENERAL DESCRIPTION

The TDA3566A is a monolithic integrated decoder for the PAL and/or NTSC colour television standards. It combines all functions required for the identification and demodulation of PAL/NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 4 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analog as well as digital, which can be used for text display systems (e.g. Teletext/broadcast antiope), channel number display, etc.

FEATURES

- A black-current stabilizer which controls the black-currents of the three electron-guns to a level low enough to omit the black-level adjustment
- Contrast control of inserted RGB signals
- No black-level disturbance when non-synchronized external RGB signals are available on the inputs
- NTSC capability with hue control

QUICK REFERENCE DATA

All voltages referenced to ground.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 1)		-	12	-	V
I_P	supply current (pin 1)		-	90	-	mA
Luminance amplifier (pin 8)						
$V_{8\,(p\text{-}p)}$	input voltage (peak-to-peak value)		-	450	-	mV
-	contrast control range		-	16.5	-	dB
Chrominance amplifier (pin 4)						
$V_{4\,(p\text{-}p)}$	input voltage range (peak-to-peak value)			40 to 1100	-	mV
-	saturation control range		50	-	-	dB
RGB matrix and amplifiers						
$V_{13,\,15,\,17\,(p\text{-}p)}$	output voltage at nominal luminance and contrast (peak-to-peak value)		-	3.8	-	V
Data insertion						
$V_{12,\,14,\,16\,(p\text{-}p)}$	input signals (peak-to-peak value)		-	1	-	V
Data blanking (pin 9)						
V_9	input voltage for data insertion		0.9	-	-	V
Sandcastle input (pin 7)						
V_7	blanking input voltage		-	1.5	-	V
V_7	burst gating and clamping input voltage		-	7	-	V

PAL/NTSC Decoder TDA3566A

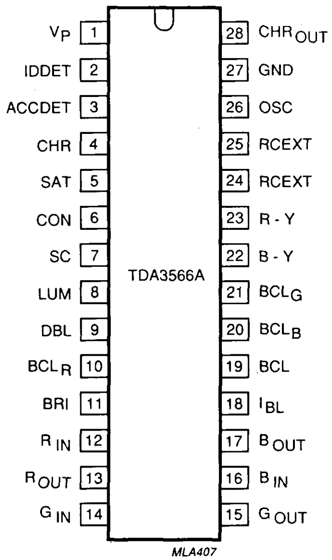


Fig.1 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage
IDDET	2	identification detection level
ACCDET	3	ACC detection level
CHR	4	chrominance control input
SAT	5	saturation control input
CON	6	contrast control input
SC	7	sandcastle input
LUM	8	luminance control input
DBL	9	data blanking input
BCL_R	10	black clamp level for R output
BRI	11	brightness input
R_{IN}	12	red input
R_{OUT}	13	red output
G_{IN}	14	green input
G_{OUT}	15	green output
B_{IN}	16	blue input
B_{OUT}	17	blue output
I_{BL}	18	black current input
BCL	19	black clamp level (ref. black level)
BCL_B	20	black clamp level for B output
BCL_G	21	black clamp level for G output
B-Y	22	demodulator input
R-Y	23	demodulator input
RCEXT	24	gated burst detector load network
RCEXT	25	gated burst detector load network
OSC	26	oscillator frequency input
GND	27	ground
CHR_{OUT}	28	chrominance signal output

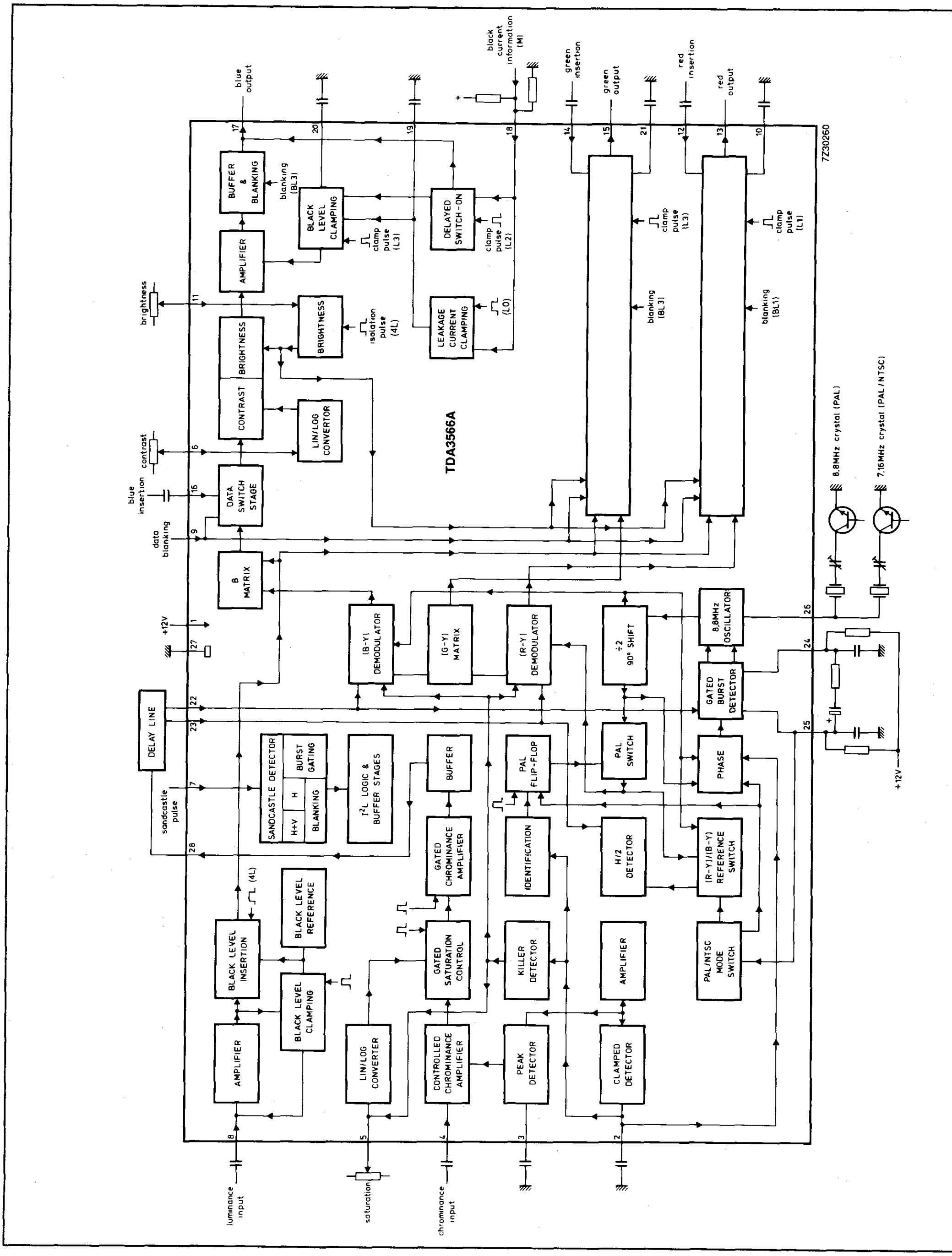


Fig.2 Block diagram; for explanation of pulse mnemonics see Fig.7

FUNCTIONAL DESCRIPTION

The TDA3566A is a further development of the TDA3562A. It has the same pinning and almost the same application. The differences between the TDA3562A and the TDA3566A are as follows:

- The NTSC-application has largely been simplified. In the case of NTSC the chrominance signal is now internally coupled to the demodulators, automatic chrominance control (ACC) and phase detectors. The chrominance output signal (pin 28) is suppressed in this case. It follows that the external switches and filters which are needed for the TDA3562A are not needed for the TDA3566A. Furthermore there is no difference between the amplitude of the colour output signals in the PAL or NTSC mode.
- The clamp capacitors connected to the pins 10, 20 and 21 can be reduced to 100 nF for the TDA3566A provided the stability of the loop is maintained. Loop stability depends upon the complete application. The clamp capacitors also receive a pre-bias voltage to avoid coloured background during switch-on.
- The crystal oscillator circuit has been changed to prevent parasitic oscillations on the third overtone of the crystal. This has the consequence that optimal tuning capacitance must be reduced to 10 pF.
- The hue-control has been improved (linear).

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak (positive video). The luminance delay line must be connected between the IF amplifier and the decoder. The input signal is AC coupled to the input (pin 8). After amplification, the black level at the output of the preamplifier is clamped to a fixed DC level by the black level clamping circuit. During three line periods after vertical blanking, the luminance signal is blanked out and the black level reference voltage is inserted by a switching circuit. This black level reference voltage is controlled via pin 11 (brightness). At the same time the RGB signals are clamped. Noise and residual signals have no influence during clamping thus simple internal clamping circuitry is used.

Chrominance amplifiers

The chrominance amplifier has an asymmetrical input. The input signal must be AC coupled (pin 4) and have a minimum amplitude of 40 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal must not exceed 1.1 V peak-to-peak, otherwise clipping of the input signal will occur. From the gain control stage the chrominance signal is fed to the saturation control stage. Saturation is linear controlled via pin 5. The control voltage range is 2 to 4 V, the input impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by saturation control. The signal is then fed to a gated amplifier which has a 12 dB higher gain during the chrominance signal. As a result the signal at the output (pin 28) has a burst-to-chrominance ratio which is 6 dB lower than that of the input signal when the saturation control is set at –6 dB The chrominance output signal is fed to the delay line and, after matrixing, is applied to the demodulator input pins (pins 22 and 23). These signals are fed to the burst phase detector. In the case of NTSC the chrominance signal is internally coupled to the demodulators, ACC and phase detectors.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	-	13.2	V
P_{tot}	total power dissipation	-	1700	mW
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	–25	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3566A	28	DIL	plastic	SOT107

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient	40	K/W

Oscillator and identification circuit

The burst phase detector is gated with the narrow part of the sandcastle pulse (pin 7). In the detector the (R-Y) and (B-Y) signals are added to provide the composite burst signal again. This composite signal is compared with the oscillator signal divided-by-2 ((R-Y) reference signal). The control voltage is available at pins 24 and 25, and is also applied to the 8.8 MHz oscillator. The 4.4 MHz signal is obtained via the divide-by-2 circuit, which generates both the (B-Y) and (R-Y) reference signals and provides a 90° phase shift between them. The flip-flop is driven by pulses obtained from the sandcastle detector. For the identification of the phase at PAL mode, the (R-Y) reference signal coming from the PAL switch, is compared to the vertical signal (R-Y) of the PAL delay line. This is carried out in the H/2 detector, which is gated during burst. When the phase is incorrect, the flip-flop gets a reset from the identification circuit. When the phase is correct, the output voltage of the H/2 detector is directly related to the burst amplitude so that this voltage can be used for the ACC. To avoid 'blooming-up' of the picture under weak input signal conditions the ACC voltage is generated by peak detection of the H/2 detector output signal. The killer and identification circuits get their information from a gated output signal of the H/2 detector. Killing is obtained via the saturation control stage and the demodulators to obtain good suppression. The time constant of the saturation control (pin 5) provides a delayed switch-on after killing. Adjustment of the oscillator is achieved by variation of the burst phase detector load resistance between pins 24 and 25 (see Fig.8). With this application the trimmer capacitor in series with the 8.8 MHz crystal (pin 26) can be replaced by a fixed value capacitor to compensate for unbalance of the phase detector.

Demodulator

The (R-Y) and (B-Y) demodulators are driven by the colour difference signals from the delay-line matrix circuit and the reference signals from the 8.8 MHz divider circuit. The (R-Y) reference signal is fed via the PAL-switch. The output signals are fed to the R and B matrix circuits and to the (G-Y) matrix to provide the (G-Y) signal which is applied to the G-matrix. The demodulation circuits are killed and blanked by-passing the input signals.

NTSC mode

The NTSC mode is switched on when the voltage at the burst phase detector outputs (pins 24 and 25) is adjusted below 9 V. To ensure reliable application the phase detector load resistors are external. When the TDA3566A is used only for PAL these two 33 kΩ resistors must be connected to +12 V (see Fig.8). For PAL/NTSC application the value of each resistor must be reduced to 20 kΩ (with a tolerance of 1%) and connected to the slider of a potentiometer (see Fig.9). The switching transistor brings the voltage at pins 24 and 25 below 9 V which switches the circuit to the NTSC mode. The position of the PAL flip-flop ensures that the correct phase of the (R-Y) reference signal is supplied to the (R-Y) demodulator. The drive to the H/2 detector is now provided by the (B-Y) reference signal. (In the PAL mode it is driven by the (R-Y) reference signal. Hue control is realized by changing the phase of the reference drive to the burst phase detector. This is achieved by varying the voltage at pins 24 and 25 between 7.0 V and 8.5 V, nominal position 7.65 V. The hue-control characteristic is shown in Fig.6.

RGB matrix and amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described. The luminance and the colour difference signals are added in the matrix circuit to obtain the colour signal, which is then fed to the contrast control stage. The contrast control voltage is supplied to pin 6 (high-input impedance). The control range is +5 dB to −11.5 dB nominal. The relationship between the control voltage and the gain is linear (see Fig.3). During the 3-line period after blanking a pulse is inserted at the output of the contrast control stage. The amplitude of this pulse is varied by a control voltage at pin 11. This applies a variable offset to the normal black level, thus providing brightness control. The brightness control range is 1 V to 3.6 V. While this offset level is present, the 'black-current' input impedance (pin 18) is high and the internal clamp circuit is activated. The clamp circuit then compares the reference voltage at pin 19 with the voltage developed across the external resistor network RA and RB (pin 18) which is provided by picture tube beam current. The output of the comparator is stored in capacitors connected from pins 10, 20 and 21 to ground which controls the black level at the output. The reference voltage is composed by the resistor divider network and the leakage current of the picture tube into this bleeder. During vertical blanking, this voltage is stored in the capacitor connected to pin 19, which ensures that the leakage current of the CRT does not influence the black current measurement. The RGB output signals can never exceed a level of 10.6 V. When the signal tends to exceed this level the output signal is clipped. The black level at the outputs (pins 13, 15 and 17) will be about 3 V. This level depends on the spread of the guns of the picture tube. If a beam current stabilizer is not used it is possible to stabilize the black levels at the outputs, which in this application must be connected to the black current measuring input (pin 18) via a resistor network.

Data insertion

Each colour amplifier has a separate input for data insertion. A 1 V peak-to-peak input signal provides a 3.8 V peak-to-peak output signal. To avoid the 'black-level' of the inserted signal differing from the black level of the normal video signal, the data is clamped to the black level of the luminance signal. Therefore AC coupling is required for the data inputs. To avoid a disturbance of the blanking level due to the clamping circuit, the source impedance of the driver circuit must not exceed 150 Ω. The data insertion circuit is activated by the data blanking input (pin 9). When the voltage at this pin exceeds a level of 0.9 V, the RGB matrix circuits are switched off and the data amplifiers are switched on. To avoid coloured edges, the data blanking switching time is short. The amplitude of the data output signals is controlled by the contrast control at pin 6. The black level is equal to the video black level and can be varied between 2 and 4 V (nominal condition) by the brightness control voltage at pin 11. Non-synchronized data signals do not disturb the black level of the internal signals.

Blanking of RGB and data signals

Both the RGB and data signals can be blanked via the sandcastle input (pin 7). A slicing level of 1.5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking a level of +1 V is available at the output. To prevent parasitic oscillations on the third overtone of the crystal the optimal tuning capacitance should be 10 pF.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; all voltages are referenced to pin 27; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 1)						
V_P	supply voltage		10.8	12	13.2	V
I_P	supply current		-	90	120	mA
P_{tot}	total power dissipation		-	1.1	1.6	W
Luminance amplifier (pin 8)						
$V_{8\ (p\text{-}p)}$	input voltage (peak-to-peak value)	note 1	-	0.45	0.63	V
V_8	input level before clipping		-	-	1.4	V
I_8	input current		-	0.1	1	μA
-	contrast control range	see Fig.3	-	−11.5 to +5	-	dB
I_7	input current contrast control		-	-	15	μA
Chrominance amplifier (pin 4)						
$V_{4\ (p\text{-}p)}$	input voltage (peak-to-peak value)	note 2	40	390	1100	mV
$\|Z_4\|$	input impedance (pin 4)		-	10	-	kΩ
C_4	input capacitance		-	-	6.5	pF
-	ACC control range		30	-	-	dB
ΔV	change of the burst signal at the output over the whole control range	100 mV to 1 $V_{p\text{-}p}$	-	-	1	dB
G	gain at nominal contrast/saturation pin 4 to pin 28	note 3	34	-	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Chrominance amplifier (pin 4)						
-	chrominance to burst ratio at nominal saturation		-	7	-	dB
$V_{28\ (p\text{-}p)}$	maximum output voltage range (peak-to-peak value)	RL = 2 kΩ	4	5	-	V
d	distortion of chrominance amplifier	output; at $V_{28(p\text{-}p)}$ = 2 V input; up to $V_{4\ (p\text{-}p)}$ = 1 V	-	-	5	%
$\alpha_{28\text{-}4}$	frequency response between 0 and 5 MHz		-	-	−2	dB
-	saturation control range	see Fig.4	50	-	-	dB
I_5	input current saturation control; (pin 5)		-	-	20	μA
-	cross-coupling between luminance and chrominance amplifier	note 4	-	-	−46	dB
S/N	signal-to-noise ratio at nominal input signal	note 5	56	-	-	dB
$\Delta\varphi$	phase shift between burst with respect to chrominance at nominal saturation		-	-	±5	deg
$\lvert Z_{28} \rvert$	output impedance of chrominance amplifier		-	10	-	Ω
I_{28}	output current		-	-	15	mA
Reference part						
Δf	phase-locked-loop catching range	note 6	500	-	-	Hz
$\Delta\varphi$	phase shift for 400 Hz deviation of f_{osc}	note 6	-	-	5	deg
TC_{osc}	oscillator temperature coefficient of oscillator frequency	note 6	-	−2	−3	Hz/K
Δf_{osc}	frequency variation when supply voltage increases from 10 to 13.2 V	note 6	-	40	100	Hz
R_{26}	input resistance (pin 26)		280	400	520	Ω
C_{26}	input capacitance (pin 26)		-	-	10	pF
ACC generation (pin 2; note 7)						
V_2	control voltage at nominal input signal		-	4.5	-	V
V_2	control voltage without chrominance input		-	2	-	V
ΔV_2	colour-on-off voltage		175	300	425	mV
V_2	colour-on voltage		3.1	3.5	3.9	V
ΔV_2	colour-on identification voltage		1.2	1.5	1.8	V
-	change in burst amplitude with temperature		-	0.1	0.25	%/K
V_3	voltage at pin 3 at nominal input signal		-	4.7	-	V
Demodulator part						
$V_{23\ (p\text{-}p)}$	input burst signal amplitude (peak-to-peak value) between pins 23 and 27	note 8	45	63	81	mV
$\frac{V_{22}}{V_{23}}$	input impedance between pins 22 or 23 and 27		0.7	1	1.3	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RATIO OF DEMODULATED SIGNALS FOR EQUIVALENT INPUT SIGNALS AT PINS 22 AND 23						
$\frac{V_{17}}{V_{13}}$	(B-Y)/(R-Y)		-	1.78 ±10%	-	
$\frac{V_{15}}{V_{13}}$	(G-Y)/(R-Y)	no (B-Y) signal	-	−0.51 ±10%	-	
$\frac{V_{15}}{V_{17}}$	(G-Y)/(B-Y)	no (R-Y) signal	-	−0.19 ±25%	-	
α_{17}	frequency response between 0 and 1 MHz		-	-	−3	dB
-	cross-talk between colour difference signals		40	-	-	dB
$\Delta\varphi$	total phase difference between chrominance input signals and demodulator output signals		-	-	8	deg
$\Delta\varphi$	phase difference between (R-Y) and (B-Y) reference signals		85	90	95	deg
RGB matrix and amplifiers						
$V_{13, 15, 17(p-p)}$	output voltage (peak-to-peak value) at nominal luminance/contrast (black-to-white)	note 3	3.3	3.8	4.3	V
$V_{13(p-p)}$	output voltage at pin 13 (peak-to-peak value) at nominal contrast/saturation and no luminance signal to (R-Y)		-	3.7	-	V
$V_{13, 15, 17 (m)}$	maximum peak-white level		9.4	10.0	10.6	V
$I_{13, 15, 17}$	available output current (pins 13, 15, 17)		10	-	-	mA
$\Delta V_{13, 15, 17}$	difference between black level and measuring level at the output for a brightness control voltage at pin 11 of 2 V	note 9	-	0	-	V
ΔV	difference in black level between the three channels for equal drive conditions for the three gains	note 10	-	-	100	mV
-	control range of black-current stabilization at V_{bl} = 3 V; V_{11} = 2 V		-	-	±2	V
ΔV	black level shift with vision contents		-	-	40	mV
-	brightness control voltage range	see Fig.5	-	-	-	
I_{11}	brightness control input current		-	-	5	μA
$\frac{DV}{DT}$	variation of black level with temperature		-	0	-	mV/K
ΔV	variation of black level with contrast (+5 to −10 dB)	note 11	-	-	100	mV
-	relative spread between the R, G, and B output signals		-	-	10	%
ΔV	relative black-level variation between the three channels during variation of contrast, brightness and supply voltage (±10 %)	note 11	-	0	20	mV
V_{blk}	blanking level at the RGB outputs		-	0.85	1.1	V
V_{blk}	difference in blanking level of the three channels		-	0	10	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{blk}	differential drift of the blanking levels over a temperature range of 40 °C		-	0	10	mV
$\frac{DV_{bl}}{V_{bl}} x \frac{V_{PI}}{DV_{PI}}$	tracking of output black level with supply voltage		0.9	1	1.1	
-	tracking of contrast control between the three channels over a control range at 10 dB		-	-	0.5	dB
V_o	output voltage during test pulse after switch-on		6.5	7.3	-	V
S/N	signal-to-noise ratio of output signals	note 5	62	-	-	dB
$V_{R\ (p\text{-}p)}$	residual 4.4 MHz signal at RGB outputs (peak-to-peak value)		-	-	100	mV
$V_{R\ (p\text{-}p)}$	residual 8.8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)		-	-	150	mV
$\|Z_{13}\|$	output impedance		-	100	-	Ω
$\|Z_{15}\|$	output impedance		-	100	-	Ω
$\|Z_{17}\|$	output impedance		-	100	-	Ω
α	frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz		-	−1	−3	dB
I_o	current source of output stage		2	3	-	mA
ΔV	difference of black level at the three outputs at nominal brightness	note 11	-	-	10	mV
-	tracking of brightness control		-	-	2	%
Signal insertion (pins 12, 14 and 16)						
$V_{12,\ 14,\ 16(p\text{-}p)}$	input signals (peak-to-peak value) for an RGB output voltage of 3.8 V (peak-to-peak) at nominal contrast	note 3	0.9	1	1.1	V
ΔV	difference between the black levels of the RGB signals and the inserted signals at the output	note 12	-	-	170	mV
t_r	output rise time		-	50	80	ns
$I_{12,\ 14,\ 16}$	input current		-	-	10	µA
Data blanking (pin 9)						
V_9	input voltage for no data insertion		-	-	0.3	V
V_9	input voltage for data insertion		0.9	-	-	V
$V_{9\ (m)}$	maximum input voltage		-	-	3	V
t_d	delay of data blanking		-	-	20	ns
R_9	input resistance		7	10	13	kΩ
-	suppression of the internal RGB signals when $V_9 > 0.9$ V		46	-	-	dB
-	suppression of external RGB signals when $V_9 < 0.3$ V		46	-	-	dB
Sandcastle input (note 13)						
V_7	level at which the RGB blanking is activated		1	1.5	2	V
V_7	level at which the horizontal pulses are separated		3	3.5	4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_7	level at which burst gating and clamping pulse are separated		6.5	7.0	7.5	V
t_d	delay between black level clamping and burst gating pulse		-	0.6	-	μs
$-I_7$	input current at V_7 = 0 to 1 V		-	-	−1	mA
I_7	input current at V_7 = 1 to 8 V		-	-	50	μA
I_7	input current at V_7 = 8 to 12 V		-	-	2	mA
Black current stabilization (pin 18)						
V_8	bias voltage (DC)		3.5	5	7.0	V
ΔV	difference between input voltage for 'black' current and leakage current		0.35	0.5	0.65	V
I_8	input current during 'black' current		-	-	1	μA
I_8	input current during scan		-	-	10	mA
V_{18}	internal limiting at pin 18		8.5	9	9.5	V
V_{18}	switching threshold for 'black' current control ON		7.6	8	8.4	V
R_{18}	input resistance during scan		1	1.5	2	kΩ
$I_{10,\ 20\ and\ 21}$	input current during scan at pins 10, 20 and 21		-	-	30	nA
-	maximum charge or discharge current during measuring time pins 10, 20 and 21		-	1	-	mA
-	difference in drift of the blank level over a temperature range of 40 °C	note 11	-	0	20	mV
NTSC						
$V_{24\text{-}25}$	level at which the PAL/NTSC switch is activated (pins 24 and 25)		-	8.8	9.2	V
$I_{24+25\ (AV)}$	average output current	note 14	62	82.5	103	μA
-	hue control	see Fig.6	-	-	-	

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a colour bar with 75 % saturation; chrominance to burst ratio is 2.2 : 1.
3. Nominal contrast is specified as the maximum contrast −5 dB and nominal saturation as the maximum saturation −6dB. This figure is valid in the PAL condition. In the NTSC condition output signal is available on pin 28.
4. Cross coupling is measured under the following condition: input signal nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to RMS noise.
6. All frequency variations are referred to 4.4 MHz carrier frequency. All oscillator specifications have been measured with the Philips crystal 4322 143 ... or 4322 144 ... series.
7. The change in burst with V_P is proportional.
8. These signal amplitudes are determined by the ACC circuit of the reference part.

Notes to the characteristics

9. This value depends on the gain setting of the RGB output amplifiers and the drift of the picture tube guns. Higher black level values are possible (up to 5 V) but in that application the amplitude of the output signal is reduced.
10. The variation of the black-level during brightness control in the three different channels is directly dependent on the gain of each channel. Discolouration during adjustments of contrast and brightness does not occur because amplitude and the black-level change with brightness control are directly related.
11. With respect to the measuring pulse.
12. This difference occurs when the source impedance of the data signals is 150 Ω and the black level clamp pulse width is 4 μs (sandcastle pulse). For a lower impedance the difference will be lower.
13. For correct operating of the black level stabilization loop, the leading and trailing edges of the sandcastle pulse (measured between 1.5 V and 3.5 V) must be within 200 ns and 600 ns respectively.
14. The voltage at pins 24 and 25 can be changed by connecting the load resistors (20 kΩ in this application) to the slider bar of the hue control potentiometer (see Fig.7). When the transistor is switched on, the voltage at pins 24 and 25 is reduced below 9 V, and the circuit is switched to NTSC mode. The width of the burst gate is assumed to be 4 μs typical.

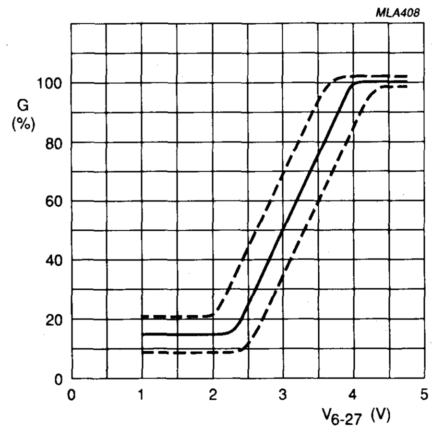


Fig.3 Contrast control voltage range.

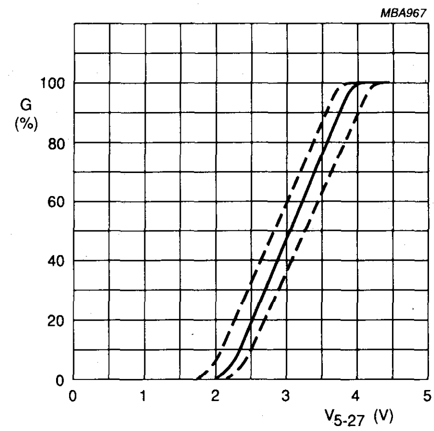


Fig.4 Saturation control voltage range.

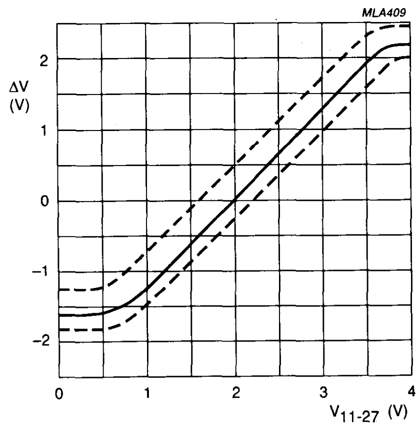


Fig.5 Difference between black level and measuring level at the RGB outputs (ΔV) as a function of the brightness control input voltage (V_{11}).

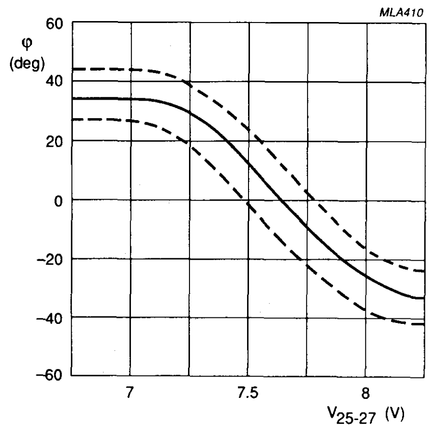


Fig.6 Hue control voltage range.

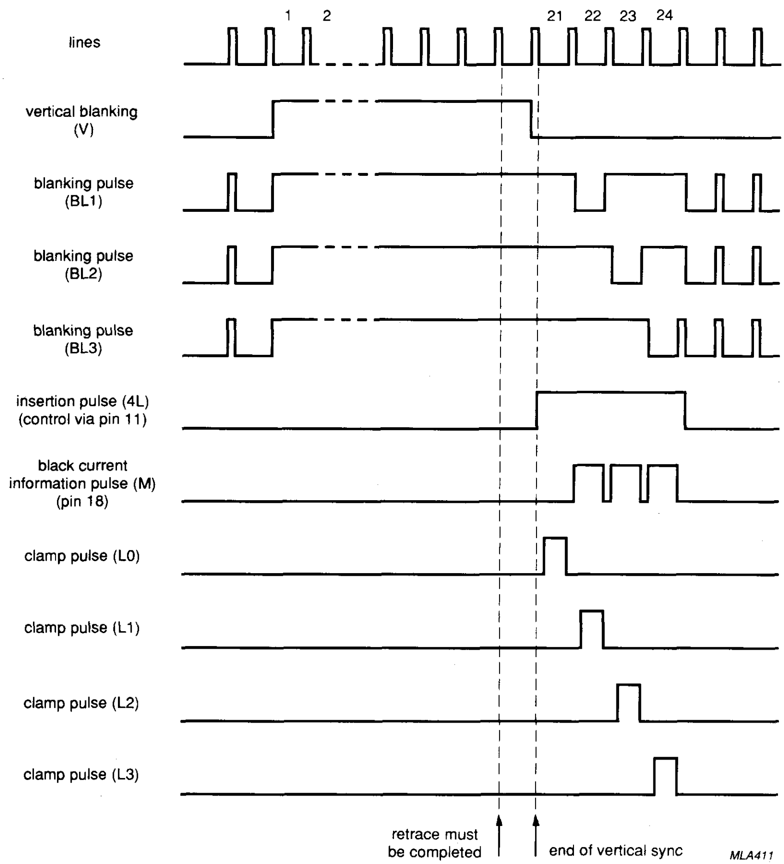


Fig.7 Timing diagram for black-current stabilizing.

APPLICATION DIAGRAMS

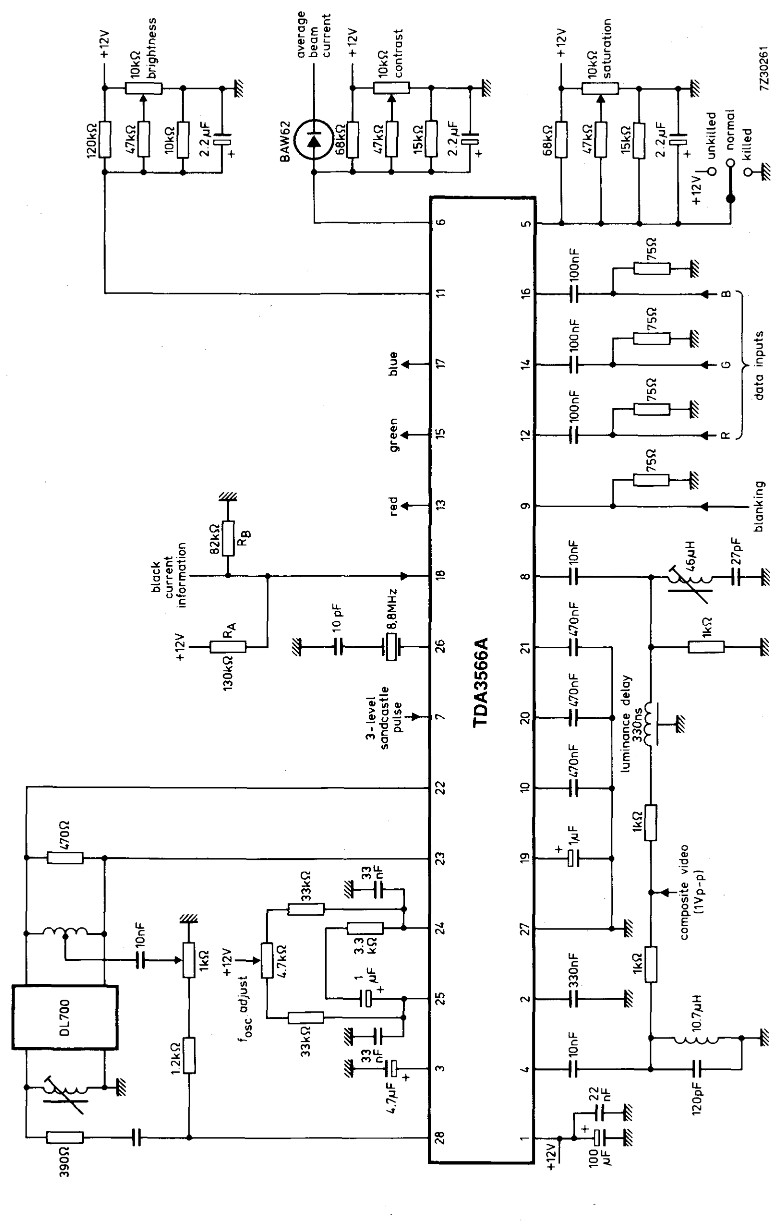


Fig.8 Application diagram showing the TDA3566A for a PAL decoder.

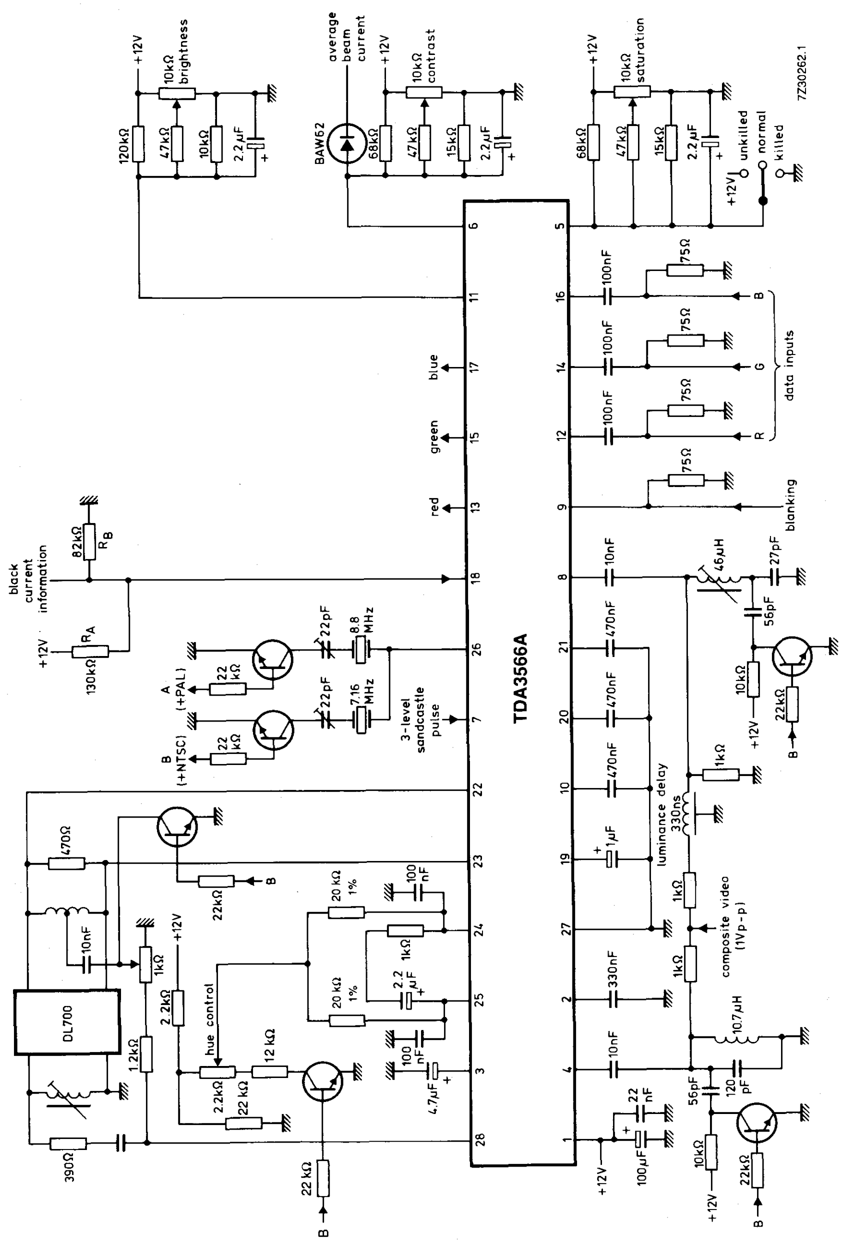


Fig.9 Application diagram showing the TDA3566A for a PAL/NTSC decoder.

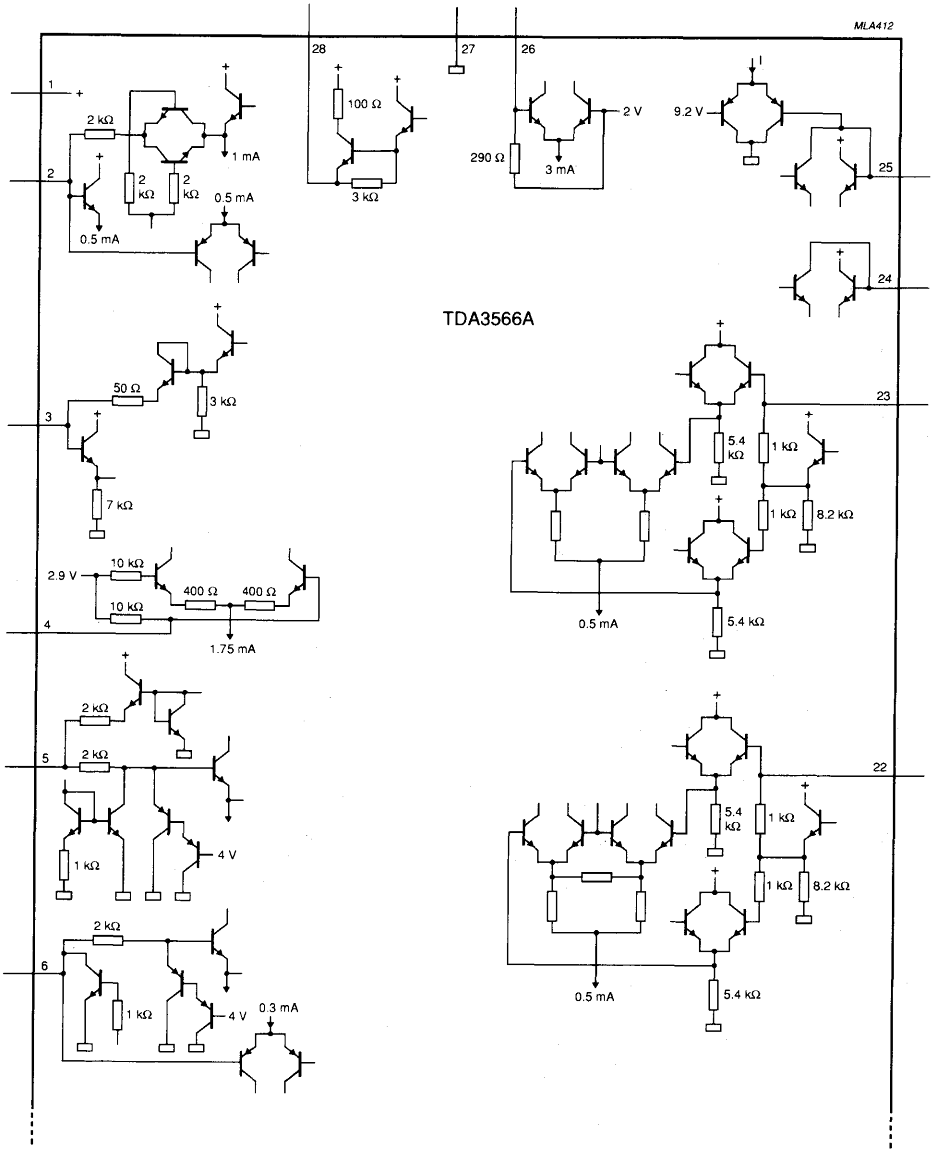


Fig.10 Internal pin circuit diagram (first part).

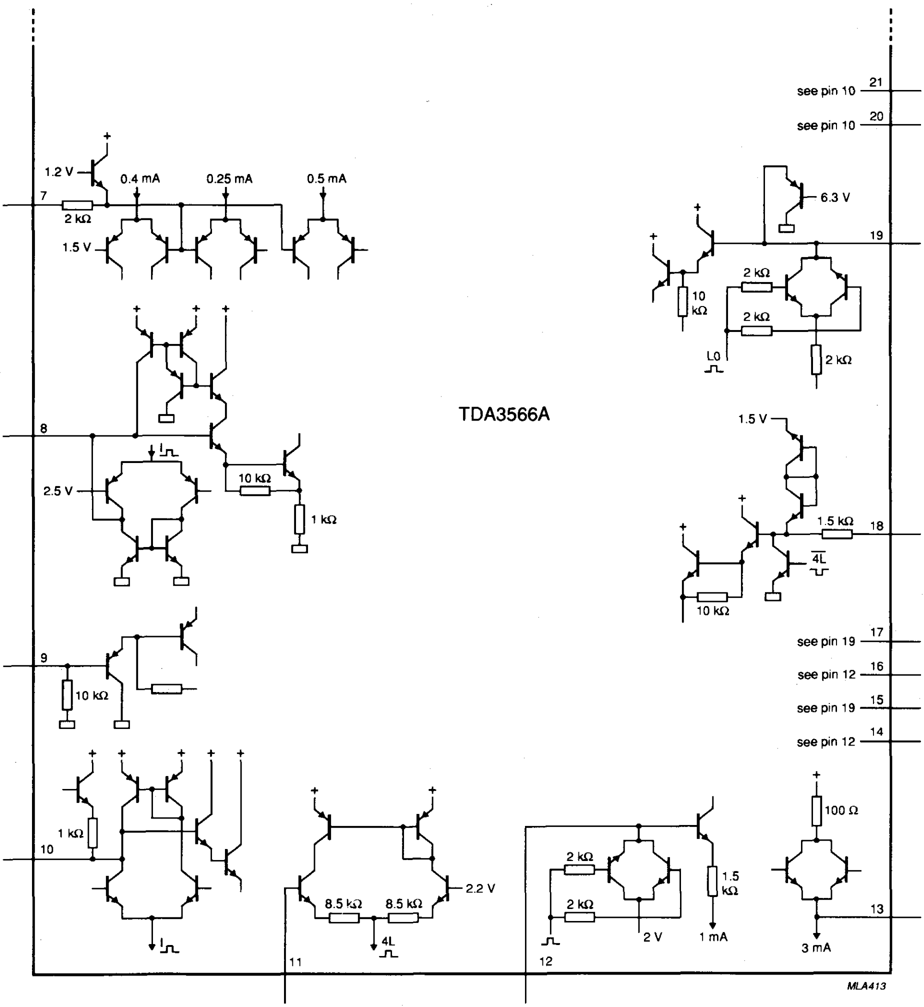


Fig.11 Internal pin circuit diagram (second part).

Baseband delay line

TDA4661

FEATURES

- Two comb filters, using the switched-capacitor technique, for one line delay time (64 μs)
- Adjustment-free application
- No crosstalk between SECAM colour carriers
- Handles negative or positive colour-difference input signals
- Clamping of AC-coupled input signals (±(R–Y) and ±(B–Y))
- VCO without external components
- 3 MHz internal clock signal derived from a 6 MHz CCO, line-locked by the sandcastle pulse (64 μs line)
- Sample-and-hold circuits and low-pass filters to suppress the 3 MHz clock signal
- Addition of delayed and non-delayed output signals
- Output buffer amplifiers
- Comb filtering functions for NTSC colour-difference signals to suppress cross-colour

GENERAL DESCRIPTION

The TDA4661 is an integrated baseband delay line circuit with one line delay. It is suitable for decoders with colour-difference signal outputs ±(R–Y) and ±(B–Y).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{P1}	analog supply voltage (pin 9)	4.5	5	6	V
V_{P2}	digital supply voltage (pin 1)	4.5	5	6	V
$I_{P\,tot}$	total supply current	–	5.9	7.0	mA
V_i	±(R–Y) input signal PAL/NTSC (peak-to-peak value, pin 16)	–	525	–	mV
	±(B–Y) input signal PAL/NTSC (peak-to-peak value, pin 14)	–	665	–	mV
	±(R–Y) input signal SECAM (peak-to-peak value, pin 16)	–	1.05	–	V
	±(B–Y) input signal SECAM (peak-to-peak value, pin 14)	–	1.33	–	V
G_v	gain V_o / V_i of colour-difference output signals				
	V_{11} / V_{16} for PAL and NTSC	5.3	5.8	6.3	dB
	V_{12} / V_{14} for PAL and NTSC	5.3	5.8	6.3	dB
	V_{11} / V_{16} for SECAM	–0.6	–0.1	+0.4	dB
	V_{12} / V_{14} for SECAM	–0.6	–0.1	+0.4	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4661	16	DIL	plastic	SOT38-4
TDA4661T	16	mini-pack	plastic	SOT109A

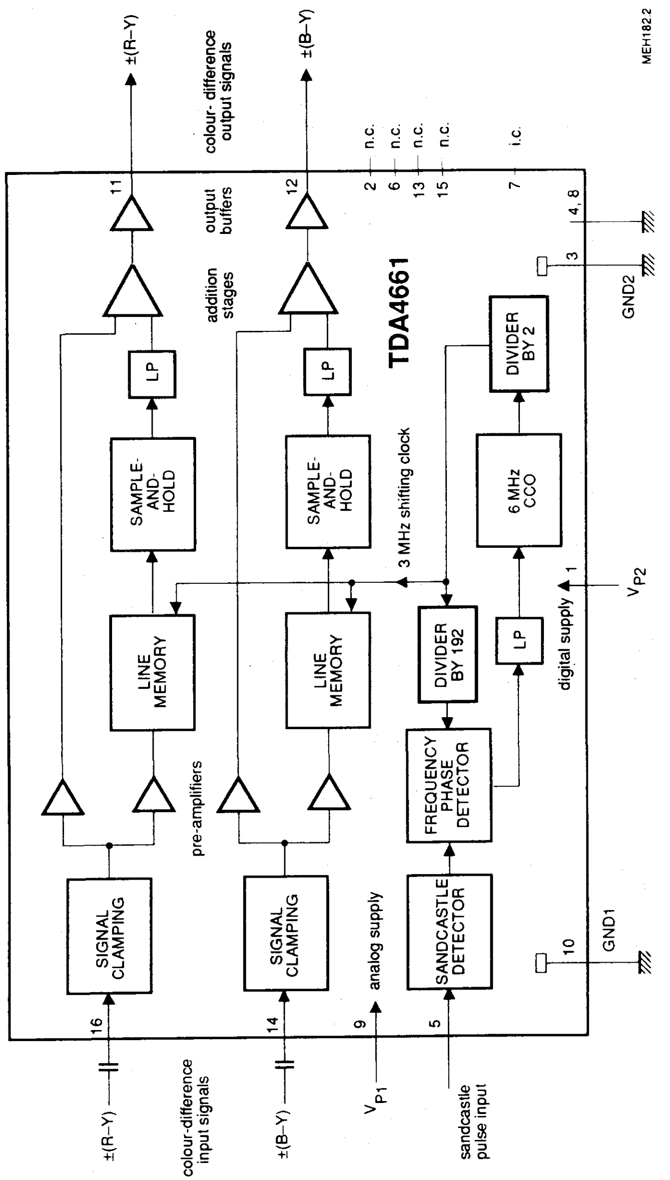


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P2}	1	+5 V supply voltage for digital part
n.c.	2	not connected
GND2	3	ground for digital part (0 V)
i.c.	4	internally connected
SAND	5	sandcastle pulse input
n.c.	6	not connected
i.c.	7	internally connected
i.c.	8	internally connected
V_{P1}	9	+5 V supply voltage for analog part
GND1	10	ground for analog part (0 V)
$V_{o\,(R-Y)}$	11	±(R–Y) output signal
$V_{o\,(B-Y)}$	12	±(B–Y) output signal
n.c.	13	not connected
$V_{i\,(B-Y)}$	14	±(B–Y) input signal
n.c.	15	not connected
$V_{i\,(R-Y)}$	16	±(R–Y) input signal

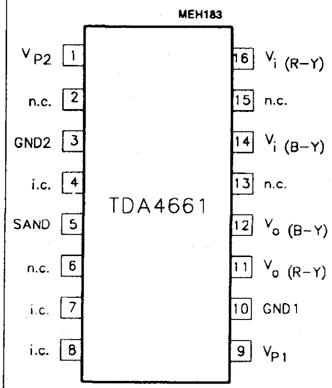


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)
Ground pins 3 and 10 connected together

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 9)	−0.5	+7	V
V_{P2}	supply voltage (pin 1)	−0.5	+7	V
V_5	voltage on pin 5	−0.5	V_P + 1.0	V
V_n	voltage on pins 11, 12, 14 and 16	−0.5	V_P	V
T_{stg}	storage temperature range	−25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling for all pins (note 1)	–	±500	V

Note to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\,j-a}$	from junction to ambient in free air	
	SOT38-4	75 K/W
	SOT109A	220 K/W

CHARACTERISTICS

V_P = 5.0 V; input signals as specified in characteristics with 75% colour bars; super-sandcastle frequency of 15.625 kHz; T_{amb} = +25 °C, measurements taken in Fig.3 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage (analog part, pin 9)		4.5	5	6	V
V_{P2}	supply voltage (digital part, pin 1)		4.5	5	6	V
I_{P1}	supply current		–	5.2	6.0	mA
I_{P2}	supply current		–	0.7	1.0	mA
Colour-difference input signals						
V_i	input signal (peak-to-peak value)					
	±(R–Y) PAL and NTSC (pin 16)		–	525	–	mV
	±(B–Y) PAL and NTSC (pin 14)		–	665	–	mV
	±(R–Y) SECAM (pin 16)	note 1	–	1.05	–	V
	±(B–Y) SECAM (pin 14)	note 1	–	1.33	–	V
$V_{i\,max}$	maximum symmetrical input signal (peak-to-peak value)					
	±(R–Y) or ±(B–Y) for PAL and NTSC	before clipping	1	–	–	V
	±(R–Y) or ±(B–Y) for SECAM	before clipping	2	–	–	V
$R_{14,16}$	input resistance		–	–	40	kΩ
$C_{14,16}$	input capacitance		–	–	10	pF
$V_{14,16}$	input clamping voltage	proportional to V_P	1.5	1.6	1.7	V
Colour-difference output signals						
V_o	output signal (peak-to-peak value)					
	±(R–Y) on pin 11	all standards	–	1.05	–	V
	±(B–Y) on pin 12	all standards	–	1.33	–	V
V_{11}/V_{12}	ratio of output amplitudes at equal input signals	$V_{i\,14,16}$ = 1.33 V (p-p)	–0.4	0	+0.4	dB
$V_{11,12}$	DC output voltage	proportional to V_P	2.90	3.10	3.30	V
$R_{11,12}$	output resistance		–	330	400	Ω
G_v	gain for PAL and NTSC	ratio V_o/V_i	5.3	5.8	6.3	dB
	gain for SECAM	ratio V_o/V_i	–0.6	–0.1	+0.4	dB
V_n/V_{n+1}	ratio of output signals on pins 11 and 12 for adjacent time samples at constant input signals	$V_{i\,14,16}$ = 1.33 V (p-p); SECAM signals	–0.1	0	+0.1	dB
V_n	noise voltage (RMS value, pins 11 and 12)	$V_{i\,14,16}$ = 0 V; note 2	–	–	1.2	mV
S/N(W)	weighted signal-to-noise ratio	V_o = 1 V (p-p); f = tbn	–	54	–	dB
t_d	delay of delayed signals		63.94	64.0	64.06	µs
	delay of non-delayed signals		40	60	80	ns
t_{tr}	transient time of delayed signal on pins 11 respectively 12	300 ns transient of SECAM signal	–	350	–	ns
	transient time of non-delayed signal on pins 11 respectively 12	300 ns transient of SECAM signal	–	320	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle pulse input (pin 5)						
f_{BK}	burst-key frequency / sandcastle frequency		14.2	15.625	17.0	kHz
V_5	top pulse voltage	note 3	4.5	–	$V_P + 1.0$	V
V_{slice}	internal slicing level		$V_5 - 1.0$	–	$V_5 - 0.5$	V
I_5	input current		–	–	10	μA
C_5	input capacitance		–	–	10	pF

Notes to the characteristics

1. The signal must be blanked line-sequentially. The blanking level must be equal to the non-colour signal.
2. Noise voltage at f = 10 kHz to 1 MHz; $V_{i\,14,\,16} = 0$ ($R_S < 300\ \Omega$).
3. The leading edge of the burst-key pulse or H-blanking pulse is used for timing.

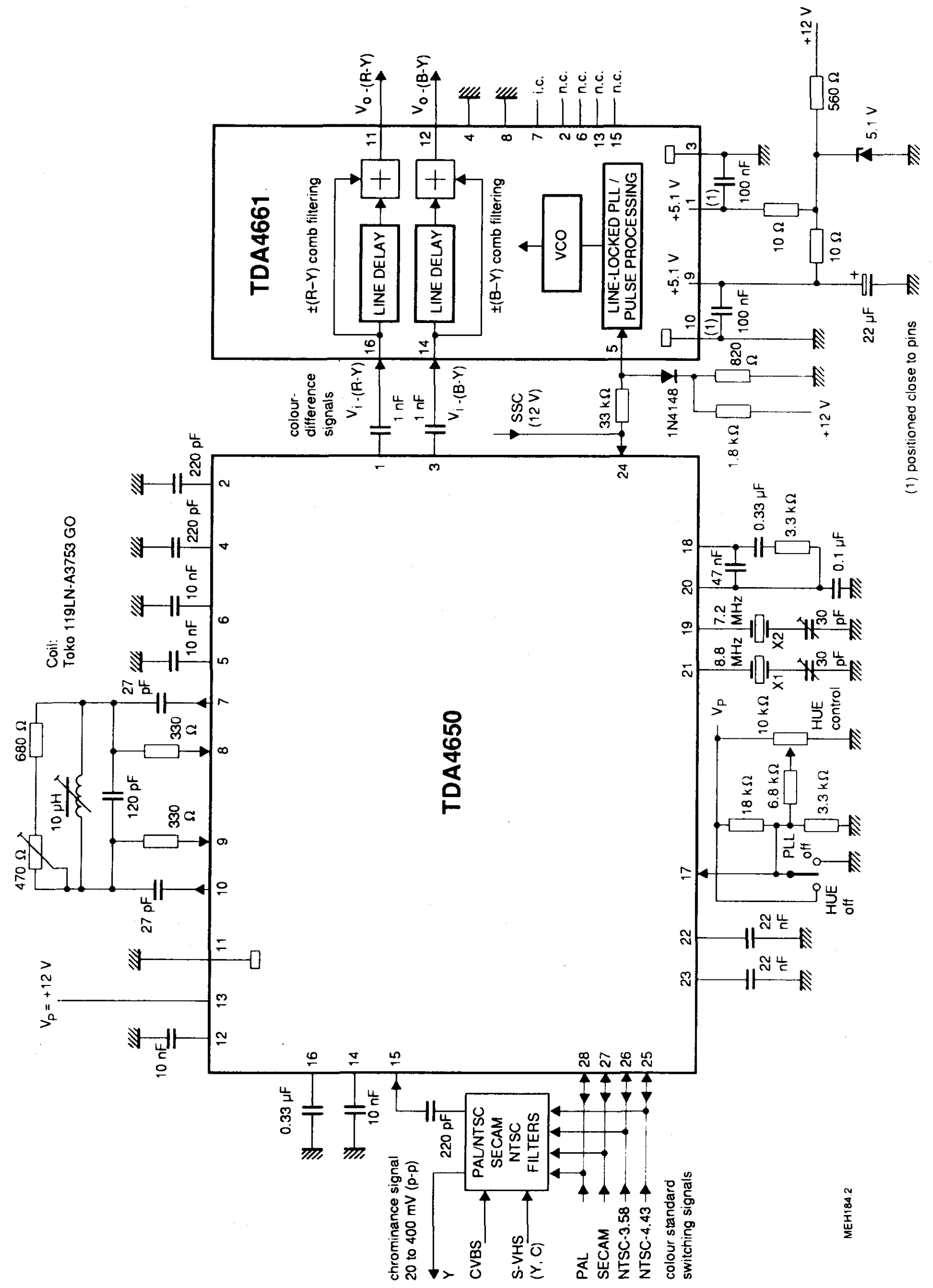


Fig.3 Application circuit with TDA4650.

Picture signal improvement (PSI) circuit

TDA4670

Supersedes data of August 1990

FEATURES

- Luminance signal delay from 20 ns up to 1100 ns (minimum step 45 ns)
- Luminance signal peaking with symmetrical overshoots selectable
- 2.6 or 5 MHz peaking centre frequency and degree of peaking selectable (–3, 0, +3 and +6 dB)
- Noise reduction by coring selectable
- Handles negative as well as positive colour-difference signals
- Colour transient improvement (CTI) selectable to decrease the colour-difference signal transient times to those of the high frequency luminance signals
- 5 or 12 V sandcastle input voltage selectable
- All controls selected via the I^2C-bus
- Timing pulse generation for clamping and delay time control synchronized by sandcastle pulse
- Automatic luminance signal delay correction using a control loop
- Luminance and colour-difference input signal clamping with coupling-capacitor
- +4.5 to 8.8 V supply voltage range
- Minimum of external components

GENERAL DESCRIPTION

The TDA4670 delays the luminance signal and improves colour-difference signal transients. Additional, the luminance signal can be improved by peaking and noise reduction (coring).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 1 and 5)	4.5	5	8.8	V
I_P	total supply current	31	41	52	mA
$t_{d\,Y}$	Y signal delay time	20	-	1130	ns
$V_{i\,VBS}$	composite Y input signal (peak-to-peak value, pin 16)	-	450	640	mV
$V_{i\,CD}$	colour-difference input signal (peak-to-peak value)				
	±(R–Y) on pin 3	-	1.05	1.48	V
	±(B–Y) on pin 7	-	1.33	1.88	V
G_Y	gain of Y channel	-	–1	-	dB
G_{CD}	gain of colour-difference channel	-	0	-	dB
T_{amb}	operating ambient temperature range	0	-	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4670	18	DIL	plastic	SOT102

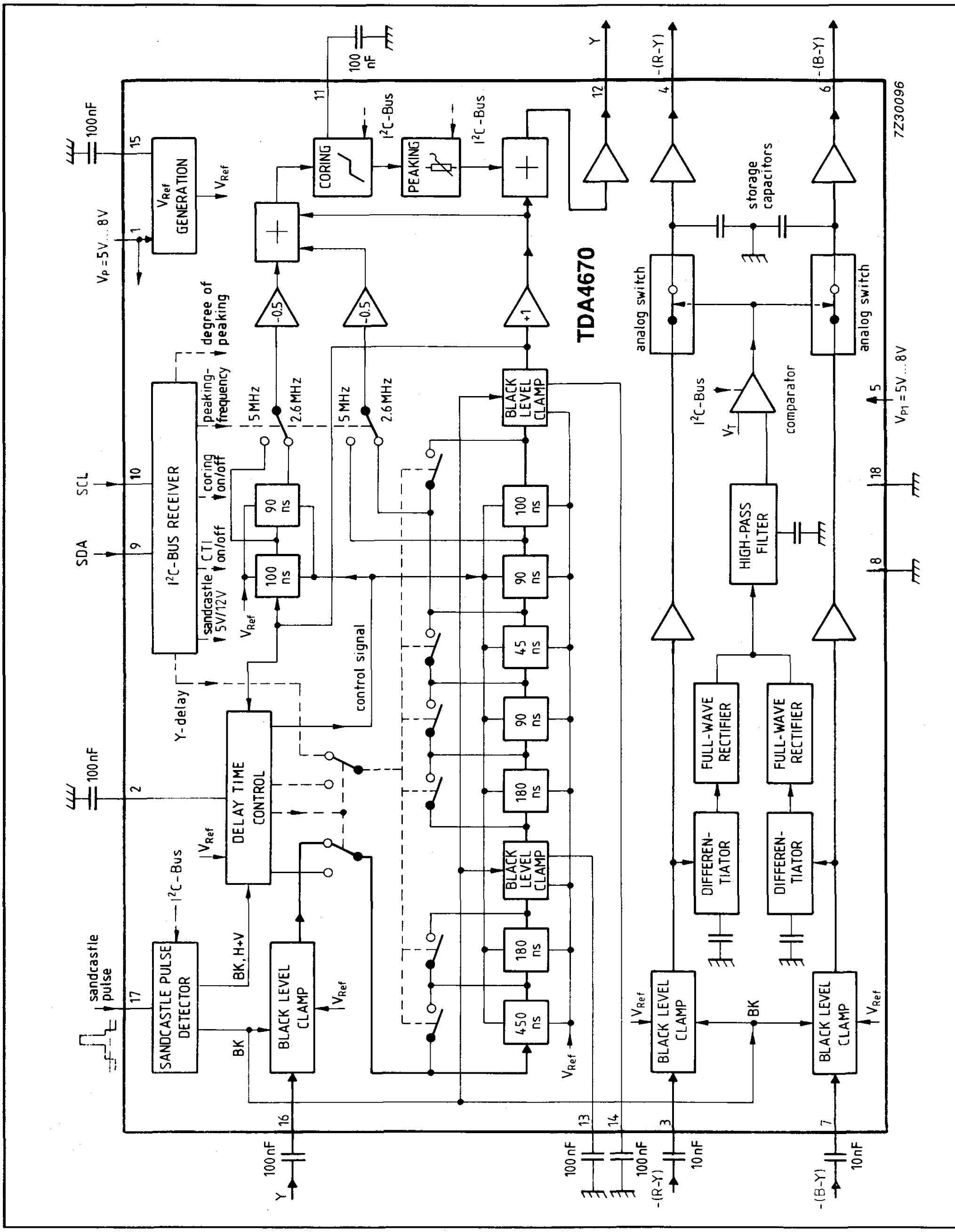


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P1}	1	positive supply voltage 1
C_{DL}	2	capacitor of delay time control
$V_{i\,(R-Y)}$	3	±(R–Y) colour-difference input signal
$V_{o\,(R-Y)}$	4	±(R–Y) colour-difference output signal
V_{P2}	5	positive supply voltage 2
$V_{o\,(B-Y)}$	6	±(B–Y) colour-difference output signal
$V_{i\,(B-Y)}$	7	±(B–Y) colour-difference input signal
GND2	8	ground 2 (0 V)
SDA	9	I^2C-bus data line
SCL	10	I^2C-bus clock line
C_{COR}	11	coring capacitor
$V_{o\,Y}$	12	delayed luminance output signal
C_{CLP1}	13	black level clamping capacitor 1
C_{CLP2}	14	black level clamping capacitor 2
C_{ref}	15	capacitor of reference voltage
$V_{i\,Y}$	16	luminance input signal
SAND	17	sandcastle pulse input
GND1	18	ground 1 (0 V)

PIN CONFIGURATION

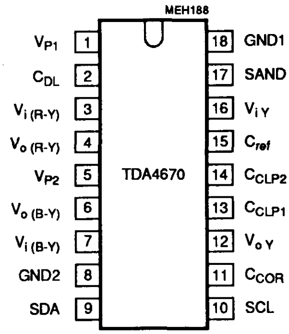


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA4670 contains luminance signal processing and colour-difference signal processing.The luminance signal section comprises a variable, integrated luminance delay line with luminance signal peaking and a noise reduction by coring.
The colour-difference section consists of a transient improvement circuit to decreases the rise and fall times of the colour-difference signal transients. All functions and parameters are controlled via the I^2C-bus.

Y-signal path

The video and blanking signal is AC-coupled to the input pin 16. Its black porch is clamped to a DC reference voltage to ensure fitting to the operating range of the luminance delay stage.
The luminance delay line consists of all-pass filter sections with delay times of 45, 90, 100, 180 and 450 ns (Fig.1). The luminance signal delay is controlled via the I^2C-bus in steps of 45 ns in the range of 20 to 1100 ns, this ensures that the maximum delay difference between the luminance and colour-difference signals is ±22.5 ns.
An automatic luminance delay time *adjustment* in an internal control loop (with the horizontal frequency as a reference) is used to correct changes in the delay time, due to component tolerances. The control loop is automatically enabled between the burst-key pulses of lines 16 (330) and 17 (331) during the vertical blanking interval. The control voltage is stored in the capacitor C_{DL} at pin 2.
The peaking section is using a transversal filter circuit with selectable centre frequencies of 2.6 and 5.0 MHz.
It provides selectable degrees of peaking of –3, 0, +3 and +6 dB and a noise reduction by coring, which attenuates the high-frequency noise introduced by peaking.
The output buffer stage ensures a low-ohmic VBS output signal on pin 12 (< 160 Ω). The gain of the luminance signal path from pin 16 to pin 12 is unity.

An oscillation signal of the delay time control loop is present on output pin 12 instead of the VBS signal during the vertical blanking interval in lines 16 (330) to 18 (332). Therefore, this output signal should not be applied for synchronization.

Colour-difference signal paths

The colour-difference input signals (on pins 3 and 7) are clamped to a reference voltage.

Each colour-difference signal is fed to a transient detector and to an analog signal switch with an attached voltage storage stage.
The transient detectors consist of differentiators and full-wave rectifiers. The output voltages of both transient detectors are added and then compared in a comparator. This comparator controls both following analog signal switches simultaneously. The analog signal switches are in open position at a certain value of transient time; then the held value (held by storage capacitors) is applied to the outputs. The switches close to accept rapidly the actual signal levels at the end of these transients. The improved transient time is approximately 100 ns long independent of the input signal transient time.

Colour-difference paths are independent of the input signal polarity and have a gain of unity .

The CTI functions are switched on and off via the I^2C-bus.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134). V_{P1} and V_{P2} as well as GND1 and GND 2 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 1)	0	8.8	V
V_{P2}	supply voltage (pin 5)	0	8.8	V
P_{tot}	total power dissipation	0	0.97	W
T_{stg}	storage temperature range	–25	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for pins 9 and 10	- -	+300 –500	V V
	for other pins	-	±500	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\,j\text{-}a}$	from junction-to-ambient in free air	-	82	K/W

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

$V_{P1} = V_{P2} = 5$ V; nominal video amplitude $V_{VB} = 315$ mV; $t_H = 64$ µs; $t_{BK} = 4$ µs (burst key); $T_{amb} = 25$ °C and measurements taken in Fig.3 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}	supply voltage range (pin 1)		4.5	5	8.8	V
V_{P2}	supply voltage range (pin 5)		4.5	5	8.8	V
I_P	total supply current		31	41	52	mA
Y-signal path						
$V_{i\,Y}$	VBS input signal on pin 16 (peak-to-peak value)		-	450	640	mV
V_{16}	black level clamping voltage		-	3.1	-	V
I_{16}	input current	during clamping	±95	-	±190	µA
		outside clamping	-	-	±0.1	µA
R_{16}	input resistance	outside clamping	5	-	-	MΩ
C_{16}	input capacitance		-	3	10	pF
$t_{d\,Y}$	maximum Y delay time	set via I²C-bus	1070	1100	1130	ns
	minimum Y delay time		-	20	-	ns
$\Delta t_{d\,Y}$	minimum delay step	set via I²C-bus	40	45	50	ns
	group delay time difference	f = 0.5 to 5 MHz maximum delay	-	0	±25	ns
	delay time difference between Y and colour-difference signals	Y delay; CTI and peaking off	70	100	130	ns
$t_{d\,peak}$	minimum delay time for peaking		185	215	245	ns
G_Y	VBS signal gain measured on output pin 12 (composite signal, peak-to-peak value)	V_o/V_i; f = 500 kHz; maximum delay	−2	−1	0	dB
I_{12}	output current (emitter-follower with constant current source)	source current	−1	-	-	mA
		sink current	0.4	-	-	mA
R_{12}	output resistance		-	-	160	Ω
f	frequency response for	maximum delay				
	f = 0.5 to 3 MHz		−2	−1	0	dB
	f = 0.5 to 5 MHz		−4	−3	−1	dB
LIN	signal linearity for	a_{min}/a_{max}				
	video contents of 315 mV (p-p)	V_{VBS} = 450 mV (p-p)	0.85	-	-	-
	video contents of 450 mV (p-p)	V_{VBS} = 640 mV (p-p)	0.60	-	-	-

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Luminance peaking, selected via I^2C-bus						
f_{peak}	peaking frequency	f_{C1}; LCF-bit = 0	4.5	5	5.5	MHz
		f_{C2}; LCF-bit = 1	2.3	2.6	2.9	MHz
V_{peak}	peaking amplitude for grade of peaking (f_C amplitude over 0.5 MHz amplitude)					
	selectable values		-	−3	-	dB
			-	0	-	dB
			-	+3	-	dB
			-	+6	-	dB
	limitation of peaking (positive amplitude of correction signal referred to 315 mV)		-	20	-	%
V_n	noise voltage on pin 12 (RMS value)	without peaking f = 0 to 5 MHz	-	-	1	mV
COR	coring of peaking (coring part referred to 315 mV)	COR-bit = 1	-	20	-	%
Colour-difference paths measured with transient times $t_r = t_f = 1$ µs; $t_{p\,H} \geq 1$ µs; $V_i = 1.33$ V (p-p) on pins 3 and 7 and with burst key pulse $t_{BK} = 4$ µs.						
$V_{i\,CD}$	±(R–Y) input signal (peak-to-peak values, pin 3)	75% colour bar;	-	1.05	1.48	V
	±(B–Y) input signal (peak-to-peak values, pin 7)	75% colour bar	-	1.33	1.88	V
	input transient sensitivity	$V_{3,7}$ /dt	0.15	-	-	V/µs
$V_{3,7}$	internal clamping voltage level		-	2.45	-	V
$I_{3,7}$	input current	outside clamping	-	-	±1	µA
		during clamping	±100	-	±190	µA
$C_{3,7}$	input capacitance		-	6	12	pF
$V_{4,6}$	DC output voltage		-	2	-	V
$\Delta V_{4,6}$	output offset voltage	$R_S \leq 300\ \Omega$; note 1	-	-	±5	mV
		during and after storage time	-	-	±18	mV
V_{spike}	spurious spike signals on pins 4 and 6	$R_S \leq 300\ \Omega$; note 1	-	-	±30	mV
$I_{4,6}$	output current (emitter-follower with constant current source)	source current	−1	-	-	mA
		sink current	0.4	-	-	mA
$R_{4,6}$	output resistance		-	-	100	Ω
G_v	signal gain in each path	V_o / V_i	−1	0	+1	dB
ΔG_v	gain difference −(R–Y) / −(B–Y)		-	0	±0.3	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LIN	signal linearity	a_{min} / a_{max}				
	for nominal signal	V_i = 1.33 V (p-p)	0.90	-	-	
	for +3 dB signal	V_i = 1.88 V (p-p)	0.65	-	-	
ΔV_o	signal reduction at higher frequency (output signal ratio V_i / V_o)	signal with $t_{p\,H}$ = 50 ns; $t_r = t_f$ = 1 µs	−1.5	-	-	dB
Sandcastle pulse, input voltage selectable via I²C-bus						
V_{17}	input voltage threshold for H and V sync	SC5-bit = 0 (12 V)	1.1	1.5	1.9	V
	input voltage threshold for burst	SC5-bit = 0 (12 V)	5.5	6.5	7.5	V
	input voltage threshold for H and V sync	SC5-bit = 1 (5 V)	1.1	1.5	1.9	V
	input voltage threshold for burst	SC5-bit = 1 (5 V)	3.0	3.5	4.0	V
R_{17}	input resistance	12 V input level	30	40	50	kΩ
		5 V input level	15	20	25	kΩ
C_{17}	input capacitance		-	4	8	pF
t_{BK}	burst-key pulse width		3.0	4.0	4.6	µs
t_d	leading edge delay for clamping pulse	referred to t_{BK}	-	1	-	µs
n_p	number of required burst-key pulses vertical blanking interval	note 2	4	-	31	
I²C-bus control, SDA and SCL						
V_{IH}	input voltage HIGH on pins 9 and 10		3	-	5	V
V_{IL}	input voltage LOW		0	-	1.5	V
$I_{9,10}$	input current		-	-	±10	µA
V_9	output voltage at acknowledge on pin 9	I_9 = 3 mA	-	-	0.4	V
I_{ACK}	output current at acknowledge on pin 9	sink current	3	-	-	mA

Notes to the characteristics

1. Crosstalk on output, measured in the unused channel when the other channel is provided with a nominal input signal (CTI active).
2. A number of more than 31 burst-key pulses repeats the counter cycle of delay time control.

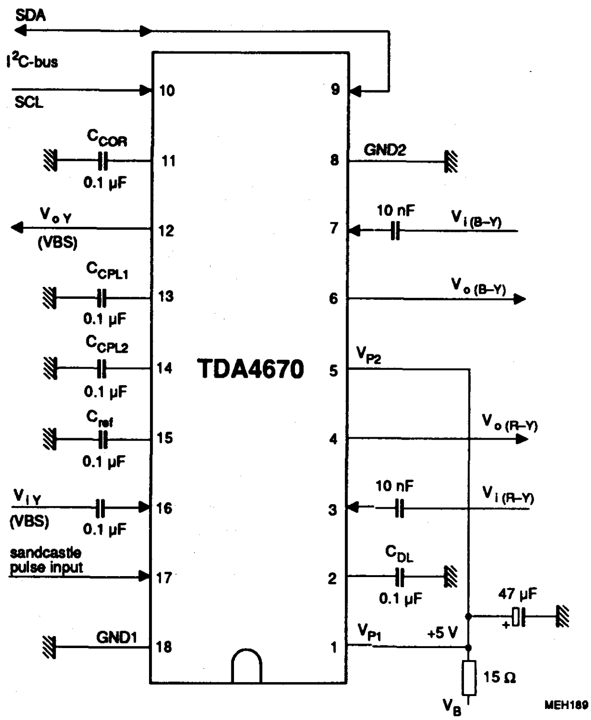


Fig.3 Test and application circuit.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S	=	start condition
SLAVE ADDRESS	=	**1000 100X**
A	=	acknowledge, generated by the slave
SUBADDRESS	=	subadress byte, Table 1
DATA	=	data byte, Table 1
P	=	stop condition
X	=	read/write control bit X = 0, to write (the circuit is slave receiver only)

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 1 I^2C-bus transmission

function	subaddress byte	D7	D6	D5	D4	D3	D2	D1	D0
		data byte							
Y delay / CTI / SC	0 0 0 1 0 0 0 0	0	SC5	CTI	DL4	DL3	DL2	DL1	DL0
peaking and coring	0 0 0 1 0 0 0 1	COR	PEAK	LCF	0	0	0	PCON1	PCON0

Function of the bits:

DL0	set delay in luminance channel:	1 = 45 ns;	0 = 0 ns
DL1		1 = 90 ns;	0 = 0 ns
DL2		1 = 180 ns;	0 = 0 ns
DL3		1 = 180 ns;	0 = 0 ns
DL4		1 = 450 ns;	0 = 0 ns
CTI	set colour transient improvement:	1 = active	0 = inactive
SC5	select sandcastle pulse voltage:	1 = 5 V	0 = 12 V
LCF	set peaking frequency response:	1 = 2.6 MHz	0 = 5.0 MHz
PEAK	set peaking delay:	1 = active	0 = inactive
COR	set coring control:	1 = active	0 = inactive
PCON	set peaking amplification:		

PCON1	PCON0	grade of peaking
0	0	−3 dB
0	1	0 dB
1	0	+3 dB
1	1	+6 dB

Remarks to the subaddress bytes

Hex subaddresses 00 to 0F are reserved for colour decoders and RGB processors.
Subaddresses 10 and 11 only are acknowledged .
General call address is not acknowledged.
Power-on reset: D7 to D1 bits of data bytes are set to 0 , D0 bit is set to 1.

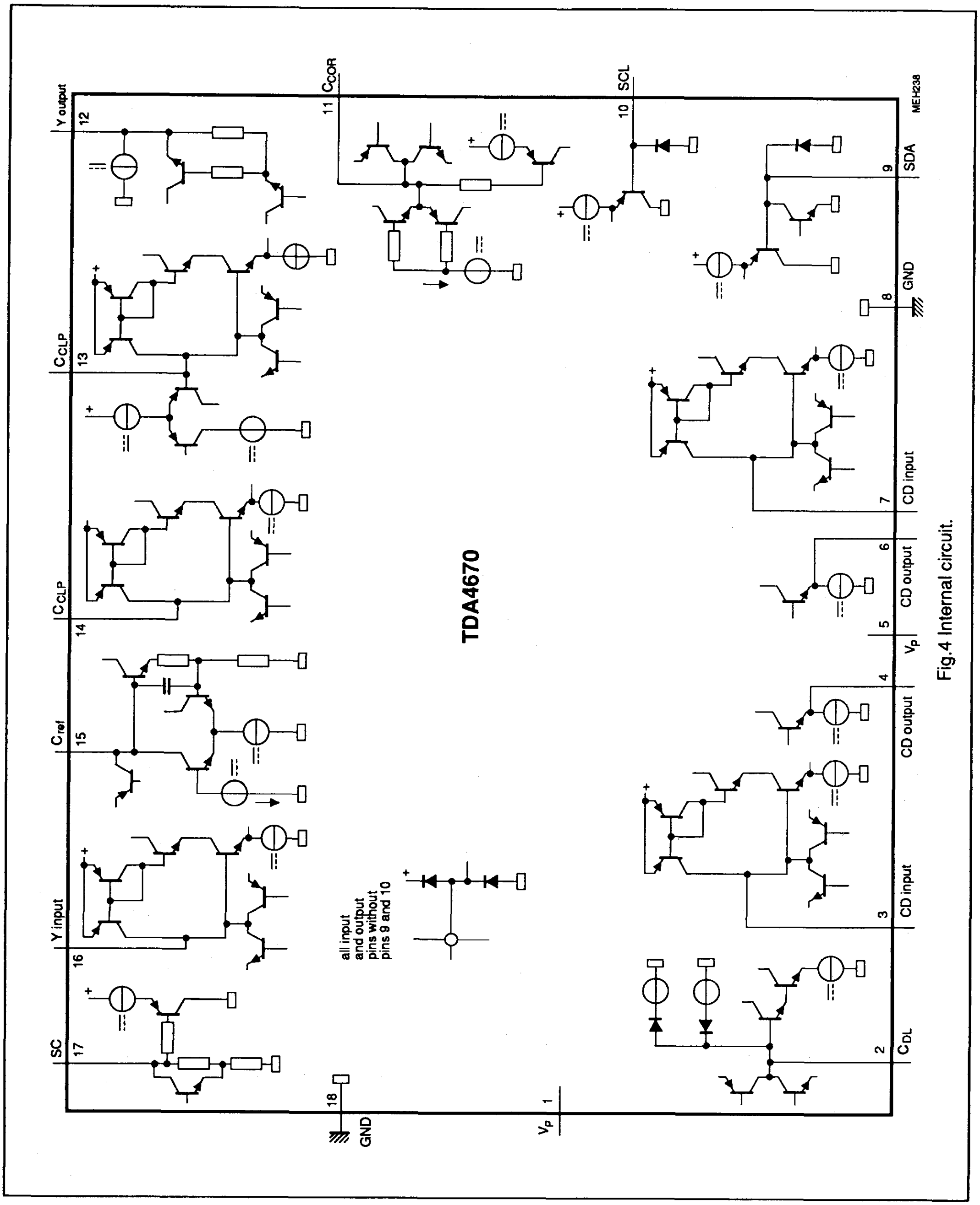


Fig.4 Internal circuit.

Video processor with automatic cut-off and white level control

TDA4680

FEATURES

- Operates from an 8 V DC supply
- Black level clamping of the colour difference, luminance and RGB input signals with coupling-capacitor DC level storage
- Two fully-controlled, analog RGB inputs, selected either by fast switch signals or via I^{2}C-bus
- Saturation, contrast and brightness adjustment via I^{2}C-bus
- Same RGB output black levels for Y/CD and RGB input signals
- Timing pulse generation from either a 2- or 3-level sandcastle pulse for clamping, horizontal and vertical synchronization, cut-off and white level timing pulses
- Automatic cut-off control with picture tube leakage current compensation
- Software-based automatic white level control or fixed white levels via I^{2}C-bus
- Cut-off and white level measurement pulses in the last 4 lines of the vertical blanking interval (I^{2}C-bus selection for PAL, SECAM, or NTSC, PAL-M)
- Increased RGB signal bandwidths for progressive scan and 100 Hz operation (selected via I^{2}C-bus)
- Two switch-on delays to prevent discolouration before steady-state operation
- Average beam current and peak drive limiting
- PAL/SECAM or NTSC matrix selection via I^{2}C-bus
- Three adjustable reference voltage levels (via I^{2}C-bus) for automatic cut-off and white level control
- Emitter-follower RGB output stages to drive the video output stages
- Hue control output for the TDA4555, TDA4650/T, TDA4655/T or TDA4657.

There is a very similar IC TDA4681 available. The only differences are in the NTSC matrix.

GENERAL DESCRIPTION

The TDA4680 is a monolithic integrated circuit with a colour difference interface for video processing in TV receivers. Its primary function is to process the luminance and colour difference signals from multistandard colour decoders, TDA4555, TDA4650/T, TDA4655/T or TDA4657, Colour Transient Improvement (CTI) IC, TDA4565, Picture Signal Improvement (PSI) IC, TDA4670, or from a Feature Module.

The required input signals are:

- luminance and negative colour difference signals
- 2- or 3-level sandcastle pulse for internal timing pulse generation
- I^{2}C-bus data and clock signals for microprocessor control.

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector and the other from an on-screen display generator; both inputs are fully-controlled internally. The TDA4680 includes full I^{2}C-bus control of all parameters and functions with automatic cut-off and white level control of the picture tube cathode currents. It provides RGB output signals for the video output stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)	7.2	8.0	8.8	V
I_P	supply current (pin 5)	–	85	–	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value)	–	0.45	–	V
$V_{6(p-p)}$	–(B–Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	–(R–Y) input (peak-to-peak value)	–	1.05	–	V
V_{14}	three-level sandcastle pulse				
	H+V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	two-level sandcastle pulse				
	H+V	–	2.5	–	V
	BK	–	4.5	–	V
V_i	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (black-to-white value)	–	0.7	–	V
$V_{o(p-p)}$	RGB outputs at pins 24, 22 and 20 (peak-to-peak value)	–	2.0	–	V
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4680	28	DIL	plastic	SOT117
TDA4680WP	28	PLCC	plastic	SOT261CG

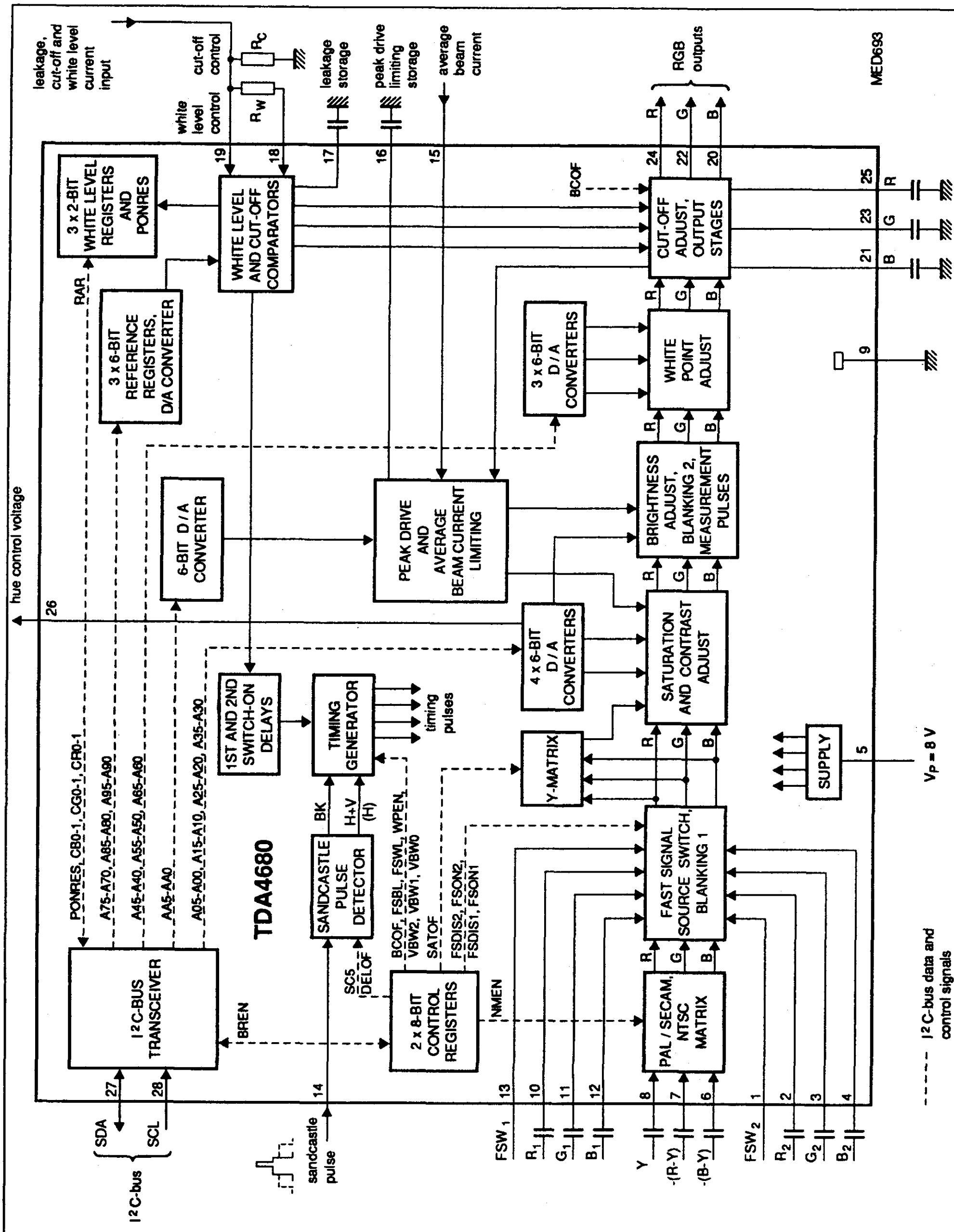


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
–(B–Y)	6	colour difference input –(B–Y)
–(R–Y)	7	colour difference input –(R–Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input

SYMBOL	PIN	DESCRIPTION
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak drive limiting
C_L	17	storage capacitor for leakage current
WI	18	white level measurement input
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
HUE	26	hue control output
SDA	27	I^2C-bus serial data input/output
SCL	28	I^2C-bus serial clock input

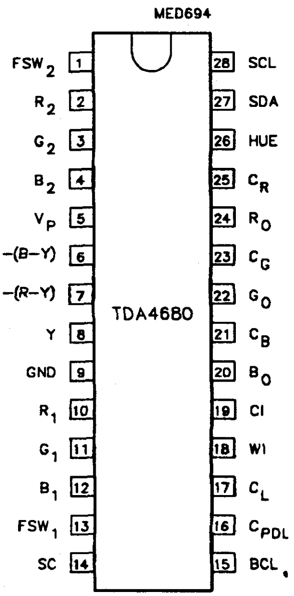


Fig.2 Pin configuration for DIL package.

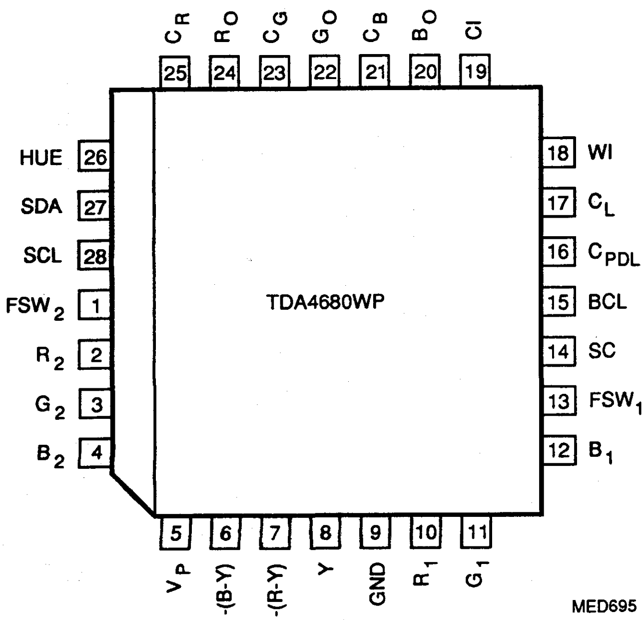


Fig.3 Pin configuration for PLCC package.

I²C-BUS CONTROL

The I²C-bus transmitter/receiver provides the data bytes to select and adjust the following functions and parameters:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- RGB reference voltage levels
- peak drive limiting
- selection of the vertical blanking interval and measurement lines for cut-off and white level control according to transmission standard
- selects either 3-level or 2-level (5 V) sandcastle pulse
- enables/disables input clamping pulse delay
- enables/disables white level control
- enables cut-off control / enables output clamping
- enables/disables full screen white level
- enables/disables full screen black level
- selects either PAL/SECAM or NTSC matrix
- enables saturation adjust / enables nominal saturation
- enables/disables synchronization of the execution of I²C-bus commands with the vertical blanking interval
- reads the result of the comparison of the nominal and actual RGB signal levels for automatic white level control.

I²C-BUS TRANSMITTER / RECEIVER AND DATA TRANSFER

I²C-bus specification

The I²C-bus is a bi-directional, two-wire, serial data bus for intercommunication between ICs in an equipment. The microcontroller transmits/receives data from the I²C-bus transceiver in the TDA4680 over the serial data line SDA (pin 27) synchronized by the serial clock line SCL (pin 28). Both lines are normally connected to a positive voltage supply through pull-up resistors. Data is transferred when the SCL line is LOW. When SCL is HIGH the serial data line SDA must be stable. A HIGH-to-LOW transition of the SDA line when SCL is HIGH is defined as a start bit. A LOW-to-HIGH transition of the SDA line when SCL is HIGH is defined as a stop bit. Each transmission must start with a start bit and end with a stop bit. The bus is busy after a start bit and is only free again after a stop bit has been transmitted.

I²C-bus receiver

(microcontroller write mode)

Each transmission to/from the I²C-bus transceiver consists of at least three bytes following the start bit. Each byte is acknowledged by an acknowledge bit immediately following each byte. The first byte is the Module ADdress (MAD) byte, also called slave address byte. This consists of the module address, 1000100_2 for the TDA4680, plus the R/W̄ bit (see Fig.4). When the TDA4680 is a slave receiver (R/W̄ = 0) the module address byte is 10001000_2 (88 Hex). When the TDA4680 is a slave transmitter (R/W̄ = 1) the module address byte is 10001001_2 (89 Hex). The length of a data transmission is unrestricted, but the module address and the correct sub-address must be transmitted before the data byte(s). The order of data transmission is shown in Fig.5 and Fig.6. Without auto-increment (BREN = 0 or 1) the module address (MAD) byte is followed by a Sub-ADdress (SAD) byte and one data byte only (Fig.5).

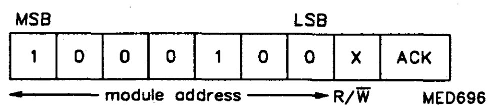


Fig.4 The module address byte.

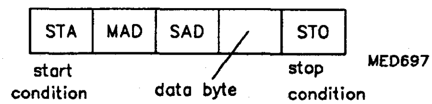


Fig.5 Data transmission without auto-increment (BREN = 0 or 1).

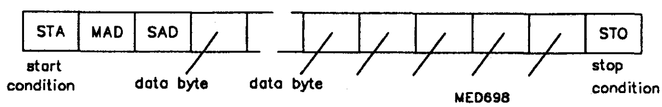


Fig.6 Data transmission with auto-increment (BREN = 0).

Auto-increment

The auto-increment format enables quick slave receiver initialization by one transmission, when the I^2C-bus control bit BREN = 0 (see control register bits of Table 1). If BREN = 1 auto-increment is not possible.
If the auto-increment format is selected, the MAD byte is followed by an SAD byte and by the data bytes of consecutive sub-addresses (Fig.6).
All sub-addresses from 00 to 0F are automatically incremented, the sub-address counter wraps round from 0F to 00. Reserved sub-addresses 0B, 0E and 0F are treated as legal but have no effect. Sub-addresses outside the range 00 and 0F are not acknowledged by the device and neither auto-increment nor any other internal operation takes place (For versions V1 to V5 sub-addresses outside the range 00 and 0F are acknowledged but neither auto-increment nor any other internal operation takes place).
Sub-addresses are stored in the TDA4680 to address the following parameters and functions, see Table 1:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- RGB reference voltage levels
- peak drive limiting adjust
- control register functions.

The data bytes (D7-D0 of Table 1) provide the data of the parameters and functions for video processing.

Control register 1

VBWx (Vertical Blanking Window):
x = 0, 1 or 2. VBWx selects the vertical blanking interval and positions the measurement lines for cut-off and white level control.
The actual lines in the vertical blanking interval after the start of the V pulses selected as measurement lines for cut-off and white level control are shown in Table 2.
The standards marked with (*) are for progressive line scan at double line frequency ($2F_L$), i.e. approximately 31 kHz.
NMEN (NTSC - Matrix ENable):
0 = PAL/SECAM matrix
1 = NTSC matrix.
WPEN (White Pulse ENable):
0 = white measuring pulse disabled
1 = white measuring pulse enabled.
BREN (Buffer Register ENable):
0 = new data is executed as soon as it is received
1 = data is stored in buffer registers and is transferred to the data registers during the next vertical blanking interval.
The I^2C-bus transceiver does not accept any new data until this data is transferred into the data registers.
DELOF (DELay OFf) delays the leading edge of clamping pulses:
0 = delay enabled
1 = delay disabled.
SC5 (SandCastle 5 V):
0 = 3-level sandcastle pulse
1 = 2-level (5 V) sandcastle pulse.

Control register 2

FSON2 - Fast Switch 2 ON
FSDIS2 - Fast Switch 2 DISable
FSON1 - Fast Switch 1 ON
FSDIS1 - Fast Switch 1 DISable
The RGB input signals are selected by FSON2 and FSON1 or FSW_2 and FSW_1:

- FSON2 has priority over FSON1;
- FSW_2 has priority over FSW_1;
- FSDIS1 and FSDIS2 disable FSW_1 and FSW_2 (see Table 3).

BCOF - Black level Control OFf:
0 = automatic cut-off control enabled
1 = automatic cut-off control disabled; RGB outputs are clamped to fixed DC levels.
FSBL - Full Screen Black Level:
0 = normal mode
1 = full screen black level (cut-off measurement level during full field).
FSWL - Full Screen White Level:
0 = normal mode
1 = full screen white level (white measurement level during full field).
SATOF - SATuration control OFf:
0 = saturation control enabled
1 = saturation control disabled, nominal saturation enabled.

I^2C-bus transmitter

(microcontroller read mode)
As an I^2C-bus transmitter, $R/\overline{W}$ = 1, the TDA4680 sends a data byte from the status register to the microcontroller. The data byte consists of following bits:
PONRES, CB1, CB0, CG1, CG0, CR1, CR0 and 0, where PONRES is the most significant bit.
PONRES (Power ON RESet) monitors the state of TDA4680's supply voltage:
0 = normal operation
1 = supply voltage has dropped below approximately 6.0 V (usually occurs when the TV receiver is switched on or the supply voltage was interrupted).
When PONRES changes state from a logic LOW to a logic HIGH all data and function bits are set to logic LOW.

2-bit white level error signal

(see Table 4).
CB1, CB0 = 2-bit white level of the blue channel.
CG1, CG0 = 2-bit white level of the green channel.
CR1, CR0 = 2-bit white level of the red channel.

Table 1 Sub-address (SAD) and data bytes.

FUNCTION	SAD (HEX)	MSB 7	6	5	DATA BYTE 4	3	2	1	LSB 0
Brightness	00	0	0	A05	A04	A03	A02	A01	A00
Saturation	01	0	0	A15	A14	A13	A12	A11	A10
Contrast	02	0	0	A25	A24	A23	A22	A21	A20
Hue control voltage	03	0	0	A35	A34	A33	A32	A31	A30
Red gain	04	0	0	A45	A44	A43	A42	A41	A40
Green gain	05	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06	0	0	A65	A64	A63	A62	A61	A60
Red level reference	07	0	0	A75	A74	A73	A72	A71	A70
Green level reference	08	0	0	A85	A84	A83	A82	A81	A80
Blue level reference	09	0	0	A95	A94	A93	A92	A91	A90
Peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Reserved	0B	x	x	x	x	x	x	x	x
Control register 1	0C	SC5	DELOF	BREN	WPEN	NMEN	VBW2	VBW1	VBW0
Control register 2	0D	SATOF	FSWL	FSBL	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Reserved	0E	x	x	x	x	x	x	x	x
Reserved	0F	x	x	x	x	x	x	x	x

Table 2 Cut-off and white level measurement lines.

VBW2	VBW1	VBW0	R	G	B	WHITE	STANDARD
0	0	0	19	20	21	22	PAL/SECAM
0	0	1	16	17	18	19	NTSC/PAL M
0	1	0	22	23	24	25	PAL/SECAM (EB)
1	0	0	38, 39	40, 41	42, 43	44, 45	PAL*/SECAM*
1	0	1	32, 33	34, 35	36, 37	38, 39	NTSC*/PAL M*
1	1	0	44, 45	46, 47	48, 49	50, 51	PAL*/SECAM* (EB)

Notes to Table 2

1. The line numbers given are those of the horizontal pulse counts after the start of the vertical component of the sandcastle pulse.
2. * line frequency of approximately 31 kHz.
3. (EB) is extended blanking.

Table 3 Signal input selection by the fast source switches.

I^2C-BUS CONTROL BITS				ANALOG SWITCH SIGNALS		INPUT SELECTED		
FSON2	FSDIS2	FSON1	FSDIS1	FSW_2 (pin 1)	FSW_1 (pin 13)	RGB_2	RGB_1	Y/CD
L	L	L	L	L	L			ON
				L	H		ON	
				H	X	ON		
L	L	L	H	L	X			ON
				H	X	ON		
L	L	H	X	L	X		ON	
				H	X	ON		
L	H	L	L	X	L			ON
				X	H		ON	
L	H	L	H	X	X			ON
L	H	H	X	X	X		ON	
H	X	X	X	X	X	ON		

Note to Table 3

Where L is a logic LOW (< 0.4 V), H is a logic HIGH (> 0.9 V), X is 'don't care', and ON is the selected input signal.

Table 4 2-bit white level error signals, CX1 and CX0.

CX1	CX0	INTERPRETATION
0	0	RAR (Reset-After-Read): no new measurements since last read
1	0	actual (measured) white level less than the tolerance range
1	1	actual (measured) white level within the tolerance range
0	1	actual (measured) white level greater than the tolerance range

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	–	8.8	V
V_I	input voltage (pins 1 to 8, 10 to 13, 16, 21, 23 and 25)	–0.1	V_P	V
	input voltage (pins 14, 15, 18 and 19)	–0.7	V_P + 0.7	V
	input voltage (pins 27 and 28)	–0.1	8.8	V
I_{AV}	average current (pins 20, 22 and 24)	4	–10	mA
I_M	peak current (pins 20, 22 and 24)	4	–20	mA
I_{18}	input current	0	2	mA
I_{26}	output current	0.5	–8	mA
T_{stg}	storage temperature	–20	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
P_{tot}	total power dissipation			
	SOT117	–	1.2	W
	SOT261CG	–	1.0	W

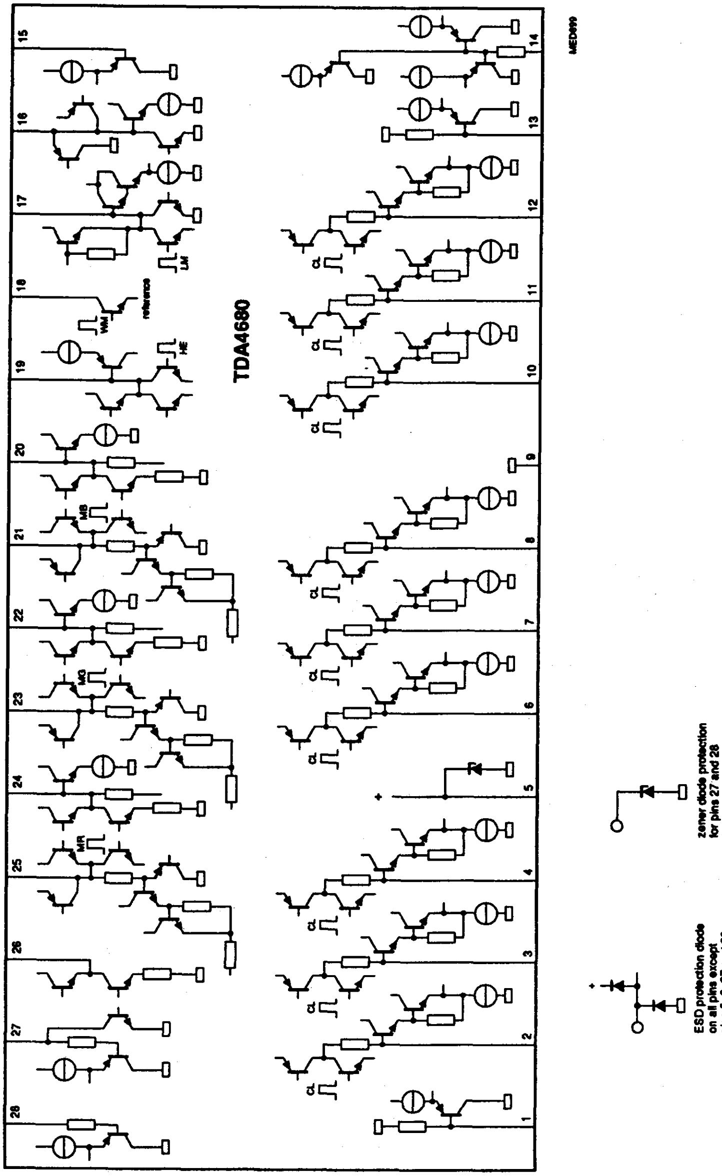


Fig.7 Internal circuits.

CHARACTERISTICS

All voltages are measured in test circuit of Fig.8 with respect to GND (pin 9); V_P = 8.0 V; T_{amb} = +25 °C:
- at nominal signal amplitudes (black-to-white) at output pins 24, 22 and 20,
- at nominal settings of brightness, contrast, saturation and white level control,
- without beam current or peak drive limiting; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)		7.2	8.0	8.8	V
I_P	supply current (pin 5)		–	85	110	mA
Colour difference inputs						
$V_{6(p-p)}$	–(B–Y) input (peak-to-peak value)	notes 1 and 2	–	1.33	–	V
$V_{7(p-p)}$	–(R–Y) input (peak-to-peak value)	notes 1 and 2	–	1.05	–	V
$V_{6,7}$	internal DC bias voltage	at black level clamping	–	3.1	–	V
$I_{6,7}$	input current	during line scan	–	–	±0.1	μA
		at black level clamping	±100	–	–	μA
$R_{6,7}$	input resistance		10	–	–	MΩ
Luminance/sync (VBS)						
$V_{i(p-p)}$	luminance input at pin 8 (peak-to-peak value)	note 2	–	0.45	–	V
V_8	internal DC bias voltage	at black level clamping	–	3.1	–	V
I_8	input current	during line scan	–	–	±0.1	μA
		at black level clamping	±100	–	–	μA
R_8	input resistance		10	–	–	MΩ
R_1, G_1 and B_1 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 10, 11 and 12 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{10/11/12}$	internal DC bias voltage	at black level clamping	–	5.3	–	V
$I_{10/11/12}$	input current	during line scan	–	–	±0.1	μA
		at black level clamping	±100	–	–	μA
$R_{10/11/12}$	input resistance		10	–	–	MΩ
R_2, G_2 and B_2 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 2, 3 and 4 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{2/3/4}$	internal DC bias voltage	at black level clamping	–	5.3	–	V
$I_{2/3/4}$	input current	during line scan	–	–	±0.1	μA
		at black level clamping	±100	–	–	μA
$R_{2/3/4}$	input resistance		10	–	–	MΩ
PAL/SECAM and NTSC matrix (notes 3 and 4)						
	PAL/SECAM matrix	control bit NMEN = 0				
	NTSC matrix	control bit NMEN = 1				
Fast signal switch FSW_1 to select Y, CD or R_1, G_1, B_1 inputs (control bits: see Table 3)						
V_{13}	voltage to select Y and CD		–	–	0.4	V
	voltage range to select R_1, G_1, B_1		0.9	–	5.0	V
R_{13}	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast signal switch FSW_2 to select Y, CD / R_1, G_1, B_1 or R_2, G_2, B_2 inputs (control bits: see Table 3)						
V_1	voltage to select Y, CD/R_1, G_1, B_1		–	–	0.4	V
	voltage range to select R_2, G_2, B_2		0.9	–	5.0	V
R_1	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns
Saturation adjust acts on internal RGB signals under I^2C-bus control, sub-address 01_{Hex} (bit resolution 1.5% of maximum saturation); data byte $3F_{Hex}$ for maximum saturation; data byte 23_{Hex} for nominal saturation; data byte 00_{Hex} for minimum saturation						
d_s	saturation below maximum	at 23_{Hex}	–	5	–	dB
		at 00_{Hex}; f = 100 kHz	–	50	–	dB
Contrast adjust acts on internal RGB signals under I^2C-bus control, sub-address 02_{Hex} (bit resolution 1.5% of maximum contrast); data byte $3F_{Hex}$ for maximum contrast; data byte $2C_{Hex}$ for nominal contrast; data byte 00_{Hex} for minimum contrast						
d_c	contrast below maximum	at $2C_{Hex}$	–	3	–	dB
		at 00_{Hex}	–	22	–	dB
Brightness adjust acts on internal RGB signals under I^2C-bus control, sub-address 00_{Hex} (bit resolution 1.5% of brightness range); data byte $3F_{Hex}$ for maximum brightness; data byte 27_{Hex} for nominal brightness; data byte 00_{Hex} for minimum brightness						
d_{br}	black level shift of nominal signal amplitude referred to cut-off measurement level	at $3F_{Hex}$	–	30	–	%
		at 00_{Hex}	–	–50	–	%
White potentiometers, under I^2C-bus control, sub-addresses 04_{Hex} (red), 05_{Hex} (green) and 06_{Hex} (blue); see note 5. data byte $3F_{Hex}$ for maximum gain; data byte 22_{Hex} for nominal gain; data byte 00_{Hex} for minimum gain						
ΔG_v	relative to nominal gain:					
	increase of gain	at $3F_{Hex}$	–	60	–	%
	decrease of gain	at 00_{Hex}	–	60	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB outputs pins 24, 22 and 20 (positive going output signals and no peak drive limitation; sub-address $0A_{Hex} = 3F_{Hex}$); see note 6.						
$V_{o(b-w)}$	nominal output signals (black-to-white value)		–	2	–	V
	maximum output signals (black-to-white value)		3.2	–	–	V
ΔV_o	spread between RGB output signals		–	–	10	%
V_o	minimum output voltages		–	–	0.8	V
	maximum output voltages		6.8	–	–	V
$V_{24,22,20}$	voltage of cut-off measurement line	output clamping (BCOF = 1)	2.3	2.5	2.7	V
I_{int}	internal current sources		–	5.0	–	mA
R_o	output resistance		–	65	110	Ω
Frequency response						
d	frequency response of Y path (from pin 8 to pins 24, 22, 20)	f = 10 MHz	–	–	3	dB
	frequency response of CD path (from pins 7 to 24 and 6 to 20)	f = 8 MHz	–	–	3	dB
	frequency response of RGB_1 path (from pins 10 to 24, 11 to 22 and 12 to 20)	f = 10 MHz	–	–	3	dB
	frequency response of RGB_2 path (from pins 2 to 24, 3 to 22 and 4 to 20)	f = 10 MHz	–	–	3	dB
Sandcastle pulse detector (control bit SC5 = 0) three level; notes 7 and 8						
V_{14}	required voltage range					
	for H and V blanking pulses		2.0	2.5	3.0	V
	for H pulses (line count)		4.0	4.5	5.0	V
	for burst key pulses		6.3	–	$V_P + 0.7$	V
Sandcastle pulse detector (control bit SC5 = 1) two level; note 7						
V_{14}	required voltage range					
	for H and V blanking pulses		2.0	2.5	3.0	V
	for burst key pulses		4.0	4.5	$V_P + 0.7$	V
Sandcastle pulse detector						
I_{14}	input current	$V_{14} = 0$ V	–	–	100	μA
t_d	leading edge delay of the clamping pulse	control bit DELOF = 0	–	1.5	–	μs
		control bit DELOF = 1	–	0	–	μs
t_{BK}	required burst key pulse time	control bit DELOF = 0; normally used with f_L	3	–	–	μs
		control bit DELOF = 1; normally used with $2f_L$	1.5	–	–	μs
n_{pulse}	required horizontal or burst key pulses during vertical blanking interval	e.g. at interlace scan (VBW2 = 0)	4	–	29	
		e.g. at progressive line scan (VBW2 = 1)	8	–	57	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Average beam current limiting (note 9)						
$V_{c(15)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(15)}$	voltage difference for full contrast reduction		–	−2.0	–	V
$V_{br(15)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(15)}$	voltage difference for full brightness reduction		–	−1.6	–	V
Peak drive limiting voltage (note 10) internal peak drive limiting level (V_{pdl}) acts on RGB outputs under I^2C-bus control, sub-address $0A_{Hex}$						
$V_{20/22/24}$	level for minimum RGB outputs	at byte 00_{Hex}	–	–	3.0	V
	level for maximum RGB outputs	at byte $3F_{Hex}$	6.5	–	–	V
I_{16}	charge current		–	−1	–	μA
	discharge current	during peak white	–	5	–	mA
V_{16}	internal voltage limitation		4.5	–	–	V
$V_{c(16)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(16)}$	voltage difference for full contrast reduction		–	−2.0	–	V
$V_{br(16)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(16)}$	voltage difference for full brightness reduction		–	−1.6	–	V
Automatic cut-off and white level control (notes 11, 12 and 13) *see Fig.10*						
V_{19}	permissible voltage (also during scanning period)		–	–	$V_P - 1.4$	V
I_{19}	output current		–	–	−140	μA
	input current		150	–	–	μA
	additional input current	during monitor pulse	–	0.5	–	mA
$V_{24,22,20}$	monitor pulse amplitude (under I^2C-bus *control*, sub-address $0A_{Hex}$)	switch-on delay 1	–	$V_{pdl} - 0.7$	–	V
V_{19}	voltage threshold for picture tube cathode warm-up	switch-on delay 1	–	5.0	–	V
	internally controlled voltage (V_{REF})	during leakage measurement period	–	3.0	–	V
data byte 07_{Hex} for red reference level data byte 08_{Hex} for green reference level data byte 09_{Hex} for blue reference level						
ΔV_{19}	difference between V_{MEAS} (cut-off or white level measurement voltage) and V_{REF}	$3F_{Hex}$ (maximum V_{MEAS})	1.5	–	–	V
		20_{Hex} (nominal V_{MEAS})	–	1.0	–	V
		00_{Hex} (minimum V_{MEAS})	–	–	0.5	V
I_{18}	input current	white level measurement	–	–	800	μA
R_{18}	internal resistance	to V_{REF}; $I_{18} \leq 800$ μA	–	100	–	Ω
ΔV_{19}	white level register (measured value within tolerance range)	white level measurement	–	250	–	mV

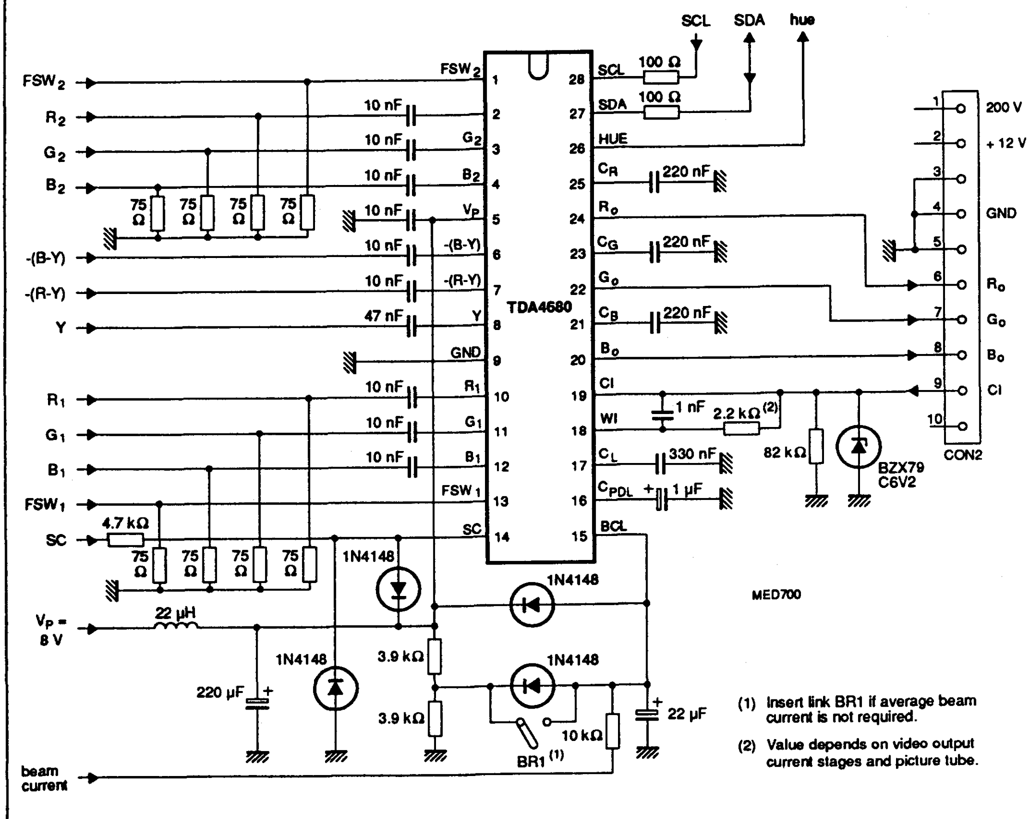
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Cut-off storage						
$I_{21/23/25}$	charge and discharge currents	during cut-off measurement lines	–	±0.3	–	mA
	current	outside measurement	–	–	±0.1	μA
Leakage storage						
I_{17}	charge and discharge currents	during leakage measurement period	–	±0.4	–	mA
	current	outside measurement	–	–	±0.1	μA
V_{17}	voltage for reset to switch-on below		–	< 3.0	–	V
Hue control (note 14) under I^2C-bus control, sub-address 03_{Hex} data byte $3F_{Hex}$ for maximum voltage data byte 20_{Hex} for nominal voltage data byte 00_{Hex} for minimum voltage						
V_{26}	output voltage	at byte $3F_{Hex}$	4.8	–	–	V
		at byte 20_{Hex}	–	3.0	–	V
		at byte 00_{Hex}	–	–	1.0	V
I_{int}	current of the internal current source at pin 26		500	–	–	μA
I^2C-bus transceiver clock SCL (pin 28)						
f_{SCL}	input frequency range		0	–	100	kHz
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	6	V
I_{IL}	LOW level input current		–	–	−10	μA
I_{IH}	HIGH level input current		–	–	10	μA
t_d	pulse delay time LOW		4.7	–	–	μs
	pulse delay time HIGH		4.0	–	–	μs
t_r	rise time		–	–	1.0	μs
t_f	fall time		–	–	0.3	μs
I^2C-bus transceiver data input/output SDA (pin 27)						
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	6	V
I_{IL}	LOW level input current		–	–	−10	μA
I_{IH}	HIGH level input current		–	–	10	μA
I_{OL}	LOW level output current		3.0	–	–	mA
t_r	rise time		–	–	1.0	μs
t_f	fall time		–	–	0.3	μs
$t_{SU;DAT}$	data set-up time		0.25	–	–	μs

Notes to the characteristics

1. The values of the −(B−Y) and −(R−Y) colour difference input signals are for a 75% colour-bar signal.
2. The pins are capacitively coupled to a low ohmic source, with a recommended maximum output impedance of 600 Ω.
3. PAL/SECAM signals are matrixed by the equation: $V_{G-Y} = -0.51V_{R-Y} - 0.19V_{B-Y}$
   NTSC signals are matrixed by the equations (hue phase shift of −5 degrees):
   $V_{R-Y}^* = 1.57V_{R-Y} - 0.41V_{B-Y}$; $V_{G-Y}^* = -0.43V_{R-Y} - 0.11V_{B-Y}$; $V_{B-Y}^* = V_{B-Y}$
   In the matrix equations: V_{R-Y} and V_{B-Y} are conventional PAL demodulation axes and amplitudes at the output of the NTSC demodulator. V_{G-Y}^*, V_{R-Y}^* and V_{B-Y}^* are the NTSC-modified colour difference signals; this is equivalent to the following demodulator axes and amplification factors:

	NTSC	PAL
(B−Y)* demodulator axis	0°	0°
(R−Y)* demodulator axis	115°	90°
(R−Y)* amplification factor	1.97	1.14
(B−Y)* amplification factor	2.03	2.03

   $V_{G-Y}^* = -0.27V_{R-Y}^* - 0.22V_{B-Y}^*$.
4. The vertical blanking interval is selected via the I^2C-bus (see Table 2 and Fig.10). Vertical blanking is determined by the vertical component of the sandcastle pulse; this vertical component has priority when it is longer than the vertical blanking interval of the transmission standard.
5. The white potentiometers affect the amplitudes of the RGB output signals including the white measurement pulses.
6. The RGB outputs at pins 24, 22 and 20 are emitter followers with current sources.
7. Sandcastle pulses are compared with internal threshold voltages independent of V_P. The threshold voltages separate the components of the sandcastle pulse. The particular component is generated when the voltage on pin 14 exceeds the defined internal threshold voltage. The internal threshold voltages (control bit SC5 = 0) are:
   1.5 V for horizontal and vertical blanking pulses (H and V blanking pulses),
   3.5 V for horizontal pulses,
   6.0 V for the burst key pulse.
   The internal threshold voltages, control bit SC5 = 1, are:
   1.5 V for horizontal and vertical blanking pulses,
   3.5 V for the burst key pulse.
8. A sandcastle pulse with a maximum voltage equal to (V_P + 0.7 V) is obtained by limiting a 12 V sandcastle pulse.
9. Average beam current limiting reduces the contrast, at minimum contrast it reduces the brightness.
10. Peak drive limiting reduces the RGB outputs by reducing the contrast, at minimum contrast it reduces the brightness. The maximum RGB outputs are determined via the I^2C-bus under sub-address $0A_{Hex}$. When an RGB output exceeds the maximum voltage, peak drive limiting is delayed by one horizontal line.
11. The vertical blanking interval is defined by a V pulse which contains 4 (8) or more H pulses; it begins with the start of the V pulse and ends with the end of the white measuring line. If the V pulse is longer than the selected vertical blanking window the blanking period ends with the end of the complete line after the end of the V pulse. The counter cycle time is 31 (63) H pulses. If the V pulse contains more than 29 (57) H pulses, the black level storage capacitors will be discharged while all signals are blanked. During leakage current measurement, the RGB channels are blanked to ultra-black level. During cut-off measurement one channel is set to the measurement pulse level, the other channels are blanked to ultra-black. Since the brightness adjust shifts the colour signal relative to the black level, the brightness adjust is disabled during the vertical blanking interval (see Figs 9 and 10).
12. During picture cathode warm-up (first switch-on delay) the RGB outputs (pins 24, 22 and 20) are blanked to the ultra-black level during line scan. During the vertical blanking interval a white-level monitor pulse is fed out on the RGB outputs and the cathode currents are measured. When the voltage threshold on pin 19 is greater than 5.0 V, the monitor pulse is switched off and cut-off and white level control are activated (second switch-on delay). As soon as cut-off control stabilize, RGB output blanking is removed.
13. Range of cut-off measurement level at the RGB outputs is 1 to 5 V. The recommended value is 3 V.
14. The hue control output at pin 26 is an emitter follower with current source.



(1) Insert link BR1 if average beam current is not required.

(2) Value depends on video output current stages and picture tube.

Fig.8 Test and application circuit.

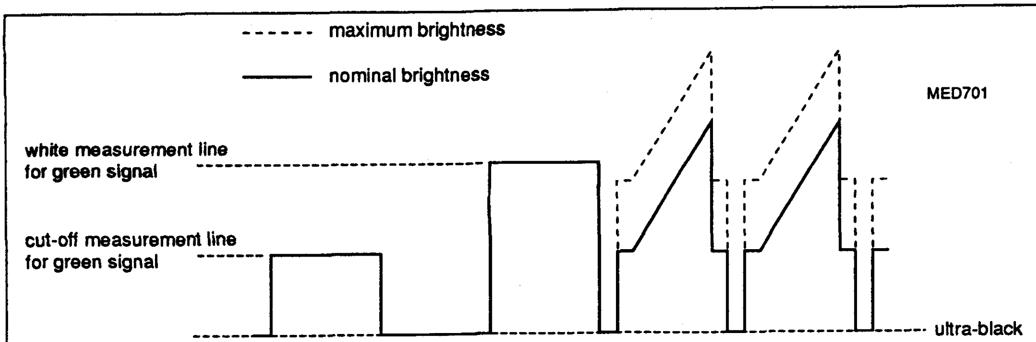


Fig.9 Cut-off and white level measurement pulses.

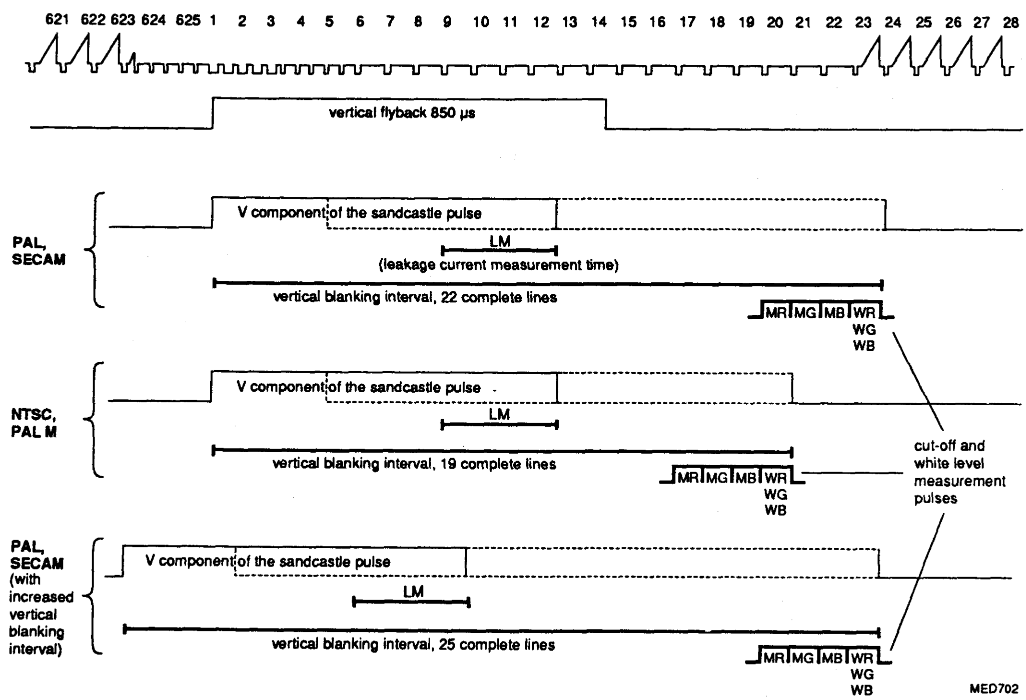


Fig.10 Leakage current, cut-off and white level current measurement timing diagram.

Video processor, with automatic cut-off control

TDA4686

FEATURES

- Intended for double line frequency application (100/120Hz)
- Operates from an 8V DC supply
- Black level clamping of the colour-difference, luminance and RGB input signals with coupling-capacitor DC level storage
- Two analog RGB inputs, selected either by fast switch signals or the I^2C-bus; brightness and contrast control of these RGB inputs
- Saturation, contrast and brightness adjustment via I^2C-bus
- Same RGB output black levels for Y/CD and RGB input signals
- Timing pulse generation from either a 2- or 3-level sandcastle pulse for clamping, vertical synchronization and cut-off timing pulses
- Automatic cut-off control with picture tube leakage current compensation
- Cut-off measurement pulses after end of the vertical blanking pulse or end of an extra vertical flyback pulse
- Increased RGB signal bandwidths
- Two switch-on delays to prevent discolouration before steady-state operation
- Average beam current and peak drive limiting
- PAL/SECAM or NTSC matrix selection via I^2C-bus
- Emitter-follower RGB output stages to drive the video output stages
- Hue control output for the TDA4555 or TDA4650
- No delay of clamping pulse
- Large luminance, colour difference and RGB bandwidth

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_P	Supply voltage range (pin 5)		7.2	8.0	8.8	V
I_P	Supply current (pin 5)		–	60	–	mA
$V_{8\text{-}(p\text{-}p)}$	Luminance input (peak-to-peak value)		–	0.45	–	V
$V_{6\text{-}(p\text{-}p)}$	–(B-Y) input (peak-to-peak value)		–	1.33	–	V
$V_{7\text{-}(p\text{-}p)}$	–(R-Y) input (peak-to-peak value)		–	1.05	–	V
V_{14}	Three-level sandcastle pulse:	H+V H BK	– – –	2.5 4.5 8.0	– – –	V V V
	Two-level sandcastle pulse:	H+V BK	– –	2.5 4.5	– –	V V
V_i	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (black-to-white value)		–	0.7	–	V
$V_{O(p\text{-}p)}$	RGB outputs at pins 24, 22 and 20 (peak-to-peak value)		–	2.0	–	V
T_{amb}	Operating ambient temperature range		0	–	+70	°C

ORDERING INFORMATION

EXTENDED	PACKAGE			
TYPE NUMBER	PINS	PIN POSITION	MATERIAL	CODE
TDA4686	28	DIL	plastic	SOT117
TDA4686WP	28	PLCC	plastic	SOT261

Video processor, with automatic cut-off control

TDA4686

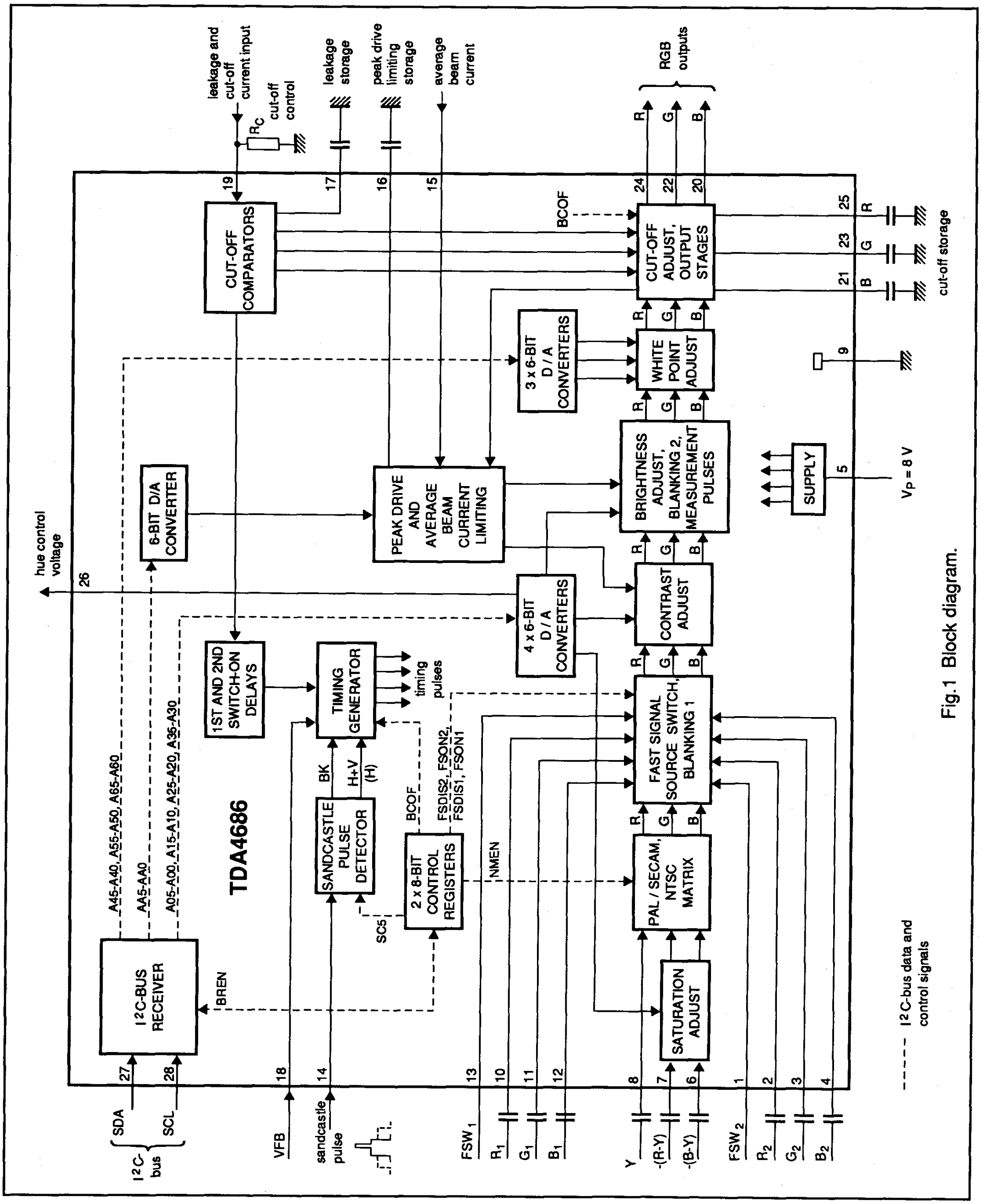


Fig.1 Block diagram.

Video processor, with automatic cut-off control

TDA4686

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
-(B-Y)	6	color difference input -(B-Y)
-(R-Y)	7	color difference input -(R-Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak drive limiting
C_L	17	storage capacitor for leakage current
V_{FB}	18	vertical flyback pulse input
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
HUE	26	hue control output
SDA	27	I²C-bus serial data input/output
SCL	28	I²C-bus serial clock input

PIN CONFIGURATIONS

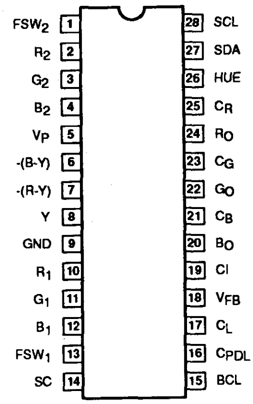


Fig.2(a) Pin configuration for DIL package

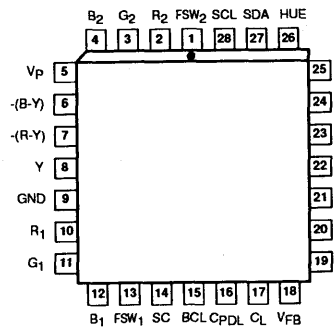


Fig.2(b) Pin configuration for PLCC package

DESCRIPTION

The TDA4686 is a monolithic, integrated circuit with a colour-difference interface for video processing in TV receivers. Its primary function is to process the luminance and colour-difference signals from multistandard colour decoders, TDA4650/TDA4660 or TDA4555, Colour Transient Improvement (CTI) IC, TDA4565, Picture Signal Improvement (PSI) IC, TDA4670, or from a Feature Module.

The required input signals are:
- luminance and negative colour-difference signals
- 2- or 3-level sandcastle pulse for internal timing pulse generation
- I²C-bus data and clock signals for microprocessor control.

Two sets of analog RGB colour signals can also be inserted, e.g., one from a peritelevision connector and the other from an on-screen display generator. The TDA4686 has I²C-bus control of all parameters and functions with automatic cut-off control of the picture tube cathode currents. It provides RGB output signals for the video output stages.

The TDA4686 is a simplified, pin compatible (except pin 18) version of the TDA4680. The module address via the I²C-bus can be used for both ICs; where a function is not included in the TDA4686 then the I2C-bus command is not executed. The differences with the TDA4680 are:
- no automatic white level control; the white levels are determined directly by the I²C-bus data
- RGB reference levels for automatic cut-off control are not generated
- clamping delay is fixed
- only contrast and brightness adjust for the RGB input signals
- the measurement lines are triggered either by the trailing edge of the vertical component of the sandcastle pulse or by the trailing edge of an optional external vertical flyback pulse (on pin 18), according to which occurs first.

The total signal path delay from input to output is:

Y	= 25ns typ., 30ns max.
UV	= 50ns typ., 60ns max.
RGB	= 20ns typ., 25ns max.

The switching signals are matched in timing with the RGB inputs with a maximum delay of 10ns. The switching transition time is 5ns typ., 10ns max.

I^{2}C-BUS CONTROL

The I^{2}C-bus transmitter provides the data bytes to select and adjust the following functions and parameters:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- peak drive limiting
- selects either 3-level or 2-level (5 V) sandcastle pulse
- enables cut-off control control/ enables output clamping
- selects either PAL/SECAM or NTSC matrix
- enables/disables synchronization of the execution of the I^{2}C-bus command with the vertical blanking interval.

I^{2}C-BUS TRANSMITTER AND DATA TRANSFER

I^{2}C-bus specification

The I^{2}C-bus is a bi-directional, two-wire, serial data bus for intercommunication between ICs in an equipment. The microcontroller transmits data to the I^{2}C-bus receiver in the TDA4686 over the serial data line SDA (pin 27) synchronized by the serial clock line SCL (pin 28). Both lines are normally connected to a positive voltage supply through pull-up resistors. Data is transferred when the SCL line is LOW. When SCL is HIGH the serial data line SDA must be stable. A HIGH-to-LOW transition of the SDA line when SCL is HIGH is defined as a start bit. A LOW-to-HIGH transition of the SDA line when SCL is HIGH is defined as a stop bit. Each transmission must start with a start bit and end with a stop bit. The bus is busy after a start bit and is only free again after a stop bit has been transmitted.

I^{2}C-bus receiver

(microcontroller write mode)

Each transmission to/from the I^{2}C-bus transceiver consists of at least three bytes following the start bit. Each byte is acknowledged by an acknowledge bit immediately following each byte. The first byte is the Module ADdress (MAD) byte, also called slave address byte. This includes the module address, 1000100_2 for the TDA4685. The TDA4686 is a slave receiver (R/WN = 0), therefore the module address byte is 10001000_2 (88 Hex), see Fig.3.

The length of a data transmission is unrestricted, but the module address and the correct sub-address must be transmitted before the data byte(s). The order of data transmission is shown in Fig.4 and Fig.5. *Without auto-increment* (BREN = 0 or 1) the module address (MAD) byte is followed by a Sub-ADdress (SAD) byte and one data byte only (Fig.4).

Auto-increment

Auto-increment format enables quick slave receiver initialization by one transmission, when the I^{2}C-bus control bit BREN = 0 (see control register bits of Table 1). If BREN = 1 auto-increment is not possible.

If auto-increment format is selected the MAD byte is followed by a SAD byte and by the data bytes of consectutive sub-addresses (Fig.5). All sub-addresses from 00 to 0F are automatically incremented, the sub-address counter wraps round from 0F to 00. Reserved sub-addresses 07, 08, 09, 0B, 0E and 0F are treated as legal but have no effect. Sub-addresses outside the range 00 and 0F are not acknowledged by the device.

The sub-addresses are stored in the TDA4686 to address the following parameters and functions, see Table 1:

- brightness adjust
- saturation adjust
- contrast adjust
- hue control voltage
- RGB gain adjust
- peak drive limitting adjust
- control register functions.

The data bytes (D7-D0 of Table 1) provide the data of the parameters and functions for video processing.

Control Register 1

NMEN (NTSC - Matrix ENable):
 0 = PAL/SECAM matrix
 1 = NTSC matrix.

BREN (Buffer Register ENable):
 0 = new data is enabled as soon as it is received
 1 = data is stored in buffer registers and is transferred to the data registers during the next vertical blanking interval. The I^{2}C-bus transceiver does not accept any new data until this data is transferred into the data registers.

SC5 (SandCastle 5 V):
 0 = 3-level sandcastle pulse
 1 = 2-level (5 V) sandcastle pulse.

Control Register 2

FSON2 - Fast Switch 2 ON

FSDIS2 - Fast Switch 2 DISable

FSON1 - Fast Switch 1 ON

FSDIS1 - Fast Switch 1 DISable

MSB							LSB	
1	0	0	0	1	0	0	0	ACK

◄—— module address ——► R/WN

Fig.3 The module address byte.

Table 1 Sub-address (SAD) and data bytes

FUNCTION	SAD (Hex)	MSB 7	DATA BYTE 6	5	4	3	2	1	LSB 0
Brightness	00	0	0	A05	A04	A03	A02	A01	A00
Saturation	01	0	0	A15	A14	A13	A12	A11	A10
Contrast	02	0	0	A25	A24	A23	A22	A21	A20
Hue control voltage	03	0	0	A35	A34	A33	A32	A31	A30
Red gain	04	0	0	A45	A44	A43	A42	A41	A40
Green gain	05	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06	0	0	A65	A64	A63	A62	A61	A60
Reserved	07	0	0	x	x	x	x	x	x
Reserved	08	0	0	x	x	x	x	x	x
Reserved	09	0	0	x	x	x	x	x	x
Peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Reserved	0B	x	x	x	x	x	x	x	x
Control Register 1	0C	SC5	x	BREN	x	NMEN	x	x	x
Control Register 2	0D	x	x	x	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Reserved	0E	x	x	x	x	x	x	x	x
Reserved	0F	x	x	x	x	x	x	x	x

The RGB input signals are selected by FSON2 and FSON1 or FSW_2 and FSW_1:

- FSON2 has priority over FSON1;
- FSW_2 has priority over FSW_1;
- FSDIS1 and FSDIS2 disable FSW_1 and FSW_2 (see Table 2).

BCOF - Black level Control OFf:

0 = automatic cut-off control enabled

1 = automatic cut-off control disabled; RGB outputs are clamped to fixed DC levels.

When the supply voltage has dropped below approximately 6.0 V (usually occurs when the TV receiver is switched on or the supply voltage is interrupted) all data and function bits are set to 01_{Hex}.

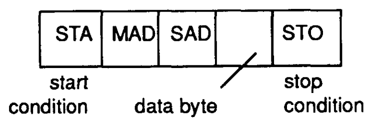


Fig.4 Data transmission without auto-increment (BREN = 0 or 1).

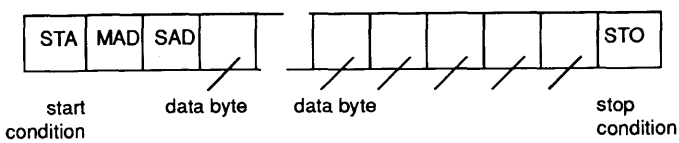


Fig.5 Data transmission with auto-increment (BREN = 0).

Table 2 Signal input selection by the fast source switches

I²C-BUS CONTROL BITS				ANALOG SWITCH SIGNALS		INPUT SELECTED		
FSON2	FSDIS2	FSON1	FSDIS1	FSW_2 (pin 1)	FSW_1 (pin 13)	RGB_2	RGB_1	Y/CD
L	L	L	L	L	L			ON
				L	H		ON	
				H	X	ON		
L	L	L	H	L	X			ON
				H	X	ON		
L	L	H	X	L	X		ON	
				H	X	ON		
L	H	L	L	X	L			ON
				X	H		ON	
L	H	L	H	X	X			ON
L	H	H	X	X	X		ON	
H	X	X	X	X	X	ON		

Note to Table 2

Where L is a logic LOW (< 0.4 V), H is a logic HIGH (> 0.9 V), X is "don't care", and ON is the selected signal input.

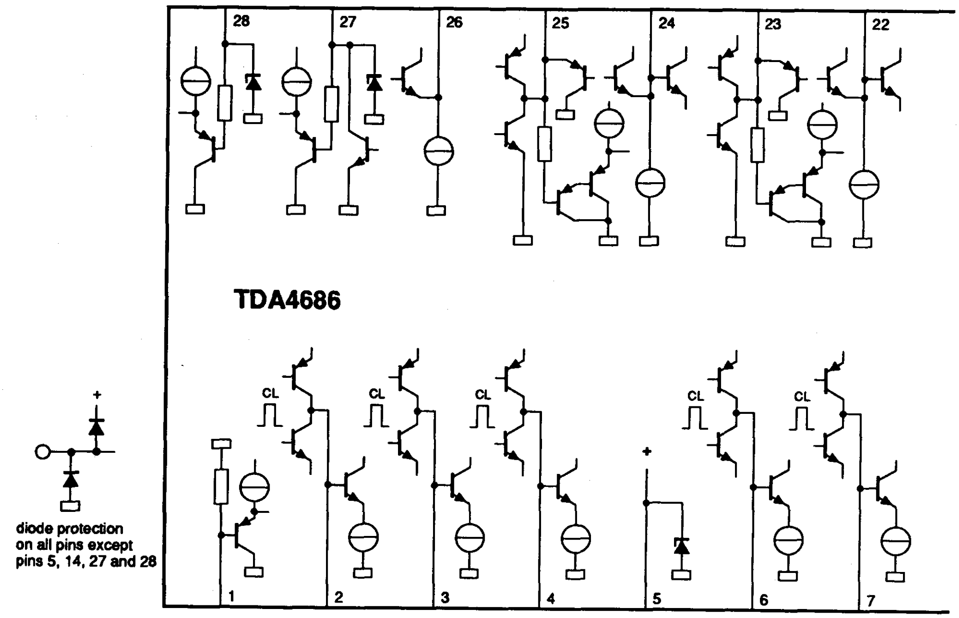


Fig.6(a) Internal circuits (continued in Fig.6b).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	–	8.8	V
V_I	voltage range (pins 1 to 8, 10 to 13, 16, 21, 23, 25, 27 and 28)	−0.1	V_P	V
	voltage range (pins 15, 18 and 19)	−0.7	V_P + 0.7	V
V_{14}	sandcastle pulse voltage range	−0.7	V_P + 5.8	V
I_{AV}	current range (pins 20, 22 and 24)	4	−10	mA
I_M	peak current range (pins 20, 22 and 24)	4	−20	mA
I_{26}	output current range	0.6	−8	mA
T_{stg}	storage temperature range	−20	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
P_{tot}	total power dissipation	–	1.2	W

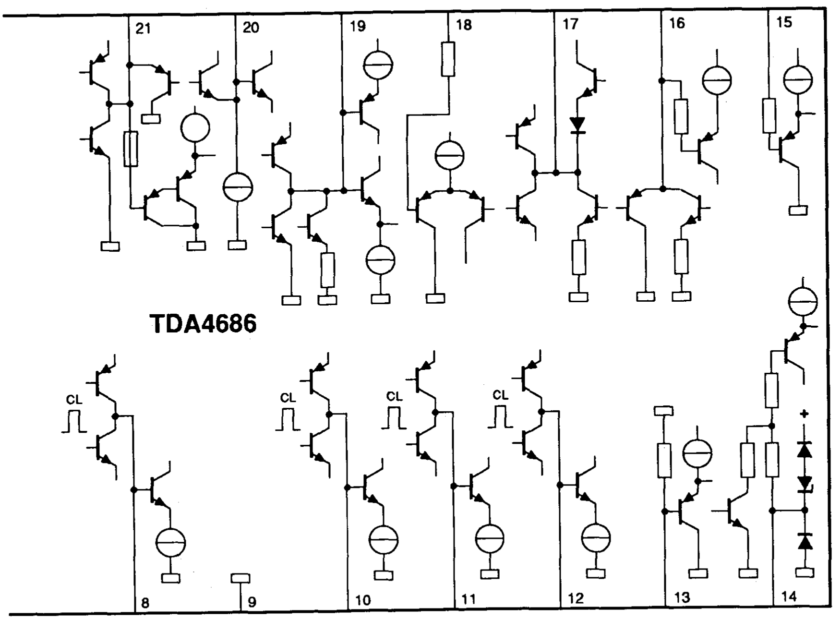


Fig.6(b) Internal circuits (continued from Fig.6a).

CHARACTERISTICS

All voltages are measured in test circuit of Fig.7 with respect to GND (pin 9); V_P = 8.0 V; T_{amb} = 25 °C:

- at nominal signal amplitudes (black-to-white) at output pins 24, 22 and 20,
- at nominal settings of brightness, contrast, saturation and white level control,
- without beam current or peak drive limiting; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 5)		7.2	8.0	8.8	V
I_P	supply current (pin 5)		–	60	–	mA
Colour-difference inputs						
$V_{6(p-p)}$	-(B-Y) input (peak-to-peak value)	note 1 and note 2	–	1.33	–	V
$V_{7(p-p)}$	-(R-Y) input (peak-to-peak value)	note 1 and note 2	–	1.05	–	V
$I_{6,7}$	input current	during line scan	–	–	± 0.1	μA
		at black level clamping	± 100	–	–	μA
$R_{6,7}$	input resistance		10	–	–	MΩ
$V_{6,7}$	internal DC bias voltage	at black level clamping	–	4.1	–	V
Luminance/sync (VBS)						
$V_{i(p-p)}$	luminance input at pin 8 (peak-to-peak value)	note 2	–	0.45	–	V
V_8	internal DC bias voltage	at black level clamping	–	4.1	–	V
I_8	input current	during line scan	–	–	± 0.1	μA
		at black level clamping	± 100	–	–	μA
R_8	input resistance		10	–	–	MΩ
R_1, G_1 and B_1 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 10, 11 and 12 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{10/11/12}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{10/11/12}$	input current	during line scan	–	–	± 0.1	μA
		at black level clamping	± 100	–	–	μA
$R_{10/11/12}$	input resistance		10	–	–	MΩ
R_2, G_2 and B_2 inputs						
$V_{i(p-p)}$	black-to-white input signals at pins 2, 3 and 4 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{2/3/4}$	internal DC bias voltage	at black level clamping	–	5.7	–	V
$I_{2/3/4}$	input current	during line scan	–	–	± 0.1	μA
		at black level clamping	± 100	–	–	μA
$R_{2/3/4}$	input resistance		10	–	–	MΩ
PAL/SECAM and NTSC matrix (see note 3)						
	PAL/SECAM matrix	control bit NMEN = 0				
	NTSC matrix	control bit NMEN = 1				

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast signal switch FSW_1 to select Y, CD or R_1, G_1, B_1 inputs control bits FSDIS1, FSON1 (see table 2)						
V_{13}	voltage to select Y and CD		–	–	0.4	V
	voltage range to select R_1, G_1, B_1		0.9	–	3.0	V
R_{13}	internal resistance to ground		–	4.0	–	kΩ
Fast signal switch FSW_2 to select Y, CD / R_1, G_1, B_1 or R_2, G_2, B_2 inputs control bits FSDIS2, FSON2 (see table 2)						
V_1	voltage to select Y, CD/R_1, G_1, B_1		–	–	0.4	V
	voltage range to select R_2, G_2, B_2		0.9	–	3.0	V
R_1	internal resistance to ground		–	4.0	–	kΩ
d_t	difference between transit times for signal switching and signal insertion		—	—	10	ns
Saturation adjust acts on -(R-Y) and -(B-Y) signals under I²C-bus control, sub-address 01_{Hex} (bit resolution 1.5 % of maximum saturation); data byte $3F_{Hex}$ for maximum saturation data byte 23_{Hex} for nominal saturation data byte 00_{Hex} for minimum saturation						
d_s	saturation below maximum	at 23_{Hex}	–	5	–	dB
		at 00_{Hex}; f = 100 kHz	–	50	–	dB
Contrast adjust acts on internal RGB signals under I²C-bus control, sub-address 02_{Hex} (bit resolution 1.5 % of maximum contrast); data byte $3F_{Hex}$ for maximum contrast data byte 22_{Hex} for nominal contrast data byte 00_{Hex} for minimum contrast						
d_c	contrast below maximum	at 22_{Hex}	–	5.0	–	dB
		at 00_{Hex}	–	22	–	dB
Brightness adjust acts on internal RGB signals under I²C-bus control, sub-address 00_{Hex} (bit resolution 1.5 % of maximum brightness); data byte $3F_{Hex}$ for maximum brightness data byte 26_{Hex} for nominal brightness data byte 00_{Hex} for minimum brightness						
d_{br}	black level shift of nominal signal amplitude referred to cut-off measurement level	at $3F_{Hex}$	–	30	–	%
		at 00_{Hex}	–	–50	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
White potentiometers, under I^2C-bus control, sub-addresses 04_{Hex} (red), 05_{Hex} (green) and 06_{Hex} (blue); see note 4. data byte $3F_{Hex}$ for maximum gain; data byte 19_{Hex} for nominal gain; data byte 00_{Hex} for minimum gain						
ΔG_v	relative to nominal gain: increase of gain	at $3F_{Hex}$	–	50	–	%
	decrease of gain	at 00_{Hex}	–	50	–	%
RGB outputs pins 24, 22 and 20 (positive going output signals); see note 5.						
$V_{o(b-w)}$	nominal output signal amplitudes (black-to-white value)		–	2	–	V
	maximum output signal amplitudes (black-to-white value)		3.0	–	–	V
ΔV_o	spread between RGB output signals		–	–	10	%
V_o	minimum output voltages		–	–	0.8	V
	maximum output voltages		6.8	–	–	V
$V_{24,22,20}$	voltage of cut-off measurement line	BCOF = 1 (output clamping)	2.3	2.5	2.7	V
I_{int}	internal current sources		–	5.0	–	mA
R_o	output resistance		–	20	–	Ω
Frequency response						
d	frequency response of Y path (from pin 8 to pins 24, 22, 20)	f = 14 MHz	–	–	3	dB
	frequency response of CD path (from pins 7 to 24 and 6 to 20)	f = 12 MHz;	–	–	3	dB
	frequency response of RGB_1 path (from pins 10 to 24, 11 to 22 and 12 to 20)	f = 22 MHz	–	–	3	dB
	frequency response of RGB_2 path (from pins 2 to 24, 3 to 22 and 4 to 20)	f = 22 MHz	–	–	3	dB
Sandcastle pulse detector (control bit SC5 = 0) three level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	for H pulses (line count)		4.0	4.5	5.0	V
	for burst key pulses (clamping)		7.6	–	V_P + 5.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sandcastle pulse detector (control bit SC5 = 1) two level; notes 6 and 7						
V_{14}	required voltage range for H and V blanking pulses		2.0	2.5	3.0	V
	burst key pulses		4.0	4.5	V_P + 5.8	V
Sandcastle pulse detector						
I_{14}	output current	V_{14} = 0 V	–	–	–100	μA
t_d	leading edge delay of the clamping pulse		–	0	–	μs
VFB (note 7)						
V_{18}	vertical flyback pulse	for LOW	–	–	2.5	V
		for HIGH	4.5	–	–	V
	internal voltage	pin 18 open (note 8)	–	5.0	–	V
I_{18}	input current		–	–	5	μA
Average beam current limiting (note 9)						
$V_{c(15)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(15)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(15)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(15)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Peak drive limiting voltage (note 10) internal peak drive limiting level (V_{pdl}) acts on RGB outputs under I²C-bus control, sub-address $0A_{Hex}$						
$V_{20/22/24}$	level for minimum RGB outputs	at byte 00_{Hex}	–	–	3.0	V
	level for maximum RGB outputs	at byte $3F_{Hex}$	7.0	–	–	V
I_{16}	charge current		–	–1	–	μA
	discharge current	during peak white	–	5	–	mA
V_{16}	internal voltage limitation		4.5	–	–	V
$V_{c(16)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(16)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(16)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(16)}$	voltage difference for full brightness reduction		–	–1.6	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic cut-off control (notes 7, 11, 12 and 13) see Fig.9						
V_{19}	cut-off measurement voltage (V_{MEAS})		–	–	V_P −1.4	V
I_{19}	output current		–	–	−60	µA
	input current		150	–	–	µA
	additional input current	switch-on delay 1	–	0.5	–	mA
$V_{24,22,20}$	monitor pulse amplitude (under I²C-bus control, sub-address $0A_{Hex}$)	switch-on delay 1 (note 14)	–	V_{pdl} −0.1	–	V
V_{19}	voltage threshold for picture tube cathode warm-up	switch-on delay 1	–	4.5	–	V
	internally controlled voltage (V_{REF})	during leakage measurement period	–	2.7	–	V
ΔV_{19}	voltage difference between V_{MEAS} and V_{REF}		–	1.0	–	V
Cut-off storage						
$I_{21/23/25}$	charge and discharge currents	during cut-off measurement lines	–	± 0.3	–	mA
	current	outside measurement	–	–	± 0.1	µA
Leakage storage						
I_{17}	charge and discharge currents	during leakage measurement period	–	± 0.4	–	mA
	current	outside measurement	–	–	± 0.1	µA
V_{17}	voltage for reset to switch-on below		–	2.5	–	V
Hue control (note 14) under I²C-bus control, sub-address 03_{Hex} data byte $3F_{Hex}$ for maximum voltage data byte 20_{Hex} for nominal voltage data byte 00_{Hex} for minimum voltage						
V_{26}	output voltage	at byte $3F_{Hex}$	4.8	–	–	V
		at byte 20_{Hex}	–	3.0	–	V
		at byte 00_{Hex}	–	–	1.2	V
I_{int}	current of the internal current source at pin 26		500	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2C-bus receiver clock SCL (pin 28)						
f_{SCL}	input frequency range		0	–	100	kHz
V_{IL}	input voltage LOW		–	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	–	V
I_{IL}	output current LOW		–	–	–10	μA
I_{IH}	input current HIGH		–	–	10	μA
t_d	pulse time LOW		4.7	–	–	μs
	pulse time HIGH		4.0	–	–	μs
t_r	rise time		–	–	1.0	μs
t_f	fall time		–	–	0.3	μs
I^2C-bus receiver data input/output SDA (pin 27)						
V_{IL}	input voltage LOW		–	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	–	V
I_{IL}	output current LOW		–	–	–10	μA
I_{IH}	input current HIGH		–	–	10	μA
I_{OL}	output current LOW		3.0	–	–	mA
t_r	rise time		–	–	1.0	μs
t_f	fall time		–	–	0.3	μs
$t_{su;DAT}$	data set-up time		0.25	–	–	μs

Notes to the characteristics

1. The values of the -(B-Y) and -(R-Y) colour-difference input signals are for a 75% colour-bar signal.
2. The pins are capacitively coupled to a low ohmic source, with a recommended maximum output impedance of 600 Ω.
3. PAL/SECAM signals are matrixed by the equation:

$$V_{G-Y} = -0.51\ V_{R-Y} - 0.19\ V_{B-Y}$$

NTSC signals are matrixed by the equations (hue phase shift of −5 degrees):

$$V_{R-Y}^* = 1.57\ V_{R-Y} - 0.41\ V_{B-Y}$$
$$V_{G-Y}^* = -0.43\ V_{R-Y} - 0.11\ V_{B-Y}$$
$$V_{B-Y}^* = V_{B-Y}$$

In the matrix equations:
V_{R-Y} and V_{B-Y} are for conventional PAL demodulation axes and amplitudes at the output of the NTSC demodulator.

V_{G-Y}^*, V_{R-Y}^* and V_{B-Y}^* are the NTSC-modified colour-difference signals; this is equivalent to the following demodulator axes and amplification factors:

	NTSC	PAL
(B-Y)* demodulator axis	0°	0°
(R-Y)* demodulator axis	115°	90°
(R-Y)* amplification factor	1.97	1.14
(B-Y)* amplification factor	2.03	2.03

$V_{G-Y}^* = -0.27\ V_{R-Y}^* - 0.22\ V_{B-Y}^*$.

4. The white potentiometers affect the amplitudes of the RGB output signals.
5. The RGB outputs at pins 24, 22 and 20 are emitter followers with current sources.
6. Sandcastle pulses are compared with internal threshold voltages independent from V_P. The threshold voltages separate the components of the sandcastle pulse. The particular component is generated when the voltage on pin 14 exceeds the defined internal threshold voltage. The internal threshold voltages (control bit SC5 = 0) are:
   1.5 V for horizontal and vertical blanking pulses (H and V blanking pulses),
   3.5 V for horizontal pulses,
   6.5 V for the burst key pulse.
   The internal threshold voltages, control bit SC5 = 1, are:
   1.5 V for horizontal and vertical blanking pulses,
   3.5 V for the burst key pulse.
7. Vertical signal blanking is determined by the vertical component of the sandcastle pulse. The leakage and the RGB cut-off measurement lines are positioned in the first four complete lines after the end of the vertical component. In this case, the RGB output signals are blanked until the end of the last measurement line; see Fig.9(a). If an extra vertical flyback pulse VFB is applied to pin 18, the four measurement lines start in the first complete line after the end of the VFB pulse; see Fig.9(b). In this case the output signals are blanked either until the end of the last measurement line or until the end of the vertical component of the sandcastle pulse, according to which occurs last.
8. If no VFB pulse is applied, pin 18 can be left open or connected to V_P.
9. Average beam current limiting reduces the contrast, at minimum contrast it reduces the brightness.
10. Peak drive limiting reduces the RGB outputs by reducing the contrast, at minimum contrast it reduces the brightness. The maximum RGB outputs are determined via the I^2C-bus under sub-address $0A_{Hex}$. When an RGB output exceeds the maximum voltage, peak drive limiting is delayed by one horizontal line.
11. During leakage current measurement, the RGB channels are blanked to ultra-black level. During cut-off measurement one channel is set to the measurement pulse level, the other channels are blanked to ultra-black. Since the brightness adjust shifts the colour signal relative to the black level, the brightness adjust is disabled during the vertical blanking interval (see Fig.8 and Fig.9).
12. During picture cathode warm-up (first switch-on delay) the RGB outputs (pins 24,22 and 20) are blanked to the ultra-black level during line scan. During the vertical blanking interval a white-level monitoring pulse is fed out on the RGB outputs and the cathode currents are measured. When the voltage threshold on pin 19 is greater than 4.5 V, the monitor pulse is switched off and cut-off control is activated (second switch-on delay). As soon as cut-off control stabilize, RGB output blanking is removed.
13. The cut-off measurement level range at the RGB outputs is 1 to 5 V. The recommended value is 3 V.
14. The hue control output at pin 26 is an emitter follower with current source.

Video processor, with automatic cut-off control

TDA4686

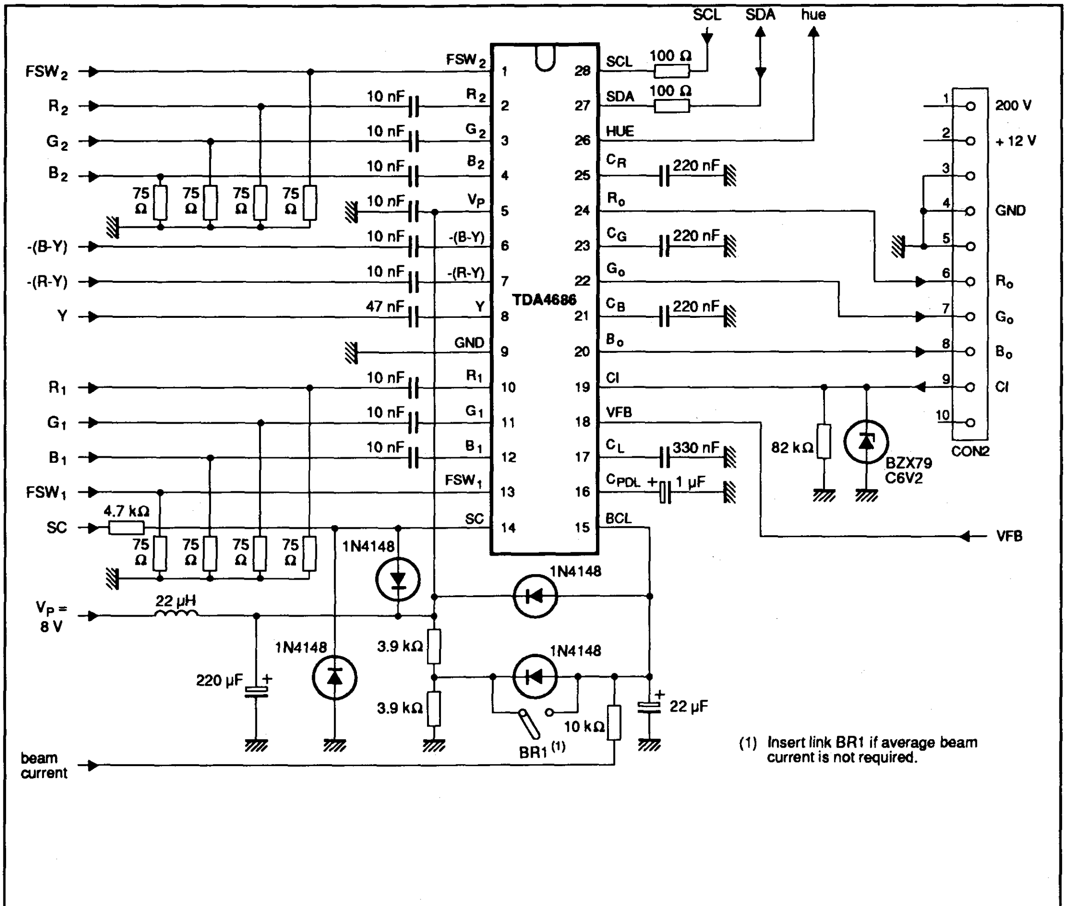


Fig.7 Test and application circuit.

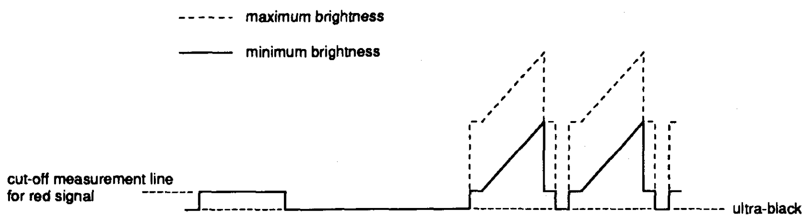


Fig.8 Cut-off measurement pulse.

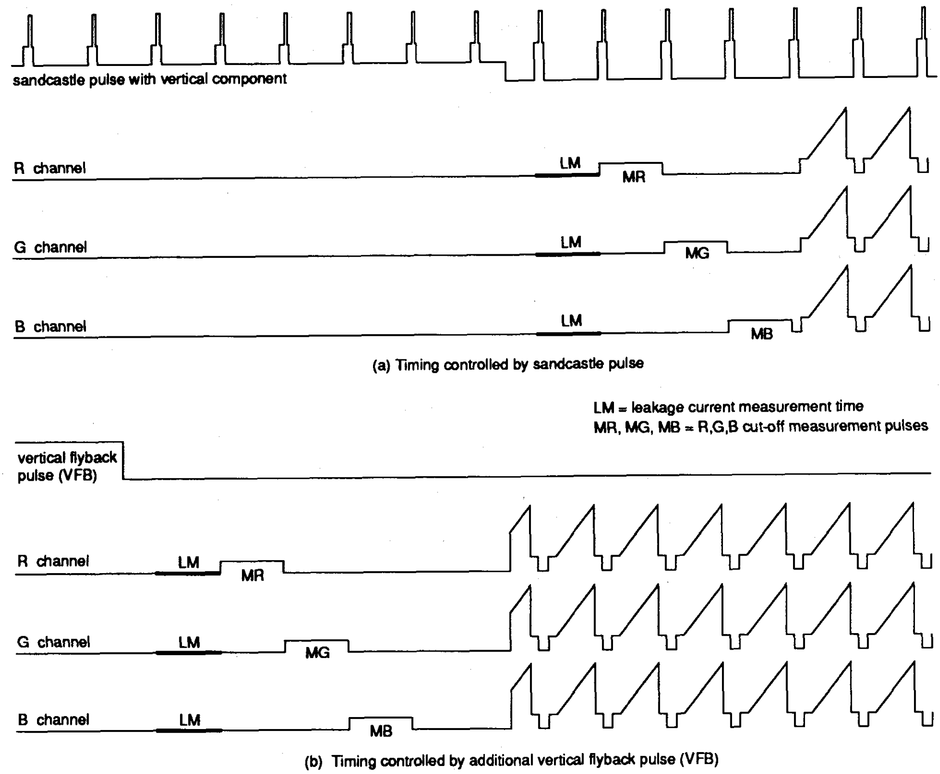


Fig.9 Leakage and cut-off current measurement timing diagram.

Purchase of Philips I²C components conveys a license under the Philips I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Sync separation circuit for video applications

TDA4820T

FEATURES

- Fully integrated, few external components
- Positive video input signal, capacitively coupled
- Operates with non-standard video input signals
- Black level clamping
- Generation of composite sync slicing level at 50% of peak sync voltage
- Vertical sync separator with double slope integrator
- Delay time of the vertical output pulse is determined by an external resistor
- Vertical sync generation with a slicing level at 40% of peak sync voltage
- Output stage for composite sync
- Output stage for vertical sync

GENERAL DESCRIPTION

The TDA4820T is a monolithic integrated circuit including a horizontal and a vertical sync separator, offering composite sync and vertical sync extracted from the video signal.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		10.8	12	13.2	V
I_P	supply current (pin 1)		–	8	12	mA
$V_{2(p-p)}$	input voltage amplitude (peak-to-peak value)		0.2	1	3	V
$V_{sync(p-p)}$	sync pulse input voltage amplitude (pin 2) (peak-to-peak value)		50	300	500	mV
V_o	maximum vertical sync output voltage (pin 6)	$I_6 = -1$ mA	10.0	–	–	V
V_o	maximum composite sync output voltage (pin 7)	$I_7 = -3$ mA	10.0	–	–	V
V_o	minimum output voltage (pins 6 and 7)	$I_{6,7} = 1$ mA	–	–	0.6	V
T_{amb}	operating ambient temperature range		0	–	+ 70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4820T	8	mini-pack	plastic	SO8; SOT96A

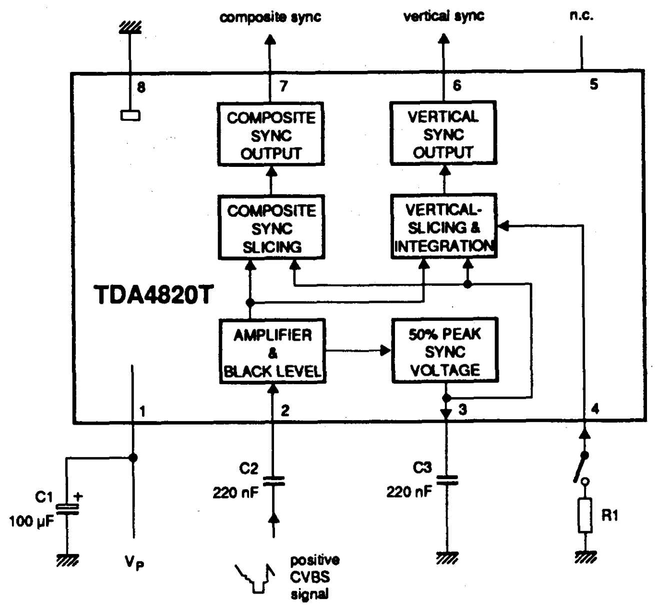


Fig. 1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage
V_{CVBS}	2	video input signal
SLEV	3	slicing level
VDEL	4	vertical integration delay time
n.c.	5	not connected
VSYN	6	vertical sync output signal
CSYN	7	composite sync output signal
GND	8	ground

PIN CONFIGURATION

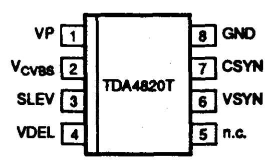


Fig. 2 Pin configuration.

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

- Video amplifier and black level clamping
- 50% peak sync voltage
- Composite sync slicing
- Vertical slicing and double slope integrator
- Vertical sync output
- Composite sync output

Video amplifier and black level clamping (pin 2)

The sync separation circuit TDA4820T is designed for positive video input signals.

The video signal (supplied via capacitor C2 at pin 2) is amplified by approximately 15 in the input amplifier. The black level clamping voltage (approximately 2 V) is stored by capacitor C2.

50% peak sync voltage (pin 3)

From the black level and the peak sync voltage, the 50% value of the peak sync voltage is generated and stored by capacitor C3 at pin 3.

A slicing level control circuit ensures a constant 50% value, as long as the sync pulse amplitude at pin 2 is between 50 mV and 500 mV, independent of the amplitude of the picture content.

Composite sync slicing

A comparator in the composite sync slicing stage compares the amplified video signal with the DC voltage derived from 50% peak sync voltage. This generates the composite sync output signal.

Vertical slicing and double slope integrator

Vertical slicing compares the composite sync signal with a DC level equal to 40 % of the peak sync voltage, similar to the composite sync slicing.

With signal interference (reflections or noise) the reduced vertical slicing level ensures more energy for the vertical pulse integration. The slope is double-integrated to eliminate the influence of signal interference.

The vertical integration delay time t_{dV} can be set from typically 45 µs (pin 4 open) to typically 18 µs (pin 4 grounded). Between these maximum and minimum values, t_{dV} can be set by a resistor R1 from pin 4 to ground. For optimum sync behaviour with input line sync pulses only, R1 has to be ≥ 3.3 kΩ. In this case t_{dV} is typically ≥ 23 µs.

Vertical sync output
Composite sync output

Both output stages are emitter followers with bias currents of 2 mA.

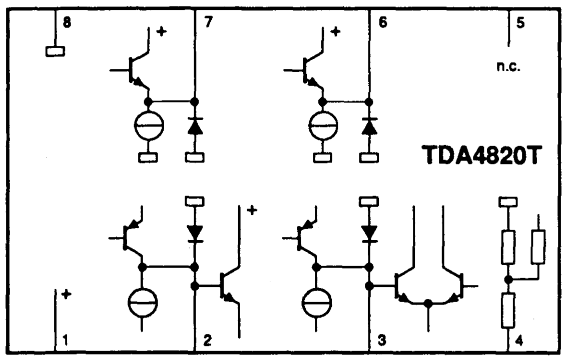


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	0	13.2	V
V_i	input voltage (pin 2)	−0.5	6	V
I_o	output current (pin 6 and pin 7)	3	−10	mA
T_{stg}	storage temperature range	−25	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
T_j	maximum junction temperature	−	150	°C
P_{tot}	total power dissipation	−	500	mW

CHARACTERISTICS

All voltages measured to GND (pin 8); V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		10.8	12.0	13.2	V
I_P	supply current (pin 1)		4	8	12	mA
Video amplifier						
$V_{2(p-p)}$	input amplitude (peak-to-peak value)	positive video signal AC coupled	0.2	1	3	V
$V_{sync\ (p-p)}$	sync pulse amplitude (pin 2) (peak-to-peak value)	composite sync slicing level 50% for $0.2\ V \leq V_{2(p-p)} \leq 1.5\ V$	50	300	500	mV
Z_s	source impedance		–	–	200	Ω
Black level clamping						
I_2	discharge current of C2	during video content	–	5	–	μA
	charge currents of C2	sync below slicing level	–	–40	–	μA
		sync above slicing level	–	–25	–	μA
		during black level	–	–20	–	μA
50% peak sync voltage						
I_3	discharge current of C3	during video content	–	16	–	μA
	maximum charge current of C3		–	–345	–	μA
	reduced charge current of C3	during vertical sync	–	–255	–	μA
	charge current of C3	during sync pulse	–	–160	–	μA
Composite sync slicing (see Fig.4)						
	composite sync slicing level	$0.2\ V \leq V_{2(p-p)} \leq 1.5\ V$	–	50	–	%
t_{dH}	horizontal delay time (pin 7)	maximum load at pin 7: $C_L \leq 5$ pF; $R_L \geq 100$ kΩ	–	250	500	ns
Vertical sync separation (see Fig.5)						
	slicing level for vertical sync	$0.2\ V \leq V_{2(p-p)} \leq 1.5\ V$	–	40	–	%
t_{dV}	vertical leading edge delay times (pin 6)	pin 4 open	30	45	60	μs
		pin 4 grounded	11	18	25	μs
Vertical and composite sync outputs						
V_o	maximum vertical sync output voltage (pin 6)	I_6 = –1 mA	10.0	10.5	11.5	V
V_o	maximum composite sync output voltage (pin 7)	I_7 = –3 mA	10.0	10.5	11.5	V
V_o	minimum output voltages (pins 6 and 7)	$I_{6,7}$ = 1 mA	0.1	0.3	0.6	V
t_W	vertical sync pulse width	pin 4 open; standard signal of 625 lines	–	180	–	μs

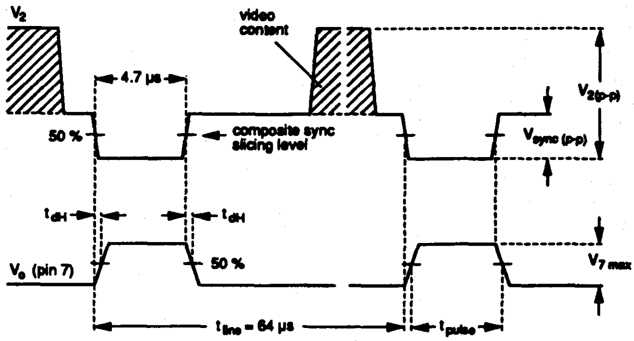
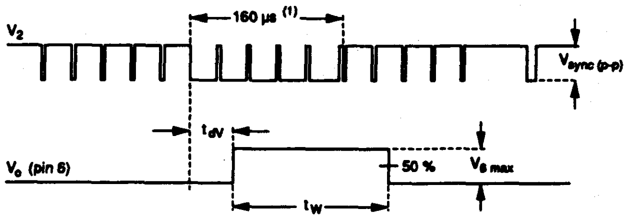


Fig.4 Typical horizontal sync signal.



(1) due to 625 line standard

Fig.5 Typical vertical sync signal.

Octuple 6-bit DAC with I²C-bus

TDA8444/AT/T

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	$V_P = 12$ V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; $I_O = -2$ mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

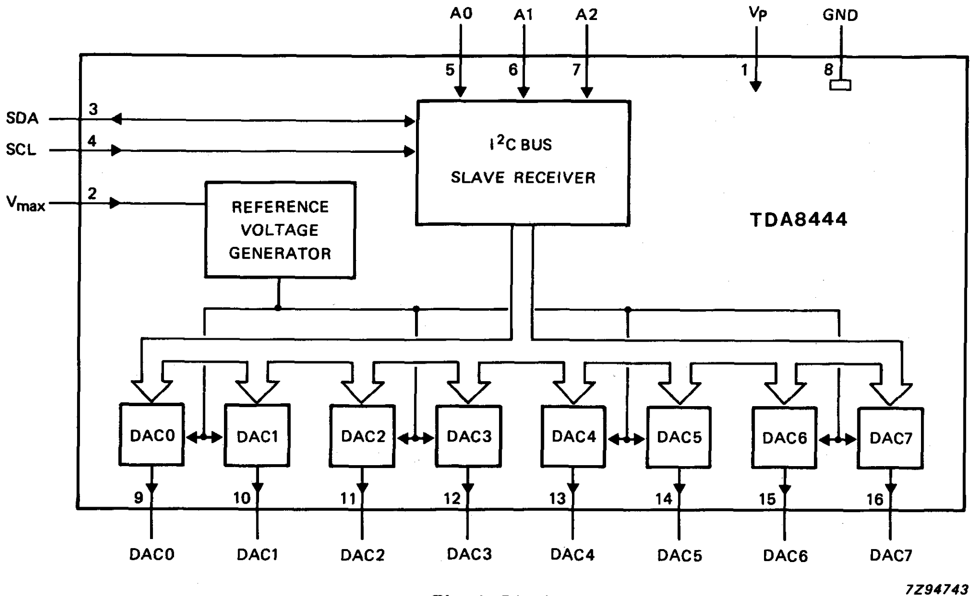


Fig. 1 Block diagram.

PINNING

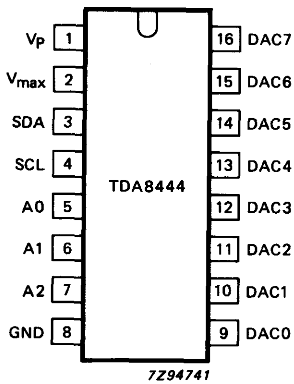
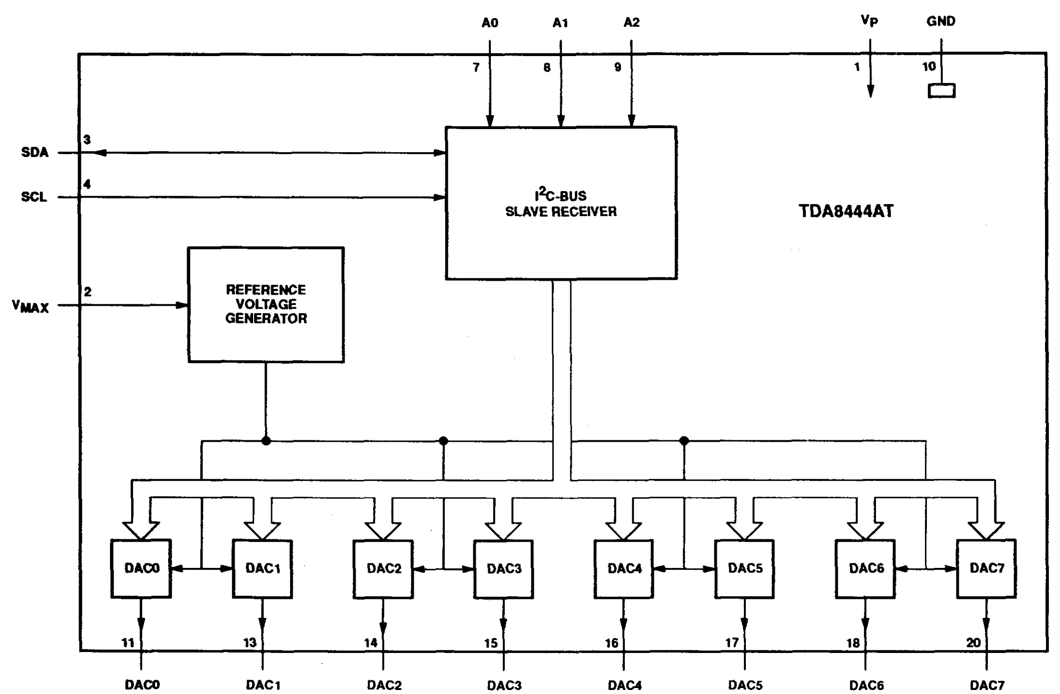


Fig. 2 Pinning diagram.

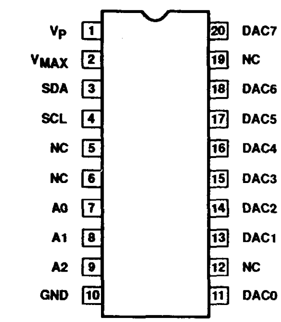
1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I²C-bus serial data input/output
4	SCL	I²C-bus serial data clock
5	A0	programmable address bits for I²C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

Octuple 6-bit DAC with I²C-bus TDA8444/AT/T

BLOCK DIAGRAM – TDA8444AT (SO-20)

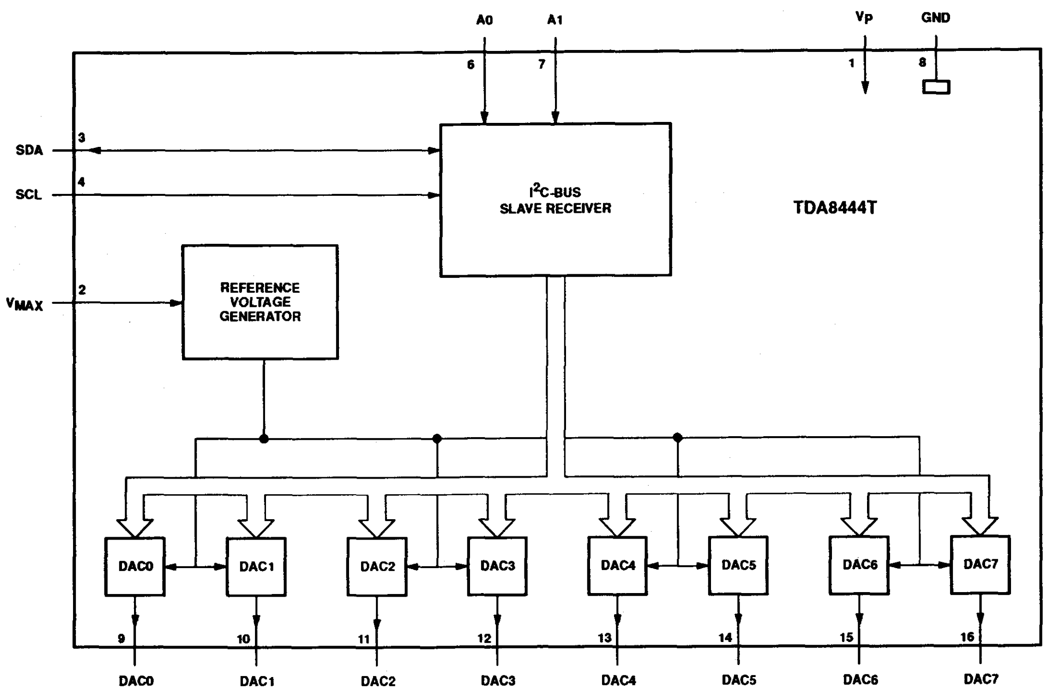


PIN CONFIGURATION AND DESCRIPTION – TDA8444AT (SO-20, SOT-163)

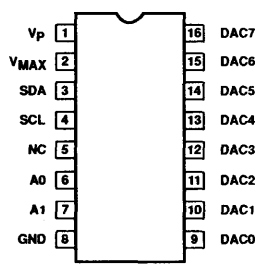


1	V_P	Positive supply voltage
2	V_{MAX}	Control input for DAC maximum output voltage
3	SDA	I²C bus serial data input/output
4	SCL	I²C bus serial data clock
7	A0	Programmable address bits for I²C bus slave receiver
8	A1	Programmable address bits for I²C bus slave receiver
9	A2	Programmable address bits for I²C bus slave receiver
10	GND	Ground
11, 13-18, 20	DAC0-7	Analog voltage outputs

BLOCK DIAGRAM – TDA8444T (SO-16)



PIN CONFIGURATION AND DESCRIPTION – TDA8444T (SO-16, SOT-162)



1	V_P	Positive supply voltage
2	V_{MAX}	Control input for DAC maximum output voltage
3	SDA	I²C bus serial data input/output
4	SCL	I²C bus serial data clock
6	A0	Programmable address bits for I²C bus slave receiver
7	A1	Programmable address bits for I²C bus slave receiver
8	GND	Ground
9-16	DAC0-7	Analog voltage outputs

FUNCTIONAL DESCRIPTION

I²C-bus

The TDA8444 I²C-bus interface is a receive-only slave. Data is accepted from the I²C-bus in the following format:

S	0	1	0	0	A2	A1	A0	0	A	I3	I2	I1	I0	SD	SC	SB	SA	A	X	X	D5	D4	D3	D2	D1	D0	A	P

|← address byte →| |← instruction byte →| |← first data byte →|

Where:

S	= start condition	A2, A1, A0	= programmable address bits
P	= stop condition	I3, I2, I1, I0	= instruction bits
A	= acknowledge	SD, SC, SB, SA	= subaddress bits
X	= don't care	D5, D4, D3, D2, D1, D0	= data bits

Fig. 3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C-bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C-bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C-bus specifications.* Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to Vp for An = 1. If the inputs are left floating, An = 1 will result.

FUNCTIONAL DESCRIPTION (continued)

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0.5 to 10.5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_1$	–0.5	18	V
Supply current (source)		$I_P = I_1$	–	–10	mA
		$I_P = I_I$	–	40	mA
I²C-bus line voltage		$V_{3,4}$	–0.5	5.9	V
Input voltage		V_I	–0.5	$V_P + 0.5$	V
Output voltage		V_O	–0.5	$V_P + 0.5$	V
Maximum current on any pin (except pins 1 and 8)		$\pm I_{max}$	–	10	mA
Total power dissipation		P_{tot}	–	500	mW
Operating ambient temperature range		T_{amb}	–20	+ 70	°C
Storage temperature range		T_{stg}	–65	+ 150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 75 K/W

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C; V_P = 12 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Voltage level for power-on reset		V_1	1	–	4.8	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$I_P = I_1$	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input (pin 2)	V_P = 12 V	$V_{max} = V_2$	1.0	–	10.5	V
Pin 2 current	V_2 = 1 V	I_2	–	–	−10	μA
	$V_2 = V_P$	I_2	–	–	10	μA
SDA, SCL inputs (pins 3 and 4)						
Input voltage range		V_I	0	–	5.5	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	–	V
Input current LOW	$V_{3;4}$ = 0.3 V	I_{IL}	–	–	−10	μA
Input current HIGH	$V_{3;4}$ = 6 V	I_{IH}	–	–	±10	μA
SDA output (pin 3)						
Output voltage LOW	I_3 = 3 mA	V_{OL}	–	–	0.4	V
Sink current		I_O	3	8	–	mA
Address inputs (pins 5 to 7)						
Input voltage range		V_I	0	–	V_P	V
Input voltage LOW		V_{IL}	–	–	1	V
Input voltage HIGH		V_{IH}	2.1	–	–	V
Input current LOW		I_{IL}	–	−7	−12	μA
Input current HIGH		I_{IH}	–	–	1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
DAC outputs (pins 9 to 16)						
Output voltage range		V_O	0.1	–	V_P–0.5	V
Minimum output voltage	data = 00; I_O = –2 mA	V_{Omin}	0.1	0.4	0.8	V
Maximum output voltage	data = 3F; I_O = –2 mA					
at $V_{max} = V_P$		V_{Omax}	10	10.5	11.5	V
at $1 < V_{max} < 10.5$ V		V_{Omax}		see note		V
Output sink current	V = V_P; data = 1F	I_O	2	8	15	mA
Output source current	V = 0V; data = 1F	I_O	–2	–	–6	mA
Output impedance	data = 1F; $-2 < I_O < +2$ mA	Z_O	–	4	50	Ω
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV
Deviation from linearity	I_O = –2 mA; N ≠ 32		0	–	50	mV
Deviation from linearity	I_O = –2 mA; N = 32		0	–	70	mV

Note to the characteristics

$V_O = 0.95\ V_{max} + V_{Omin}$.

APPLICATION INFORMATION

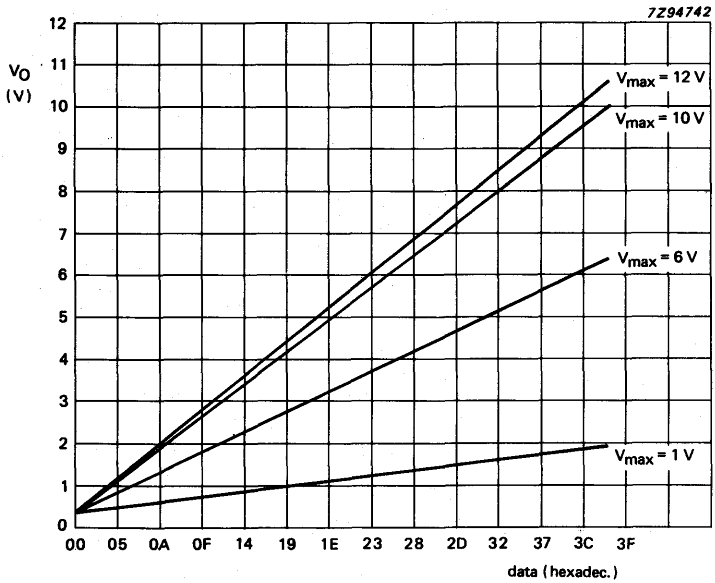


Fig. 4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.

Fast RGB/YC switch for digital decoding

TDA8446

Supersedes data of October 1990

FEATURES

- R, G, B clamped inputs
- Luminance and chrominance difference matrix
- Y clamped inputs
- Fast switching between internal and incoming Y
- Chroma input
- Amplifier with selectable gain
- 3-State switch for chroma output

APPLICATIONS

- Digital TV system
- Desktop video architecture

GENERAL DESCRIPTION

The TDA8446 is a video switch which has been designed for use in the DMSD-SCART digital video system (DMSD = Digital Multistandard System Decoder). The device is intended for matrixing incoming RGB signals and for switching between luminance signals.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply power range	10.8		13.2	V
T_{amb}	Operating ambient temperature range	0		70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				ORDER CODE
	PINS	PIN POSITION	MATERIAL	CODE	
TDA8446	20	DIL	plastic	SOT146	9350 396 50112

Fast RGB/YC switch for digital decoding

TDA8446

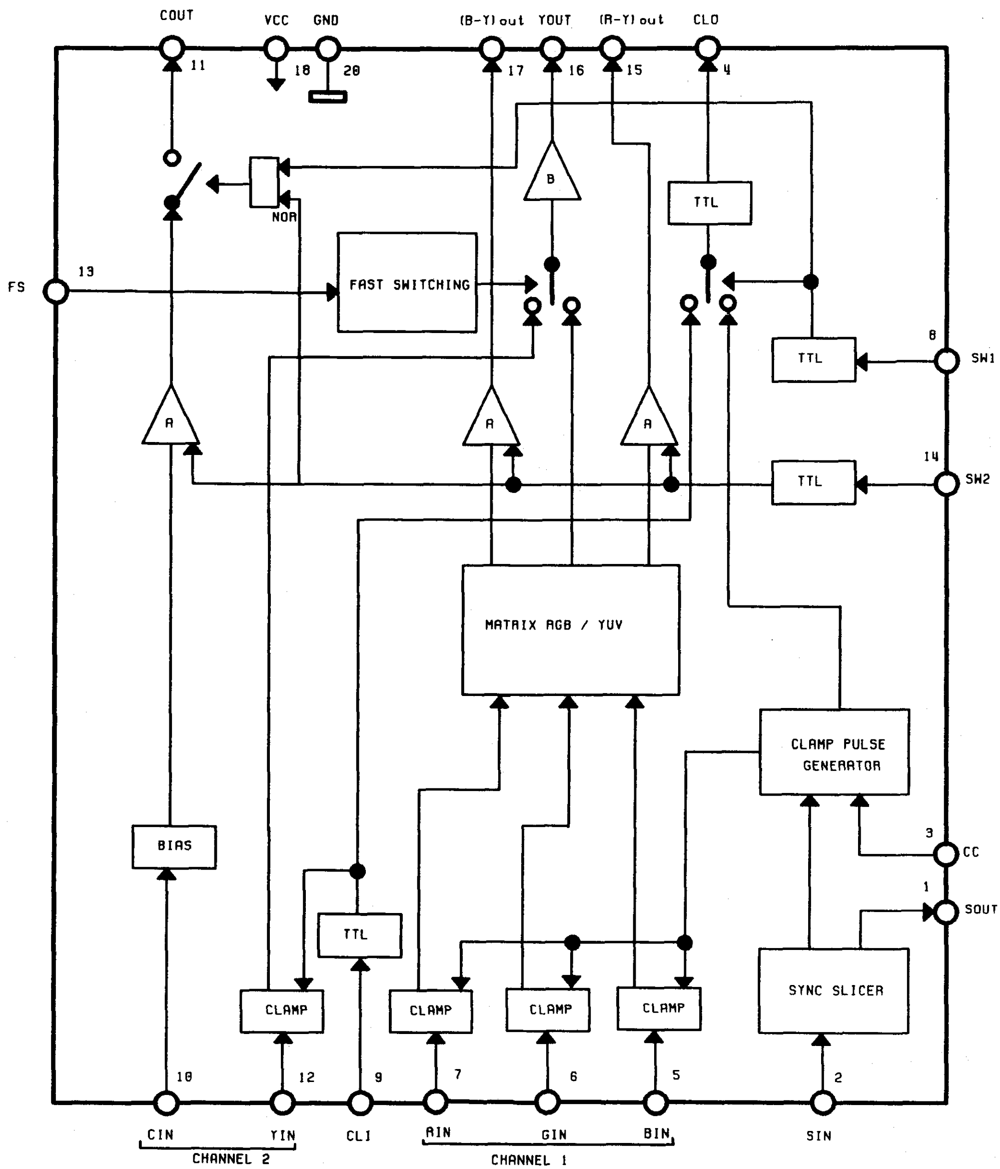


Figure 1. Block Diagram

Fast RGB/YC switch for digital decoding TDA8446

PINNING

SYMBOL	PIN	DESCRIPTION
S_{OUT}	1	Synchronization signal output. This output provides the synchronization information extracted from the incoming signal at pin S_{IN}.
S_{IN}	2	Synchronization signal input; CSYNC or CVBS signal from the periconnector.
CC	3	Clamp capacitor connection. With the external circuitry at this pin the timing for clamping pulse is generated. The generated pulse clamps the RGB inputs.
CLO	4	Clamp pulse output
B_{IN}	5	B signal input
G_{IN}	6	G signal input
R_{IN}	7	R signal input
SW1	8	Clamp control signal input. This TTL signal is used to select the clamp signal. A 'LOW' at this input forces the IC to output the generated clamp pulse.
CLI	9	Clamping pulse input. This TTL signal indicates the black level clamping period for the incoming Y signal (active HIGH).
C_{IN}	10	Chrominance signal input
C_{OUT}	11	Chrominance signal output
Y_{IN}	12	Luminance signal input: this input accepts also CVBS signal.
FS	13	Fast switching signal input; this signal is used to control fast switching of the luminance signals. A 'HIGH' at this input forces the IC to output the internal Y.
SW2	14	Gain control signal input. This TTL signal is used to fix the gain of the chroma amplifiers (A). A 'LOW' at this input forces the gain A at 6dB, (HIGH forces 0dB).
$(R-Y)_{OUT}$	15	(R-Y) signal output
Y_{OUT}	16	Luminance signal output
$(B-Y)_{OUT}$	17	(B-Y) signal output
V_{CC}	18	Supply voltage (+12V)
N.C.	19	Not connected
GND	20	Ground

PIN CONFIGURATION

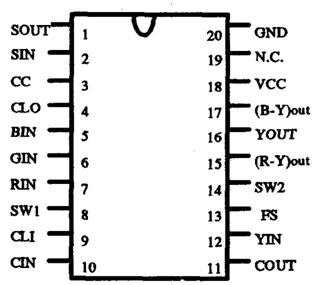


Figure 2. Pin Configuration

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	Supply voltage	−0.3	14	V
	Input voltage	−0.3	12.3	V
T_{stg}	Storage temperature range	−55	+125	°C

HANDLING

ESD according to MIL STD883C – Method 3015 (HBM 1500 ohms, 100pF)
3 pulses + and 3 pulses – on each pin vs. ground; class 2: 2000V to 2999V.

OPERATING SYSTEM

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	10.8		13.2	V
T_{amb}	Operating ambient temperature range	0		+70	°C
TTL inputs (SW1, SW2 and CL1)					
V_{IH}	HIGH input voltage	2		V_{CC}	V
V_{IL}	LOW input voltage	−0.3		+0.8	V
SYNC signal					
VS_{PP}	Sync amplitude	0.2		2.5	V
Fast switching					
V_{IH}	HIGH input voltage	1		3	V
V_{IL}	LOW input voltage			0.4	V
Video inputs					
C_{IN}	Input capacitor		100		nF
Clamp pulse generator					
Rpulse	Resistor		4.7		kΩ
Cpulse	Capactitor		1		nF

CHARACTERISTICS

V_{CC} = 12V, T°C = T_{amb} = 25°C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Supply							
I_{CC}	Supply current			tbf		tbf	mA
RR	Supply voltage rejection	see note 1		30			dB
Y/R,G,B channels							
Vclamp	Video input clamp level	VpinCLI = '1' VpinCC = 6V	Y_{IN}	tbf	5	tbf	V
		I_{IN} = tbf	$(R,G,B)_{IN}$	tbf	8.7	tbf	V
Iclamp	Input clamp current	VpinCC = 6V V_{IN} = 0		tbf			mA
I_{IN}	Input current	V_{IN} = 9V			0.5	tbf	µA
GA	Gain of amplifier A	f = 1 MHz V_{SW2} = 2.0V		–1	0	+1	dB
		V_{SW2} = 0.8V		+5	+6	+7	dB
GB	Gain of amplifier B	f = 1 MHz		–1	0	+1	dB
	RGB matriced according to the equations: Y = 0.30R + 0.59G + 0.11B R-Y = 0.70R – 0.59G – 0.11B B-Y = 0.30R – 0.59G + 0.89B Relative gain difference	see note 4			0	10	%
|ΔG|	Maximum gain variation	100kHz < f < 25MHz			3		dB
R_{OUT}	Output resistance				7		Ω
Δt	Time difference at output	see note 3				25	ns
V_{OUT}	DC output level	VpinCC = 6V		tbf		tbf	V
V_{PP}	Maximum output amplitude on differential	V_{SW2} = 2.0V		2.1			V
	chroma outputs. [(R-Y, (B-Y)]	V_{SW2} = 0.8V		4.2			V
V_{PP}	Maximum output amplitude on Y output			2.1			V
t1	Fast switching delay	see note 2			20		ns
t2	Fast switching time	see note 2			10		ns
I_{IN}	Input current on fast switching control pin	V_{IN} = 0.4V			tbf		µA
		V_{IN} = 1V			tbf		µA

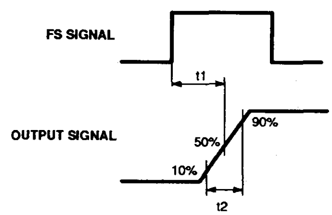
CHARACTERISTICS (Continued)

V_{CC} = 12V, T°C = T_{amb} = 25°C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C channel						
V_{BIAS}	DC level	I_{IN} = 0		5		V
R_{IN}	Internal input resistor			50		kΩ
V_{OUT}	DC output level	I_{IN} = 0	tbf	5.1	tbf	V
GA	Gain of amplifier	f = 1 MHz V_{SW1} = 2.0V V_{SW2} = 2.0V	–1	0	+1	dB
		V_{SW2} = 0.8V	+5	+6	+7	dB
|ΔG|	Maximum gain variation	100kHz < f < 25MHz		3		dB
αoff	Isolation (off state)	V_{SW1} = V_{SW2} = 0.8V f = 5 MHz	60			dB
Z_{HI}	Output impedance	V_{SW1} = 0.8V V_{SW2} = 0.8V	100			kΩ
R_{OUT}	Output resistance			7		Ω
V_{PP}	Maximum output amplitude on C output	V_{SW1} = 2.0V V_{SW2} = 2.0V	2.1			V
		V_{SW2} = 0.8V	4.2			V
TTL inputs (SW1, SW2, CLI)						
I_{IH}	Input current HIGH	V_{IH} = 2V			10	µA
I_{IL}	Input current LOW	V_{IL} = 0.8V			600	µA
CLAMP output (CLO)						
V_{OL}	Output voltage LOW	I_{OL} = tbf			0.4	V
V_{OH}	Output voltage HIGH	I_{OH} = tbf	2.4			V
Synchronization channel						
V_{PP}	Output amplitude		0.2		1.5	V

NOTES:

1. Supply voltage rejection = $20 \log \frac{\text{V2 supply}}{\text{V2 on the output}}$

2. 

3. f = 1MHz
The inputs R_{IN}, G_{IN}, and B_{IN} are connected together.
Δt is the maximum time coincidence error between the luminance and chrominance signals.

4. The relative gain difference is measured when only one input signal (R, G or B) is present.

APPLICATION DIAGRAM

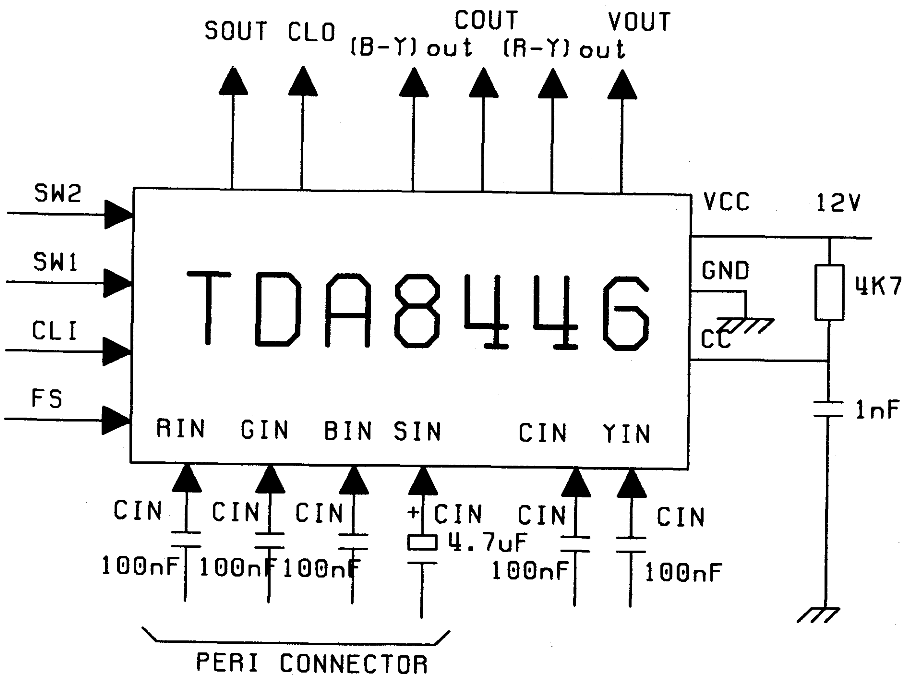


Figure 3. Typical Application Diagram

PAL/NTSC encoder — TDA8501

FEATURES

- Two input stages: R, G, B and –(R–Y), –(B–Y), Y with multiplexing
- Chrominance processing, highly integrated, includes low frequency filters for the colour difference signals, and after the modulator a bandpass filter
- Fully controlled modulator produces a signal according to the PAL or NTSC standard without adjustments
- A free running oscillator. Can be tuned by crystal or by an external frequency source
- Output stages with separated Y + SYNC and chrominance (Y + C, SVHS), and a CVBS output. Signal amplitudes are correct for 75 Ω driving via an external emitter follower. Internal generation of NTSC setup
- Sync separator circuit and pulse shaper, to generate the required pulses for the processing, clamping, blanking, FH/2, and burst pulse
- H/2 control pin. In PAL mode the internally generated H/2 is connected to this pin and the phase of this signal can be reset
- Internal bandgap reference.

GENERAL DESCRIPTION

The TDA8501 is a highly integrated PAL/NTSC encoder IC which is designed for use in all applications where R, G and B or Y, U and V signals require transformation to PAL or NTSC values. the specification of the input signals are fully compatible with the specification of those of the TDA8505 SECAM-encoder.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8501	24	DIL	plastic	SOT234AH2
TDA8501T	24	SO	plastic	SOT137AH1

PAL/NTSC encoder TDA8501

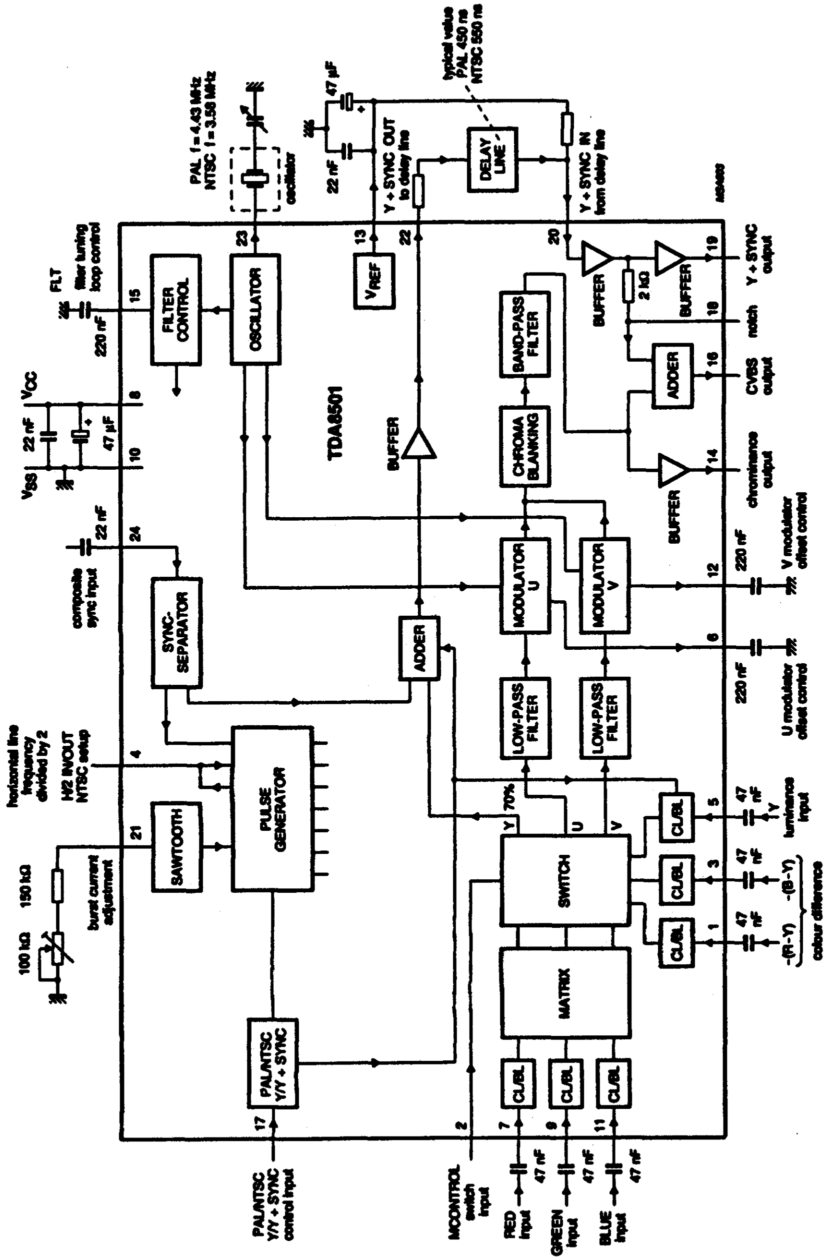


Fig.1 Block diagram.

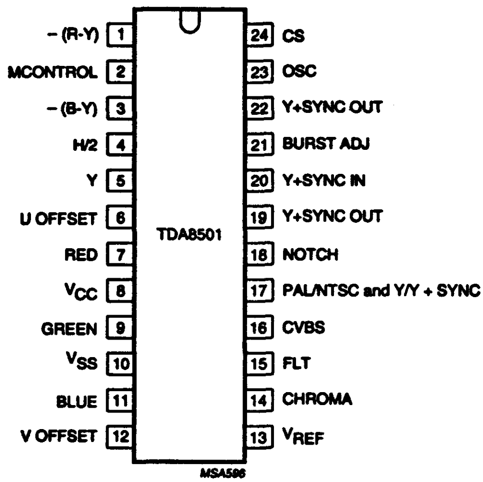


Fig.2 Pin configuration.

PINNING

U and V respectively, are the terms used to describe the colour difference signals at the output of the matrix.

SYMBOL	PIN	DESCRIPTION
−(R−Y)	1	colour difference input signal, for EBU bar (75%) 1.05 V (p-p)
MCONTROL	2	multiplexer switch control input; HIGH = RGB, LOW = −(R−Y), −(B−Y), Y
−(B−Y)	3	colour difference input signal, for EBU bar (75%) 1.33 V (p-p)
H/2	4	line pulse input/output divided-by-2 for synchronizing the internal H/2, if not used, this pin dependent on mode selected, is either left open-circuit, or connected to V_{CC} or to ground (note 1)
Y	5	luminance input signal 1 V nominal without sync
U OFFSET	6	U modulator offset control capacitor
R	7	RED input signal for EBU bar of 75% 0.7 V (p-p)
V_{CC}	8	supply voltage; 5 V nominal
G	9	GREEN input signal for EBU bar of 75% 0.7 V (p-p)
V_{SS}	10	ground (0 V)
B	11	BLUE input signal for EBU bar of 75% 0.7 V (p-p)
V OFFSET	12	V modulator offset control capacitor
V_{REF}	13	2.5 V internal reference voltage output
CHROMA	14	chrominance output
FLT	15	filter tuning loop capacitor

SYMBOL	PIN	DESCRIPTION
CVBS	16	composite PAL or NTSC output, 2 V (p-p) nominal
PAL/NTSC and Y/Y + SYNC	17	four level control pin (note 2)
NOTCH	18	Y + SYNC output via an internal resistor of 2 kΩ; a notch filter can be connected to this pin
Y + SYNC OUT	19	2 V (p-p) nominal Y + SYNC output
Y + SYNC IN	20	Y + SYNC input; (from pin 22) connected to the output of the external delay line
BURST ADJ	21	burst current adjustment via external resistor
Y + SYNC OUT	22	Y + SYNC output 1 V (p-p) nominal, connected to the input of the external delay line
OSC	23	oscillator tuning: connected to either a crystal in series with capacitor to ground, or to an external frequency source via a resistor in series with a capacitor
CS	24	composite sync input, 0.3 V (p-p) nominal

Notes

1. Pin 4: in PAL mode, if not connected to external H2 pulse, this pin is the output for the internally generated H/2 signal.
   Pin 4: in NTSC mode, for internal set-up this pin is connected to ground; when internal set-up is switched off, this pin is connected to V_{CC}.
2. The listed voltages connected to pin 17 (if V_{CC} = + 5 V) enable the following Y (via pin 5) input signal states:
   0 V = PAL mode; at pin 5, Y without sync and input blanking on
   5 V = NTSC mode; at pin 5, Y without sync and input blanking on
   1.8 V = PAL mode; at pin 5, Y with sync and input blanking off
   3.2 V = NTSC mode; at pin 5, Y with sync and input blanking off

FUNCTIONAL DESCRIPTION

The TDA8501 device comprises:

- encoder circuit
- oscillator and filter control
- sync separator and pulse shaper.

Within this functional description, the term Y is used to describe the luminance signal and the terms U and V respectively, are used to describe the colour difference signals.

Encoder circuit

INPUT STAGE

The input stage of the device uses two signal paths (see Fig.1). Fast switching between the two signal paths is achieved by means of the signal path selection switch MCONTROL (pin 2).

R, B AND G INPUT SIGNALS PATH

One signal path provides the connection for R, G and B signal inputs (via pins 7, 9 and 11) which are connected to a matrix via clamping and line blanking circuits. The signal outputs from the matrix are U, V and Y.

For an EBU colour bar of 75% the amplitude of the signal must be 0.7 V (peak-to-peak):

U = 0.493 (B–Y)

V = 0.877 (R–Y)

Y = 0.299 R + 0.587 G + 0.114 B

When selected (via MCONTROL), the U, V signals from the matrix are routed through the selection switch to the low pass filters. The Y signal from the matrix is routed through the selection switch to the adder and combined with the sync pulse from the sync separator and then connected via a buffer internally to pin 22 (Y + SYNC OUT to delay line).

–(R–Y), –(B–Y) AND Y INPUT SIGNALS PATH

A second signal path provides the connection for negative colour difference signal inputs –(R–Y), –(B–Y) i.e. V, U (via pins 1, 3) and luminance Y (via pin 5), which are routed directly to the switch inputs via clamping and line blanking circuits.

The Y input signal (via pin 5) differs from other signal inputs, in that the timing of the internal clamp is after the sync period.

The amplitude and polarity of these colour difference and luminance input signals are processed to provide suitable switch inputs of U, V and Y signal values.

The condition for 75% colour bar is:

pin 1 –(R–Y) = 1.05 V (peak-to-peak)

pin 3 –(B–Y) = 1.33 V (peak-to-peak)

pin 5 Y = 1 V (peak-to-peak) without sync

When selected (via MCONTROL), the U and V signals (via the switch) are routed to the low pass filters. The Y signal (via the switch) is routed via the adder and buffer to pin 22 (Y + SYNC OUT to delay line). Dependent on pin 17 conditioning, the Y signal may have external or internal sync added (see section Four level control pin).

FOUR LEVEL CONTROL PIN

The Y input signal (via pin 5) is conditioned by use of the 4-level control pin (pin 17) to emulate either the PAL or NTSC modes, with sync and input blanking off or without sync and input blanking on.

Pin 17 may be hard wire connected to either ground (LOW for PAL mode) or V_{CC} (HIGH for NTSC mode). External resistors can further modify the voltage level input at pin 17 to condition (pin 5) Y with sync and input blanking off or Y without sync and input blanking on. (see section PAL/NTSC and Y/Y + SYNC).

U AND V SIGNALS

In PAL and NTSC modes the U and V (colour difference) signals at the output of the switch are configured differently as follows:

PAL mode:

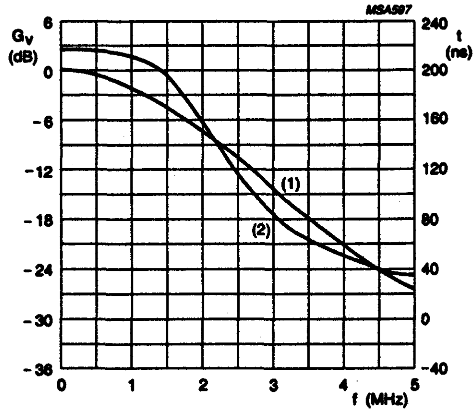
- after the adding of the burst pulse to U and V, these signals are connected to the input of the low pass filters. During the vertical sync period the burst pulse is suppressed.

NTSC mode:

- the burst pulse is only added to U and the gain of the U and V signals is 0.95 of the gain in PAL mode. During the vertical sync period the burst pulse is suppressed.

LOW PASS FILTERS

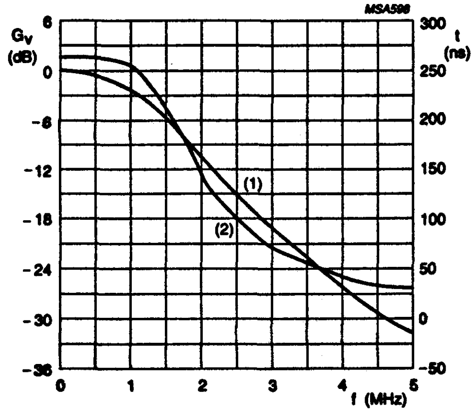
The –3dB nominal frequency response level of the low pass filters are different in PAL and NTSC modes.



(1) frequency response.

(2) group delay.

Fig.3 Low pass filter response for colour difference signals (PAL mode).



(1) frequency response.

(2) group delay.

Fig.4 Low pass filter response for colour difference signals (NTSC mode).

PAL mode: bandwidth = 1.35 MHz nominal (see Fig.3).

NTSC mode: bandwidth = 1.1 MHz nominal (see Fig.4).

The signal outputs of the low pass filters are connected to the signal inputs of the U and V modulators.

U AND V MODULATORS

Two four-quadrant multipliers are used for quadrature amplitude modulation of the U and V signals. The level of harmonics produced by the modulated signals are minimal, because of real multiplication with sinewave carriers.

The unbalance of the modulators is minimized by means of a control loop and two external capacitors, pin 6 for the U modulator and pin 12 for the V modulator. The timing of the control loop is triggered by the H/2 pulse, so that during one sync period the U control is active and during the next sync period the V control is active. In this way, when U and V are both zero, the suppressed carrier is guaranteed to be at a low level.

The internal oscillator circuit generates two sinewave carriers (0 degree and 90 degree). The '0 degree' (0) carrier is connected to the U modulator and the '90 degree' (1) carrier is connected to the V modulator.

PAL mode:

- switched sequentially by the H/2 pulse, the V signal is modulated alternately with the direct and inverse carrier.
- the internal H/2 pulse can be forced into a specific phase by means of an external pulse connected to pin 4 (H/2). Forcing is active at HIGH level. If not used pin 4 can be left open-circuit or connected to ground. If pin 4 is left open, the internally generated H/2 pulse (output) is connected to this pin.

NTSC mode:

- alternation of the V modulation is not allowed. If pin 4 is not used for set-up control (see Y + SYNC, CVBS and Chrominance outputs), it can be left open-circuit or connected to ground.

CHROMINANCE BLANKING

The signal outputs from the modulators are connected to the signal input of the chrominance blanking circuit. To avoid signal distortion that may be caused by the control loop, the signal outputs of the modulators are blanked during the sync period. This prevents signal distortion during the adding of the sync pulse at the CVBS output circuit.

BANDPASS FILTER

A wide symmetrical bandpass filter is used so that a maximum performance of the chrominance for Y + C (SVHS) is guaranteed. This wide curve is possible because of the minimal signal level of the harmonics within the modulators see Figs (PAL mode: 5 and 6); (NTSC mode: 7 and 8) which illustrate the nominal response for PAL and NTSC modes.

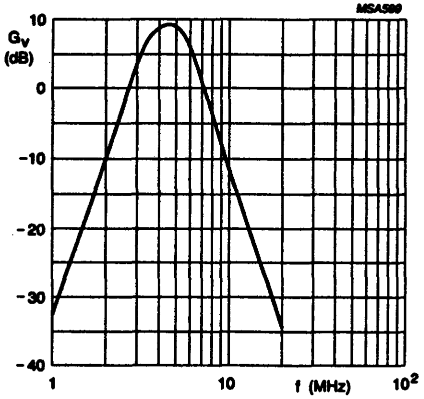
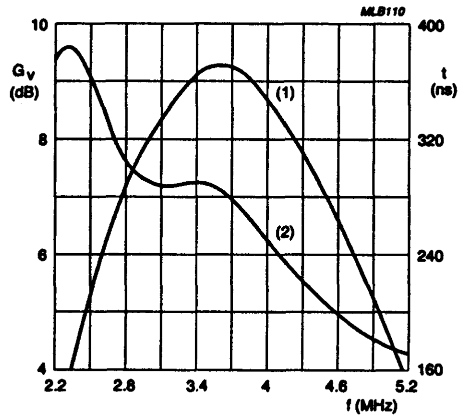


Fig.5 Band pass filter nominal frequency response (PAL mode).



(1) frequency response.

(2) group delay.

Fig.6 Band pass filter nominal frequency/group delay response (PAL mode).

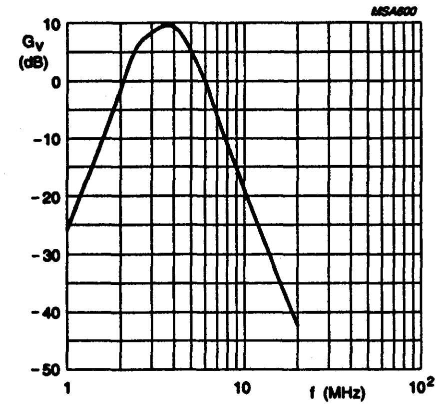
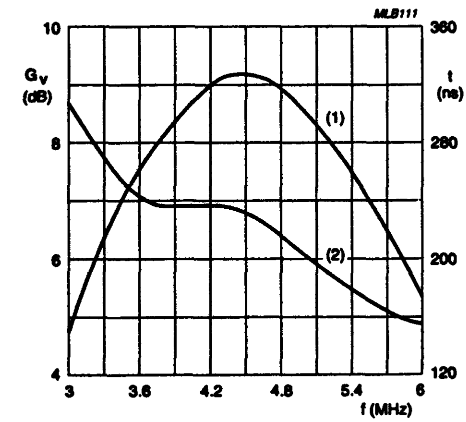


Fig.7 Band pass filter nominal frequency response (NTSC mode).



(1) frequency response.

(2) group delay.

Fig.8 Band pass filter nominal frequency/group delay response (NTSC mode).

Y + SYNC, CVBS AND CHROMINANCE OUTPUTS

The Y signal from the matrix, or the Y signal from pin 5, (selected via the switch) is added with the composite sync signal of the sync separator (dependent on pin 17 conditioning). The output of the adder, nominal 1 V (peak-to-peak), is connected to pin 22 (see Fig.1). Pin 22 is connected to an external delay line.

The delay line is necessary for correct timing of the Y + SYNC signal with the chrominance signal. The output resistor of the delay line is connected to V_{REF} (pin 13). The output of the external delay line is connected to (input) pin 20.

The Y + SYNC (delayed) input signal at pin 20 is amplified via a buffer to a level of 2 V (peak-to-peak) nominal and connected to pin 19 (Y + SYNC output).

The Y + SYNC (delayed) input signal at pin 20 is also connected via an internal resistor of 2 kΩ to the input of the CVBS adder stage. After the internal resistor of 2 kΩ, and before the input of the CVBS adder, an external notch filter can be connected via pin 18.

The chrominance output of the bandpass filter is added with Y + SYNC signal via the CVBS adder. The CVBS (combined video and blanking signal) output of the adder is connected to pin 16 with a nominal amplitude of 2 V (peak-to-peak).

The chrominance output of the bandpass filter is amplified via a buffer and connected to pin 14. The chrominance amplitude corresponds with the value of Y + SYNC signal output at pin 19. Together both outputs give the Y + C (SVHS) signals.

BLACK AND BLANKING LEVELS IN PAL AND NTSC MODES

PAL mode: Fig.9 illustrates the nominal Y + SYNC signal at pin 22, the difference between black and blanking level is 0 mV.

NTSC mode: Fig.10 illustrates the nominal Y + SYNC signal at pin 22, the difference between black and blanking level is 53 mV.

Because of the difference between the black and blanking level in the NTSC mode, there are two options for NTSC.

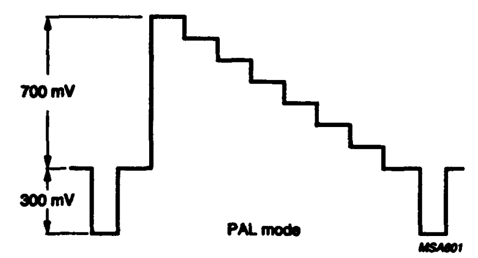


Fig.9 Nominal Y + SYNC signal level at pin 22 (PAL mode).

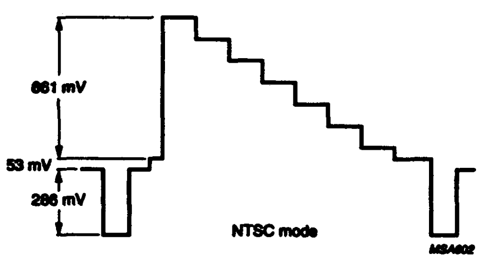


Fig.10 Nominal Y + SYNC signal level at pin 22 (NTSC mode).

NTSC option with internal set-up generation

Pin 4 connected to ground or left open-circuit. The set-up is generated internally and the input signals have the values already specified in section Input stage. The set-up is not suppressed during vertical sync.

NTSC option without internal set-up generation

Pin 4 connected to V_{CC}. This option places some restrictions on the input signals as follows:

- if the output signal must be according to the NTSC standard, the input signals must be generated with a specific set-up level
- for R, G and B inputs a set-up level of 53 mV is required, therefore the specified amplitude must be 753 mV (peak-to-peak) instead of 700 mV (peak-to-peak)
- for U, V and Y inputs a set-up level for Y of 76 mV is required, therefore the specified amplitude must be 1076 mV (peak-to-peak) (without sync) instead of 1 V (peak-to-peak). This option, combined with U, V and Y inputs, is not possible if V_{CC} is < 4.75 V.

Oscillator and Filter Control

The internal crystal oscillator is connected to pin 23 which provides for the external connection of a crystal in series with a trimmer to ground. It is possible to connect an external signal source to pin 23, via a capacitor in series with a resistor. The signal shape is not important. Figure 11 shows the external components connected to pin 23 and the required conditions. The minimum AC current of 50 μA must be determined by the resistors (R_{int} and R_{ext}) and the voltage of the signal source. For example, in this way an external sub-carrier, locked to the sync, can be used.

PAL mode: frequency of the oscillator is 4.433618 MHz.

NTSC mode: frequency of the oscillator is 3.579545 MHz.

The –3 dB of the low pass filters and the centre frequency of the bandpass filter are controlled by the filter control loop and directly coupled to the value of the frequency of the oscillator. The external capacitor of the control loop is connected to pin 15.

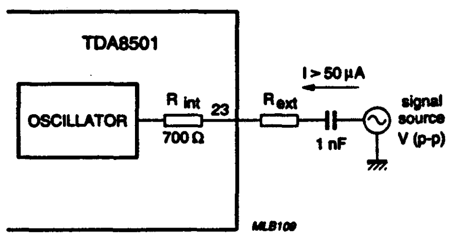


Fig.11 Tuning circuit for external signal source.

Sync separator and Pulse shaper

The composite sync (CS) input at pin 24 (via the sync separator) together with a sawtooth generator provide the source for all pulses necessary for the processing.

Pulses are used for:

- clamping
- video blanking
- H/2
- chrominance blanking
- burst pulse generation for adding to U, V
- pulses for the modulator offset control.

The value of the sawtooth generator output (current) is determined by the value of a fixed resistor to ground which is connected externally at pin 21 (BURST ADJ). When finer tolerance of the burst position is required, the fixed resistor is connected in series with a variable potentiometer to ground. By use of the potentiometer the burst position at the outputs can be finely adjusted, after which the pulse width of the burst and the position and pulse width of all other internal pulses are then determined. When using a fixed resistor with a tolerance of 2%, a tolerance of 10% of the burst position can be expected. Timing diagrams of the pulses are provided by Figs 12 and 13.

H/2 at pin 4 is only necessary in the PAL mode when the internal H/2 pulse requires locking with an external H/2 phase (two or more encoders locked in same phase). The forcing of the internal H/2 to a desired phase is possible by means of an external pulse. Forcing is active at HIGH level.

For the functioning of Pin 4 in the NTSC mode see also section Black and Blanking levels in PAL and NTSC modes.

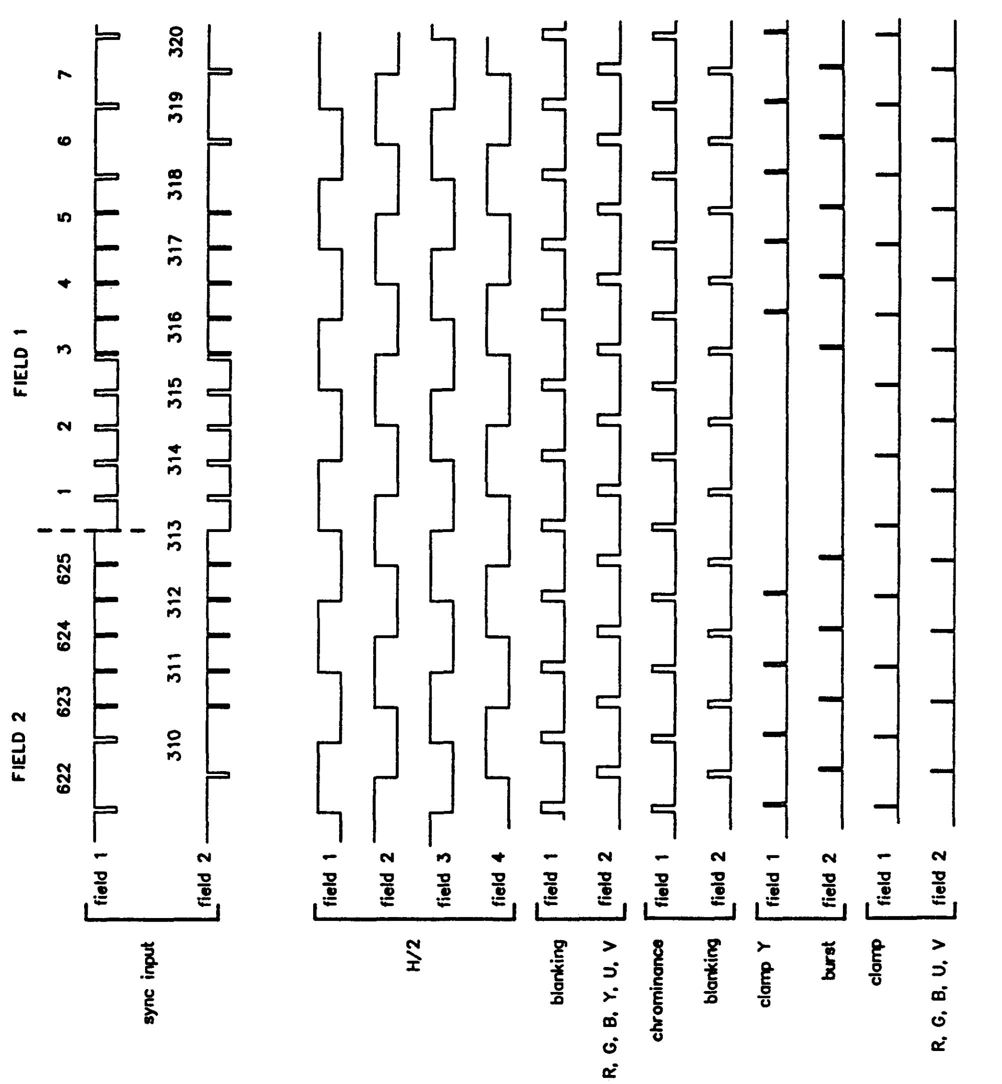


Fig.12 Sync separator and pulse shaper pulses.

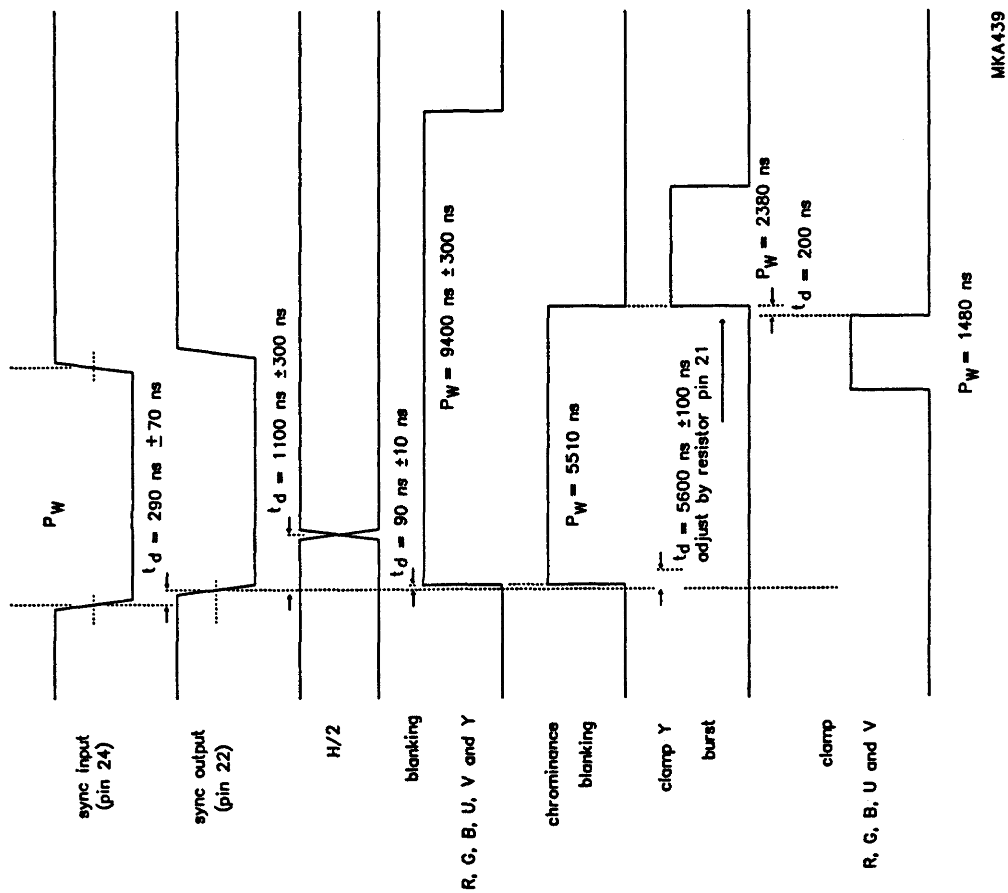


Fig.13 Sync separator and pulse shaper pulse timing levels.

PAL/NTSC and Y/Y + SYNC

Pin 17 is used as a four level control pin to condition the Y/Y + SYNC input signal (via pin 5). Pin 17 is normally connected to ground for PAL mode, or to V_{CC} for the NTSC mode. By use of external resistors (potential divider connected to pin 17), the input blanking at pin 5 can be switched on and off. (see Table 1 and Fig 14).

Table 1 PAL/NTSC Y/Y + SYNC pin 5 options (pin 17 connection configurations).

MODE	PIN 5 STATUS	PIN 17 CONNECTION REQUIREMENT
PAL	Y without sync and input blanking on	pin 17 LOW, connected to V_{SS}
NTSC	Y without sync and input blanking on	pin 17 HIGH, connected to V_{CC}
PAL	Y with sync and input blanking off	pin 17 with 39 kΩ connected to V_{CC} and 22 kΩ connected to V_{SS}
NTSC	Y with sync and input blanking off	pin 17 with 22 kΩ connected to V_{CC} and 39 kΩ connected to V_{SS}

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134); all voltages referenced to V_{SS} (pin 10).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	positive supply voltage	0	5.5	V
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−25	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT234	66 K/W
	SOT137	75 K/W

DC CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; all voltages referenced to ground (pin 10); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 8)						
V_{CC}	supply voltage		4.5	5.0	5.5	V
I_{CC}	supply current		–	40	–	mA
P_{tot}	total power dissipation		–	200	–	mW
V_{REF}	reference voltage output (pin 13)		2.425	2.5	2.575	V

AC CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; composite sync signal connected to pin 24; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Encoder circuit						
Input stage (pins 1, 3, 5, 7, 9 and 11); black level = clamping level						
	maximum signal					
$V_{n(max)}$	from black level positive		–	1.2	–	V
$V_{n(min)}$	from black level negative	only pins 1, 3 and 5	–	0.9	–	V
I_{bias}	input bias current	$V_I = V_{13}$	–	–	< 1	µA
V_I	input voltage clamped	input capacitor connected to ground	tbf	V_{13}	tbf	V
$\|Z_I\|$	input clamping impedance					
		I_I = 1 mA	–	80	–	Ω
		I_O = 1 mA	–	80	–	Ω
	matrix and gain tolerance of R, G and B signals		–	–	< 5	%
G	gain tolerance of Y, –(R–Y) and –(B–Y)		–	–	< 5	%
MCONTROL (pin 2; note 1)						
V_{IL}	LOW level input voltage Y, –(R–Y) and –(B–Y)		0	–	0.4	V
V_{IH}	HIGH level input voltage R, G and B		1	–	5	V
I_I	input current		–	–	–3	µA
t_{sw}	switching time		–	50	–	ns
U modulator offset control (pin 6)						
V_6	DC voltage control level		–	2.5	–	V
I_{LI}	input leakage current		–	–	100	nA
V_{LL}	limited level voltage LOW		–	1.8	–	V
V_{HL}	limited level voltage HIGH		–	3.2	–	V
V modulator offset control (pin 12)						
V_{12}	DC voltage control level		–	2.5	–	V
I_{LI}	input leakage current		–	–	100	nA
V_{LL}	limited level voltage LOW		–	1.8	–	V
V_{HL}	limited level voltage HIGH		–	3.2	–	V
Y + SYNC (pin 22 out to delay circuit)						
R_O	output resistance		–	–	< 25	Ω
I_{sink}	maximum sink current		350	–	–	µA
I_{source}	maximum source current		1000	–	–	µA
V_{BL}	black level output voltage		–	2.5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAL mode; pin 17 = 0 V						
V_{SYNC}	sync voltage amplitude		285	300	315	mV
V_Y	Y voltage amplitude		665	700	735	mV
V_{DIF}	difference between black and blanking level		–	0	–	mV
NTSC mode; pin 17 = 5 V and pin 4 open-circuit or ground						
V_{SYNC}	sync voltage amplitude		270	286	300	mV
V_Y	Y voltage amplitude		628	661	694	mV
V_{DIF}	difference between black and blanking level		–	53	–	mV
BW	frequency response	pin 22 with external load of R = 10 kΩ and C = 10 pF	10	–	–	MHz
	group delay tolerance		–	–	20	ns
t_d	sync delay from pin 24 to pin 22		220	290	360	ns
t_d	Y delay from pin 5 to pin 22		–	10	–	ns
α	Chrominance cross talk	0 dB = 1330 mV (peak-to-peak) = 75% RED	–	–	−60	dB
Y + SYNC IN (pin 20 from delay circuit; note 2)						
I_{bias}	input bias current		–	–	1	μA
V_I	maximum voltage amplitude		–	–	1	V
Y + SYNC OUT (pin 19 output Y (SVHS); note 2)						
R_O	output resistance		–	120	–	ω
I_{sink}	maximum sink current		650	–	–	μA
I_{source}	maximum source current		1000	–	–	μA
V_{BL}	black level output voltage		–	1.65	–	V
G	Y + SYNC gain; from pin 20 to pin 19		–	12	–	dB
BW	frequency response	pin 19 with external load of R = 10 kΩ and C = 10 pF	10	–	–	MHz
	group delay tolerance		–	–	20	ns
α	Chrominance cross talk	0 dB = 1330 mV (peak-to-peak) = 75% RED	–	–	−54	dB

Notes

1. The threshold level of this pin is 700 mV ±20 mV. The specification of the HIGH and LOW levels is according to the SCART fast blanking.
2. Pin 20 condition: black level of input signal must be 2.5 V; amplitude 0.5 V (peak-to-peak) nominal.

AC CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
NOTCH (pin 18)						
R_O	output resistance		1750	2000	2500	Ω
V_{CC}	DC voltage level		–	2.5	–	V
I_{sink}	maximum sink current		350	–	–	μA
Chrominance output (pin 14)						
I_{sink}	maximum sink current		700	–	–	μA
I_{source}	maximum source current		1000	–	–	μA
R_O	output resistance		–	120	–	Ω
ΔV_{DC}	variation of DC voltage level when chrominance signal is blanked and chrominance signal is not blanked		–	–	5	mV
PAL mode; pin 17 = 0 V						
V_O	chrominance output voltage (peak-to-peak) amplitude burst		480	600	720	mV
	ratio: chrominance (75% RED)/burst		2.1	2.2	2.3	
NTSC mode; pin 17 = 5 V						
V_O	chrominance output voltage (peak-to-peak) amplitude burst		460	570	680	mV
	ratio: chrominance (75% RED)/burst		2.1	2.2	2.3	
	carrier suppression when input-signals are 0 V	0 dB = 1330 mV (peak-to-peak)	–	37	–	dB
	phase accuracy (difference between 0 and 90 degree carriers)		–	–	2	degrees
LPF	Low-pass filters	see Figs 3 and 4				
BPF	Band-pass filters	see Figs 5 and 6				
V_n	noise level (RMS value)		–	–	4	mV
BP	burst phase; 0 degrees = phase U carrier					
	PAL mode		–	±135	–	degrees
	NTSC mode		–	180	–	degrees
α	Y + SYNC cross talk (0 to 6 MHz)	0 dB = 1400 mV (peak-to-peak)	–	–	–60	dB

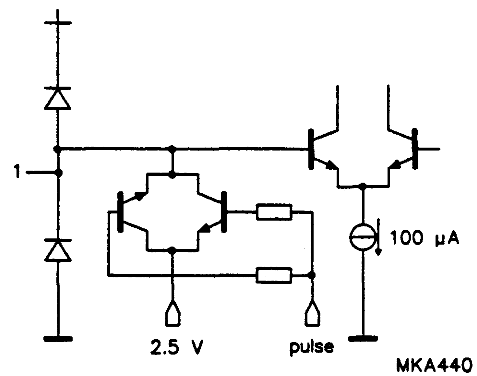
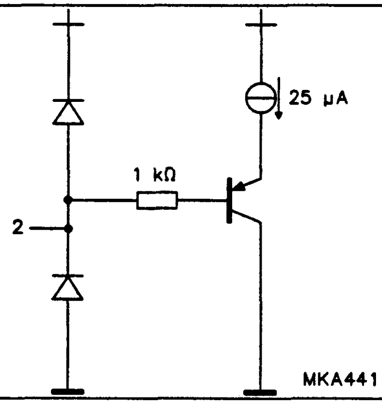
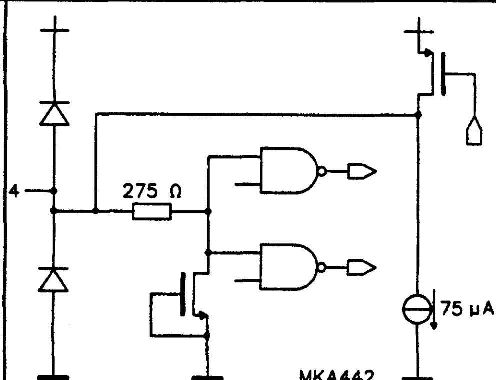
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CVBS output (pin 16)						
I_{sink}	maximum sink current		650	–	–	μA
I_{source}	maximum source current		1000	–	–	μA
V_O	DC voltage level	Y + SYNC = 0	–	1.6	–	V
G	Y + SYNC gain; from pin 20 to pin 16		–	12	–	dB
G	chrominance difference; from pin 14 to pin 16		–	0	–	dB
G_φ	differential phase	note 1	–	–	3	degrees
G_V	differential gain	note 2	–	–	3	dB
R_O	output resistance		–	120	–	Ω
Oscillator output (pin 23)						
OSC	series-resonance	the resonance resistance of the crystal should be < 60 Ω and the parallel capacitance of the crystal should be < 10 pF.				
Filter tuning loop (pin 15)						
V_{DC}	DC control voltage level NTSC		–	0.83	–	V
V_{DC}	DC control voltage level PAL		–	0.88	–	V
V_{DCL}	limited DC-level LOW	I_O = 200 μA	–	0.27	–	V
V_{DCH}	limited DC-level HIGH	I_I = 200 μA	–	1.8	–	V
H2 (pin 4)						
V_{IL}	LOW level input voltage	inactive	0	–	1	V
V_{IH}	HIGH level input voltage	active	4	–	5	V
I_I	current for forcing HIGH		220	–	–	μA
I_O	current for forcing LOW		260	–	–	μA
V_O	voltage out LOW		–	–	< 0.5	V
V_O	voltage out HIGH		4	–	–	V
I_{sink}	maximum sink current		50	–	–	μA
I_{source}	maximum source current		50	–	–	μA
Composite sync input (pin 24)						
V_{SYNC}	SYNC pulse amplitude		75	300	600	mV(p-p)
	slicing level		–	50	–	%
I_I	input current		–	4	–	μA
I_O	maximum output current during SYNC		–	100	–	μA
BURST ADJ (pin 21; note 3)						
BP	DC voltage level		–	V_{REF} (V13)	–	V

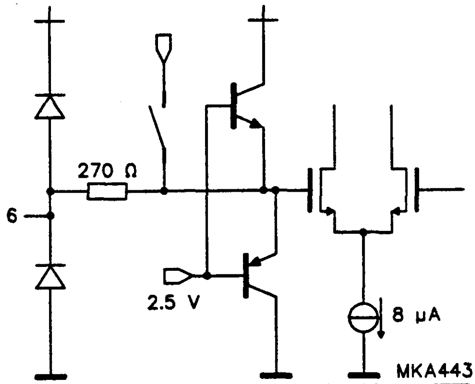
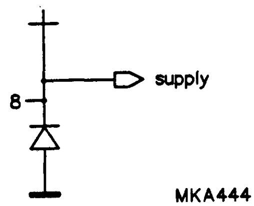
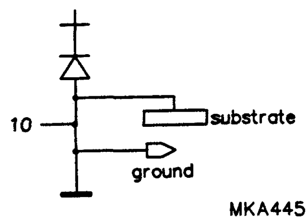
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Control pin PAL/NTSC and Y/Y + SYNC (pin 17; note 4)						
V_I	PAL mode and blanking pin 5 active internal sync added to Y		0	–	1	V
V_I	PAL mode and blanking pin 5 inactive internal sync not added to Y		1.6	–	2.0	V
V_I	NTSC mode and blanking pin 5 active internal sync added to Y		4	–	5	V
V_I	NTSC mode and blanking pin 5 inactive internal sync not added to Y		3	–	3.4	V
I_{bias}	input bias current		–	–	−10	µA

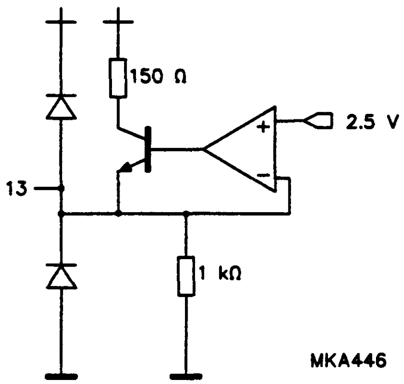
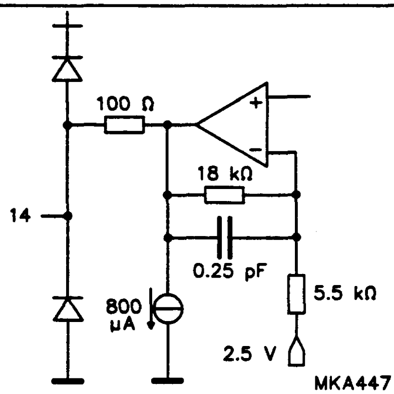
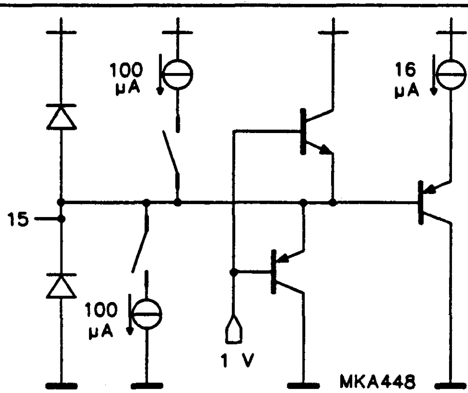
Notes

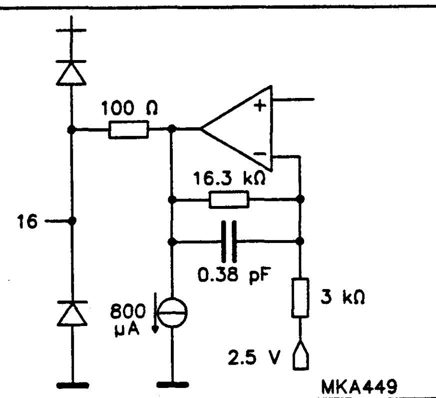
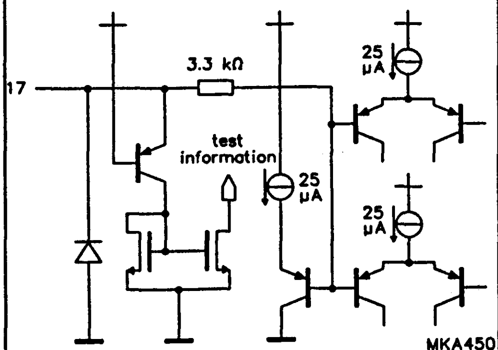
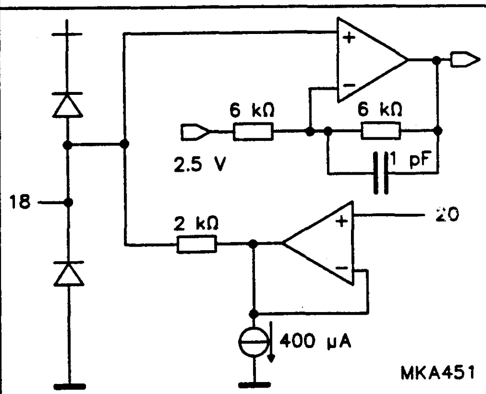
1. Definition: *maximum phase – minimum phase = difference phase*
2. Definition: $\frac{\textit{maximum gain} - \textit{minimum gain}}{\textit{maximum gain}} \times 100 = \textit{difference gain}\,\%$
3. The output impedance of this pin is low (< 100 Ω). The nominal value of the external resistor is 196 kΩ (see also section Sync separator and Pulse shaper).
4. The threshold levels are: 0.25 times V_{CC}, 0.5 times V_{CC} and 0.75 times V_{CC}.

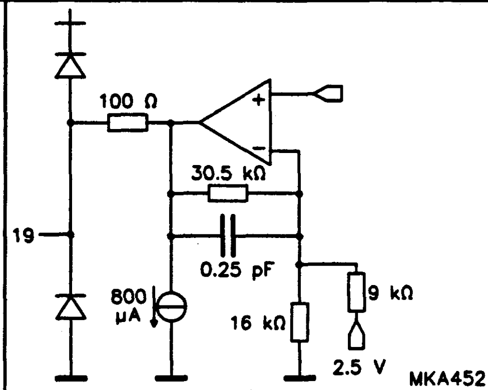
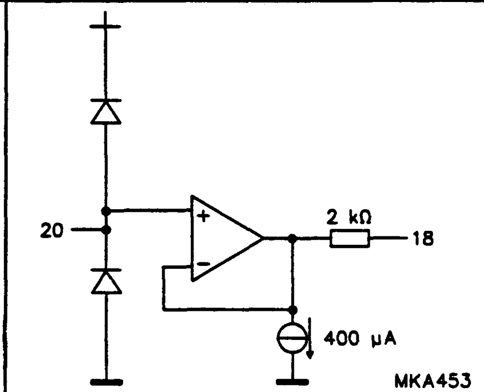
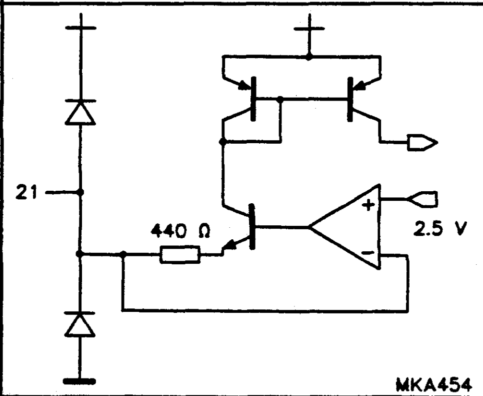
Table 2 Internal circuitry.

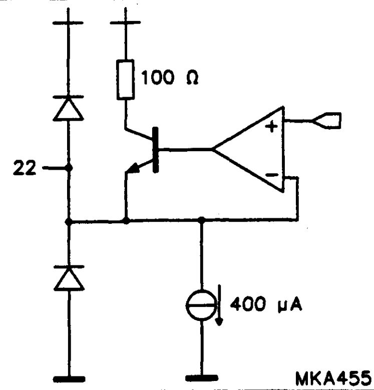
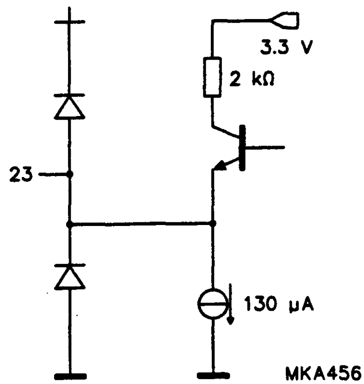
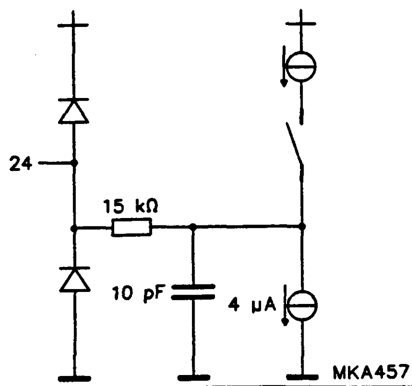
PIN	NAME	CIRCUIT	DESCRIPTION
1	−(R−Y)		−(R−Y) input; connected via 47 nF capacitor 1.05 V (p-p) for EBU bar of 75% see also pins 3, 5, 7, 9 and 11
2	MCONTROL		multiplexer switch control input < 0.4 V Y, U and V > 1 V R, G and B
3	−(B−Y)	see pin 1	−(B−Y) input; connected via 47 nF capacitor 1.33 V (p-p) for EBU bar of 75%
4	H/2 IN/OUT		H/2 input PAL MODE: pin open, output of internal H/2 Forcing possibility NTSC mode: 0 V set-up 5 V no set-up

PIN	NAME	CIRCUIT	DESCRIPTION
5	Y	see pin 1	Y input; connected via 47 nF capacitor 1 V (p-p) for EBU bar of 75%
6	U OFFSET		220 nF (low-leakage) connected to ground see also pin 12
7	R	see pin 1	RED input; connected via 47 nF capacitor 0.7 V (p-p) for EBU bar of 75%
8	V_{CC}		supply voltage 5 V nominal
9	G	see pin 1	GREEN input; connected via 47 nF capacitor 0.7 V (p-p) for EBU bar of 75%
10	V_{SS}		ground
11	B	see pin 1	BLUE input; connected via 47 nF capacitor 0.7 V (p-p) for EBU bar of 75%

PIN	NAME	CIRCUIT	DESCRIPTION
12	V OFFSET	see pin 6	220 nF (low-leakage) connected to ground
13	V_{REF}		2.5 V reference voltage decoupling with 47 µF and 22 nF capacitors
14	CHROMA		chrominance output; together with pin 19 the Y + C (SVHS) output
15	FLT		filter control pin 220 nF capacitor to ground

PIN	NAME	CIRCUIT	DESCRIPTION
16	CVBS		CVBS output
17	PAL/NTSC Y/Y + SYNC		4-level control pin Pin 5: 0 V PAL, Y 1.8 V PAL Y + SYNC 3.2 V NTSC Y + SYNC 5 V NTSC Y
18	NOTCH		pin for external notch filter

PIN	NAME	CIRCUIT	DESCRIPTION
19	Y + SYNC OUT		output of the Y + SYNC signal; together with pin 14 the Y + C (SVHS) output
20	Y + SYNC IN		input of the delayed Y + SYNC signal of the delay line black level must be 2.5 V
21	BURST ADJ		external resistor to ground for adjusting the position of the burst

PIN	NAME	CIRCUIT	DESCRIPTION
22	Y + SYNC OUT		output of the Y + SYNC signal, connected to the delay line via a resistor
23	OSC		subcarrier-crystal in series with a trimmer, or an external subcarrier signal, via 1 nF in series with a resistor
24	CS		composite SYNC signal input amplitude < 600 mV (p-p)

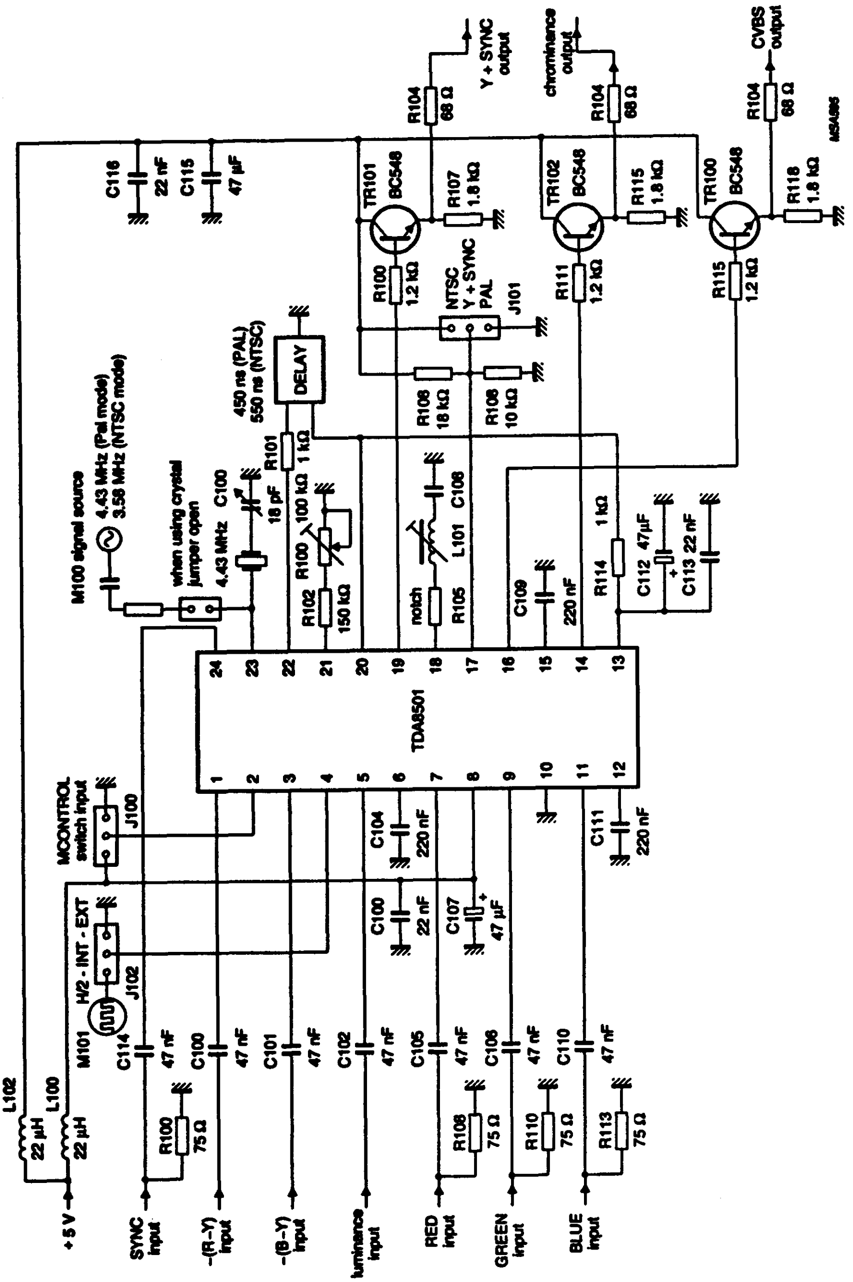


Fig.14 Application diagram.

4 × 4 video switch matrix

TDA8540

FEATURES

- I^2C-bus or the non-I^2C-bus mode (controlled by DC voltages)
- Slave receiver in the I^2C mode
- S-VHS or CVBS processing
- 3-state switches for all channels
- Selectable gain for the video channels
- sub-address facility
- Auxiliary logic outputs for audio switching
- System expansion possible up to 7 devices (28 sources)
- Static short-circuit proof outputs
- ESD protection.

APPLICATIONS

- CTV receivers
- Peritelevision sets
- Satellite receivers.

GENERAL DESCRIPTION

The TDA8540 has been designed primarily for switching between composite video signals. Consequently, a minimum of four input lines has been provided as required for switching between two S-VHS sources. Each of the four outputs can be set to a high impedance state, permitting parallel connection to several devices.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.2	–	8.8	V
I_{CC}	supply current		–	20	30	mA
I_{SO}	isolation "OFF" state	at f = 5 MHz	60	80	–	dB
B	3 dB bandwidth		12	–	–	MHz
α	crosstalk attenuation between channels		60	70	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8540	20	DIL	plastic	SOT146E
TDA8540T	20	SO	plastic	SOT163A

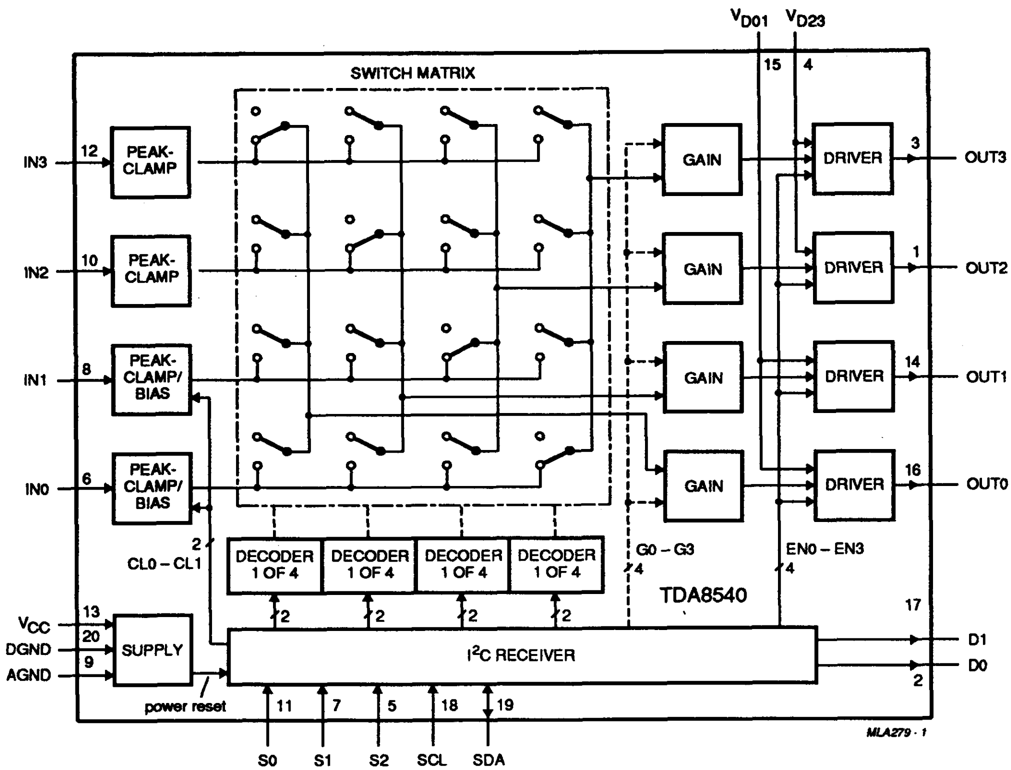


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUT2	1	video output 2
DO	2	control output
OUT3	3	video output 3
V_{D23}	4	driver supply
S2	5	sub-address input 2
IN0	6	video input (CVBS or chrominance signal)
S1	7	sub-address input 1
IN1	8	video input (CVBS or chrominance signal)
AGND	9	analog ground
IN2	10	video input (CVBS or luminance signal)
SO	11	sub-address input 0
IN3	12	video input (CVBS or luminance signal)
V_{CC}	13	positive supply voltage
OUT1	14	video output 1
V_{D01}	15	driver supply
OUT0	16	video output 0
D1	17	control output
SCL	18	serial clock input
SDA	19	serial data input/output
DGND	20	digital ground

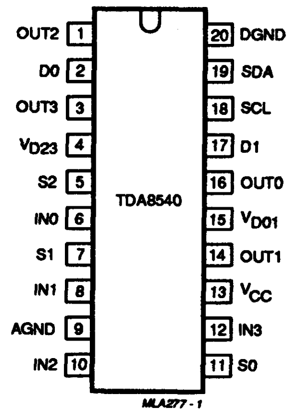


Fig.2 Pinning configuration.

FUNCTIONAL DESCRIPTION

The TDA8540 is controlled via a bi-directional I²C-bus. 3-bits of the I²C address can be selected via sub-address input pins, thus providing a facility for parallel operation of 7 devices.

Control options via the I²C-bus:

- the input signals can be clamped at their negative peak (top sync).
- the gain factor of the outputs can be selected between 1× or 2×.
- each of the four outputs can be individually connected to one of the four inputs.
- each output can be individually set in a high impedance state.
- two binary output data lines can be controlled for switching accompanying sound signals.

The SDA and SCL pins (pins 19 and 18) can be connected to the I²C-bus or to DC switching voltage sources. Address inputs S0 to S2 (pins 11, 7 and 5) are used to select sub-addresses for switching to the non-I²C mode. Inputs S0, S1 and S2 can be connected to the supply voltage (HIGH) or the ground (LOW). In this way no peripheral components are required for selection.

Table 1 I²C-bus sub-addressing.

S2	S1	S0	sub-address		
			A2	**A1**	**A0**
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I²C addressable		

I²C-bus control

After power-up the outputs are initialized in the high impedance state, and D0, D1 are at a low level.

Detailed information on I²C-bus is available on request.

The TDA8540 is a SLAVE RECEIVER with the following protocol:

S	SLV	A	SUB	A	DATA	A	DATA	A	P

Where:

- S : start condition
- A : acknowledge bit (generated by TDA8540)
- P : stop condition.

Data transmission to the TDA8540 begins with the following slave address (SLV):

	MSB							**LSB**	
SLV:	A6	A5	A4	A3	A2	A1	A0	R/W	

Where:

A6 = 1, A5 = 0, A4 = 0, A3 = 1

A2, A1, A0 : pin programmable address bits

R/W = 0 (write only)

Where:

if SUB = 00H : access to switch control (SW1)

if SUB = 01H : access to gain/clamp/data control (GCO)

if SUB = 02H : access to output enable control (OEN)

After the slave address, a second byte, SUB, is required for selecting the functions:

	MSB							**LSB**	
SUB:	0	0	0	0	0	0	RS1	RS0	

Note

If more than one data byte is sent, the SUB byte will be automatically incremented

If more than 3 data bytes are sent, the internal counter will roll over and the device will then rewrite the first register.

DATA BYTES

- SWI (SUB = 00H)

SWI (SUB = 00H) determines which input is connected to the different outputs:

	MSB							LSB
SWI:	S31	S30	S21	S20	S11	S10	S01	S00

For J = 0 to 3:	S_j1, S_j0	00	01	10	11
	OUT_j	IN0	IN1	IN2	IN3

Example : if S21 = 0 and S20 = 1, then OUT2 is connected to IN1.

- GCO (SUB = 01H)
- selects the gain of each output
- selects the clamp action or mean value on inputs 0 and 1
- determines the value of the auxiliary outputs D1 and D0

	MSB							LSB
GCO:	G3	G2	G1	G0	CL1	CL0	D1	D0

- for j = 0 to 3 : if Gj = 0 (resp 1), then output j has a gain of 2 (resp 1)
- if CL0 (resp CL1) = 0, then input signal on IN0 (resp IN1) is clamped
- for j = 0.1 : if Dj = 0 (resp 1), then logical output j is LOW (resp HIGH).

OEN (SUB = 02H) determines which output is active or high impedance:

	MSB							LSB
OEN:	X	X	X	X	EN3	EN2	EN1	EN0

- for j = 0 to 3 : if ENj = 0 (resp 1), then OUT J is HIGHZ (resp ACTIVE).

After a power-on reset: the outputs are set to a high impedance state; the outputs are connected to IN0; the gains are set at two and inputs IN0 and IN1 are clamped.

After a power-on reset, the programming of the device is required by the outputs being in a high impedance state.

Non-I²C-bus Control

If the S0, S1 and S2 pins are all tied to V_{CC} the device will then enter the non-I²C mode.

- After a power-on reset :
  - gain is set at two for all outputs
  - all inputs are clamped
  - all outputs are active
  - the matrix position is given by SDA and SCL voltage level..

Table 2 Non I²C-bus Control.

SCL - SDA	0.0	0.1	1.0	1.1
OUT3	IN3	IN2	IN1	IN0
OUT2	IN2	IN3	IN0	IN1
OUT1	IN1	IN0	IN3	IN2
OUT0	IN0	IN1	IN2	IN3

SCL and SDA act as normal input pins:

- SCL interchanges (OUT3 and OUT2) with (OUT1 and OUT0).
- SDA interchanges OUT3 with OUT2; OUT1 with OUT0.

Note:

For use with chrominance signals, the clamp action must be overruled by external bias.

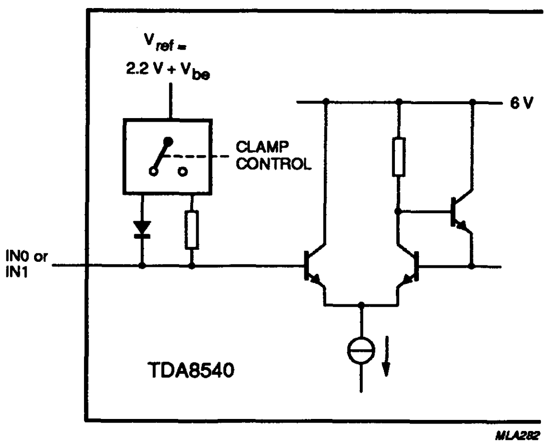


Fig.3 IN0 and IN1 inputs.

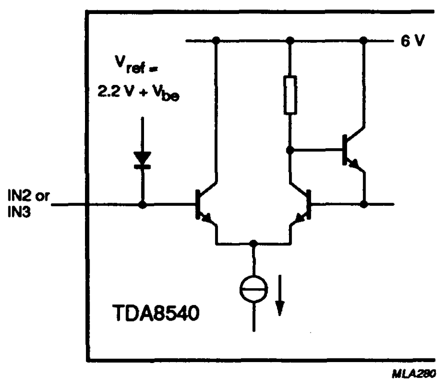


Fig.4 IN2 and IN3 inputs.

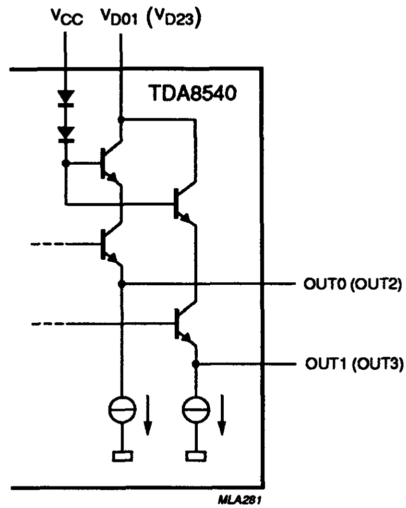


Fig.5 Driver output stage.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	9.1	V
P_{tot}	total power dissipation	–	750	mW
T_{stg}	storage temperature	–55	+125	°C
T_j	maximum junction temperature	–	+150	°C
V_{D01}, V_{D23}	driver supply input voltage	–0.3	13.8	V
IN0 to IN3	video input voltage	–0.3	7.2	V
OUT0 to OUT3	video output voltage	–0.3	7.2	V
D0, D1	control output voltage	–0.3	7.2	V
SDA, SDL	I^2C input/output voltage	–0.3	8.8	V
S0 to S2	sub-address input voltage	–0.3	8.8	V

Handling

HUMAN BODY MODEL

The IC withstands 1500 V in accordance with UZW-BO-FQ-A303.

MACHINE MODEL

The IC withstands 200 V in accordance with UZW-BO-FQ-B303 (stress reference pins : AGND - GNDD short-circuit and V_{CC}).

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT146	60 K/W
	SOT163A	85 K/W

OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.2	–	8.8	V
T_{amb}	operating ambient temperature		0	–	70	°C
Video inputs (pins 6, 8, 10 and 12)						
C_I	external capacitor		–	100	–	nF
V_I	C signal amplitude (peak-to-peak value)	note 1	–	–	1	V
V_I	CVBS or Y-signal amplitude (peak-to-peak value)	note 2	–	–	1.5	V
Video drivers (pins 4 and 15)						
R_D	external collector resistor	note 3	–	25	–	Ω
C_D	external decoupling capacitor	note 4	–	22	–	μF
sub-address S0, S1 and S2 (pins 5, 7 and 11)						
V_{IH}	HIGH level input voltage		4	–	V_{CC}	V
V_{IL}	LOW level input voltage		0	–	1	V

Notes to the Operating Characteristics:

1. Only for pins 6 and 8 when clamp action is not selected for these pins.
2. On all the video input pins when non-I²C-bus control mode is selected or when clamp action is selected on pins 6 and 8 (by I²C-bus control).
3. Connected between V_{CC} and pin 4 or pin 15.
4. Connected between AGRND and pin 4 or pin 15.

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; gain condition, clamp condition and OFF state are controlled by the I²C bus unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{CC}	supply current	without load	–	20	30	mA
		OFF state	–	12	–	mA
Video inputs : IN0 to IN3 when the clamp is active (see Figs 3 and 4)						
I_{LI}	input leakage current	V_I = 3 V	–	0.4	1	mA
V_{clamp}	input clamping voltage	I_I = 5 µA	–	2.2	–	V
I_{clamp}	nput clamping current	V_I = 0 V	1.2	–	–	mA
Video inputs : IN0 and IN2 when the clamp is not active (see Fig.3)						
V_{bias}	DC input bias level	I_I = 0	–	2.9	–	V
R_I	input resistance		–	10	–	kΩ
Video outputs : OUT0 to OUT3 (see Fig.5)						
Z_O	output impedance	OFF state	100	–	–	kΩ
R_O	output resistance		–	5	–	Ω
ISO	isolation	OFF state f = 5 MHz	60	–	–	dB
V_O	output top sync level (Y or CVBS)		0.4	0.7	1	V
V_{bias}	output mean value for chrominance signals	G = 2, load = 150 Ω	1.5	1.9	2.2	V
		G = 1, without load	1	1.3	1.6	V
G_v	voltage gain	G = 1; f = 1 MHz	−1	0	+1	dB
		G = 2 f = 1 MHz	+5	+6	+7	dB
G_{diff}	differential gain	note 1	–	0.5	3	%
φ_{diff}	differential phase	note 1	–	0.6	–	deg
NL	non linearity	note 2	–	0.5	2	%
α	crosstalk attenuation between channels	note 3	60	70	–	dB
SVRR	supply voltage rejection	note 4	36	55	–	dB
ΔG	maximum gain variation	100 kHz < f < 5 MHz	–	0.5	–	dB
		100 kHz < f < 8.5 MHz	–	1	–	dB
		100 kHz < f < 12 MHz	–	3	–	dB
αI²C	crosstalk attenuation of bus signals		60	–	–	dB
Auxiliary outputs D0, D1 (open collector)						
I_{OH}	HIGH level output current	V_{OH} = 5.5 V	–	–	10	mA
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	–	–	0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2C-bus inputs SCL, SDA						
I_{IH}	HIGH level input current	V_{IH} = 3.0 V	–	–	10	μA
I_{IL}	LOW level input current	V_{IL} = 1.5 V	–10	–	–	μA
C_I	input capacitance		–	–	10	pF
I^2C-bus output SDA						
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	–	–	0.4	V
sub-address S0, S1 and S2						
I_{IH}	HIGH level input current	$V_{IH} = V_{CC}$	–	–	10	μA
I_{IL}	LOW level input current	V_{IL} = 0 V	–	–	10	μA

Notes to the Characteristics:

1. Gain set at two, R_L = 150 Ω, test signal D2 from CCIR 330.
2. Gain set at two, R_L = 150 Ω, test signal D1 from CCIR 17.
3. Measured from any selected input to output; f = 5 MHz, R_L = 150 Ω, gain set at 2, V_I = 1.5 V (p-p). This measurement requires an optimized board.
4. Supply voltage ripple rejection: $20 \log \frac{V_{r(supply)}}{V_{r(output)}}$ measured at f = 1 kHz with $V_{r(supply\ max)}$ = 100 mV (p-p). The supply voltage rejection ratio is higher than 36 dB at f_{max} = 100 kHz.

4 × 4 video switch matrix TDA8540

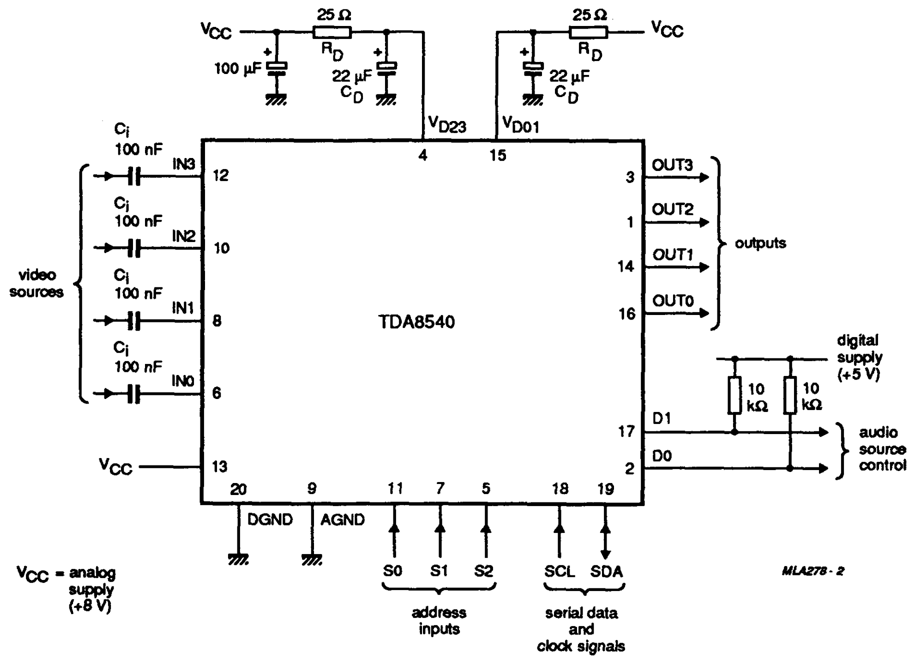


Fig.6 Application diagram.

8-bit video digital-to-analog converter | TDA8702

FEATURES

- 8-bit resolution
- Conversion rate up to 30 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High-speed digital-to-analog conversion
- Digital TV including:
  - field progressive scan
  - line progressive scan
- Subscriber TV decoders
- Satellite TV decoders
- Digital VCRs.

DESCRIPTION

The TDA8702 is an 8-bit digital-to-analog converter (DAC) for video and other applications. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 30 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	–	26	32	mA
I_{CCD}	digital supply current	note 1	–	23	30	mA
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltage (peak-to-peak value)	note 2				
		Z_L = 10 kΩ	−1.45	−1.60	−1.75	V
		Z_L = 75 kΩ	−0.72	−0.80	−0.88	V
ILE	DC integral linearity error		–	–	±1/2	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
f_{CLK}	maximum conversion rate		–	–	30	MHz
B	−3 dB analog bandwidth	f_{CLK} = 30 MHz; note 3	–	150	–	MHz
P_{tot}	total power dissipation		–	250	340	mW

Notes

1. D0 to D7 connected to V_{CCD} and CLK connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The −3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8702	16	DIL	plastic	SOT38
TDA8702T	16	SO16	plastic	SOT162A

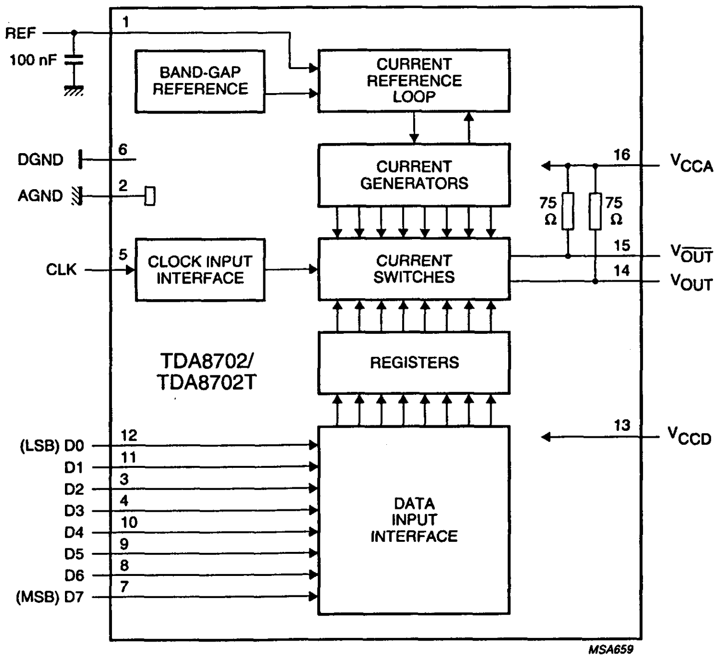


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input; bit 2
D3	4	data input; bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input; bit 7
D6	8	data input; bit 6
D5	9	data input; bit 5
D4	10	data input; bit 4
D1	11	data input; bit 1
D0	12	data input; bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$V_{\overline{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

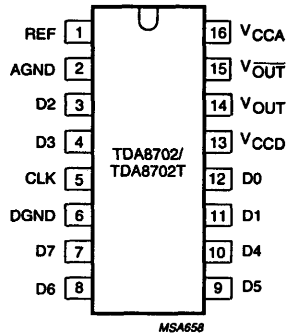


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differential	−0.5	+0.5	V
AGND − DGND	ground voltage differential	−0.1	+0.1	V
V_I	input voltage (pins 3 to 5 and 7 to 12)	−0.3	V_{CCD}	V
$I_{OUT}/\overline{I_{OUT}}$	total output current (pins 14 and 15)	−5	+26	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambienttemperature	0	+70	°C
T_j	junction temperature	−	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT38	70 K/W
	SOT162A	90 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_{16} - V_2 = 4.5$ V to 5.5 V; $V_{CCD} = V_{13} - V_6 = 4.5$ V to 5.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; V_{REF} decoupled to AGND by a 100 nF capacitor; T_{amb} = 0 °C to +70 °C; AGND and DGND shorted together; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = 5$ V and T_{amb} = 25 °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	–	26	32	mA
I_{CCD}	digital supply current	note 1	–	23	30	mA
AGND – DGND	ground voltage differential		−0.1	–	+0.1	V
Inputs						
DIGITAL INPUTS (D7 TO D0) AND CLOCK INPUT (CLK)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	–	−0.3	−0.4	mA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	0.01	20	µA
f_{CLK}	maximum clock frequency		–	–	30	MHz
Outputs (note 2; referenced to V_{CCA})						
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltages (peak-to-peak value)					
		Z_L = 10 kΩ	−1.45	−1.60	−1.75	V
		Z_L = 75 Ω	−0.72	−0.80	−0.88	V
V_{OS}	analog offset output voltage	code = 0	–	−3	−25	mV
V_{OUT}/TC	full-scale analog output voltage temperature coefficient		–	–	200	µV/K
V_{OS}/TC	analog offset output voltage temperature coefficient		–	–	20	µV/K
B	−3 dB analog bandwidth	note 3; f_{CLK} = 30 MHz	–	150	–	MHz
G_{diff}	differential gain		–	0.6	–	%
Φ_{diff}	differential phase		–	1	–	deg
Z_O	output impedance		–	75	–	Ω
Transfer function (f_{CLK} = 30 MHz)						
ILE	DC integral linearity error		–	–	±1/2	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB

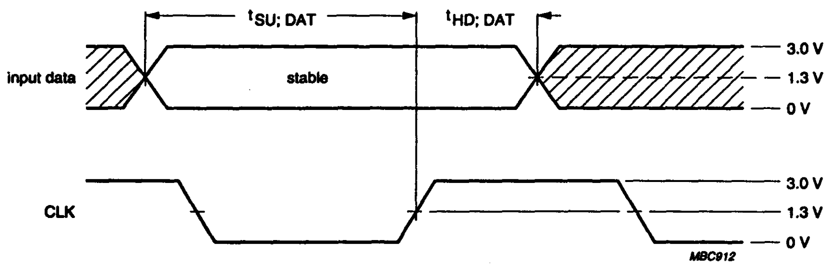
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics (f_{CLK} = 30 MHz; notes 4 and 5; see Figs 3, 4 and 5)						
$t_{SU;DAT}$	data set-up time		−0.3	–	–	ns
$t_{HD;DAT}$	data hold time		2.0	–	–	ns
t_{PD}	propagation delay time		–	–	1.0	ns
t_{S1}	settling time	10% to 90% full-scale change to ±1 LSB	–	1.1	1.5	ns
t_{S2}	settling time	10% to 90% full-scale change to ±1 LSB	–	6.5	8.0	ns
t_d	input to 50% output delay time		–	3.0	5.0	ns
Output transients (glitches; (f_{CLK} = 30 MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	–	–	30	LSB.ns

Notes

1. D0 to D7 are connected to V_{CCD}, CLK is connected to DGND.
2. The analog output voltages (V_{OUT} and $\overline{V_{OUT}}$ are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is 75 Ω (typ.).
3. The −3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).
4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $\overline{V_{OUT}}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data is latched at the rising edge of the clock. The output voltage remains stable (independent of input data variations) during the HIGH level of the clock (CLK = HIGH). During a LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages (see Fig.5).
5. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising edge of the clock and still be recognized. The data hold time ($t_{HD;DAT}$) is the minimum period following the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising edge of the clock and still be recognized.
6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 to 128 and on the falling edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of the offset voltage).

CODE	INPUT DATA (D7 to D0)	DAC OUTPUT VOLTAGES			
		Z_L = 10 kΩ		Z_L = 75 Ω	
		V_{OUT}	$\overline{V_{OUT}}$	V_{OUT}	$\overline{V_{OUT}}$
0	000 00 00	0	−1.6	0	−0.8
1	000 000 01	−0.006	−1.594	−0.003	−0.797
.	....				
128	100 000 00	−0.8	−0.8	−0.4	−0.4
.	....				
254	111 111 10	−1.594	−0.006	−0.797	−0.003
255	111 111 11	−1.6	0	−0.8	0



The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns after the first rising edge of the clock ($t_{SU;DAT}$ is negative; −0.3 ns). Data must be held at least 2 ns after the rising edge ($t_{HD;DAT}$ = +2 ns).

Fig.3 Data set-up and hold times.

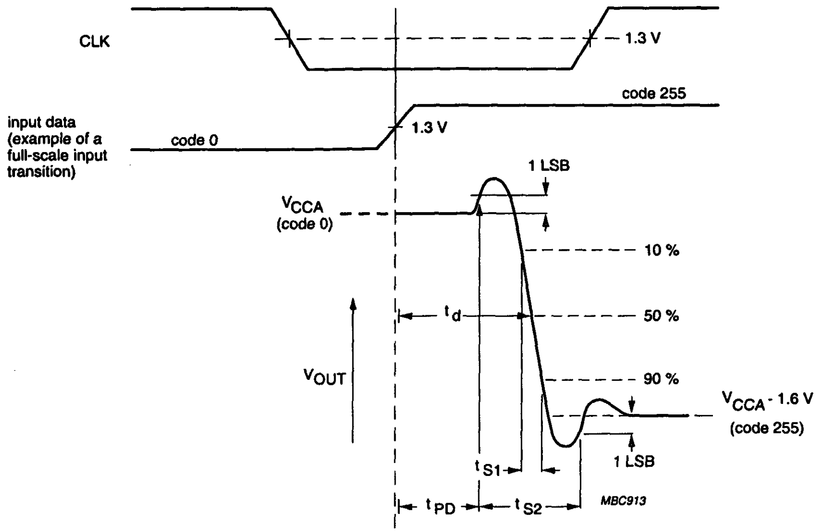
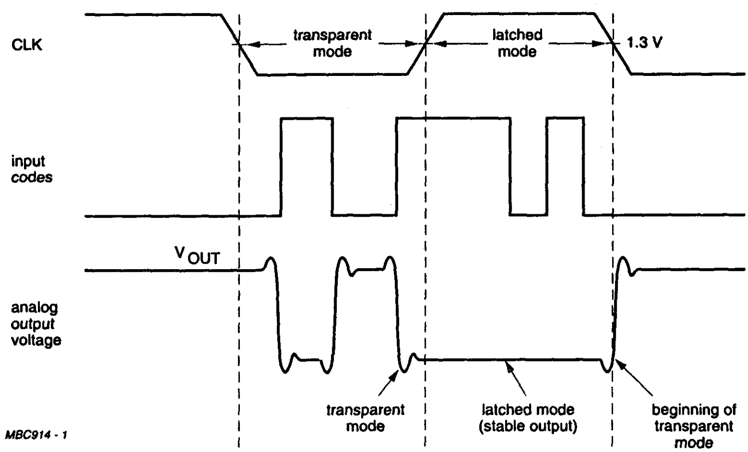
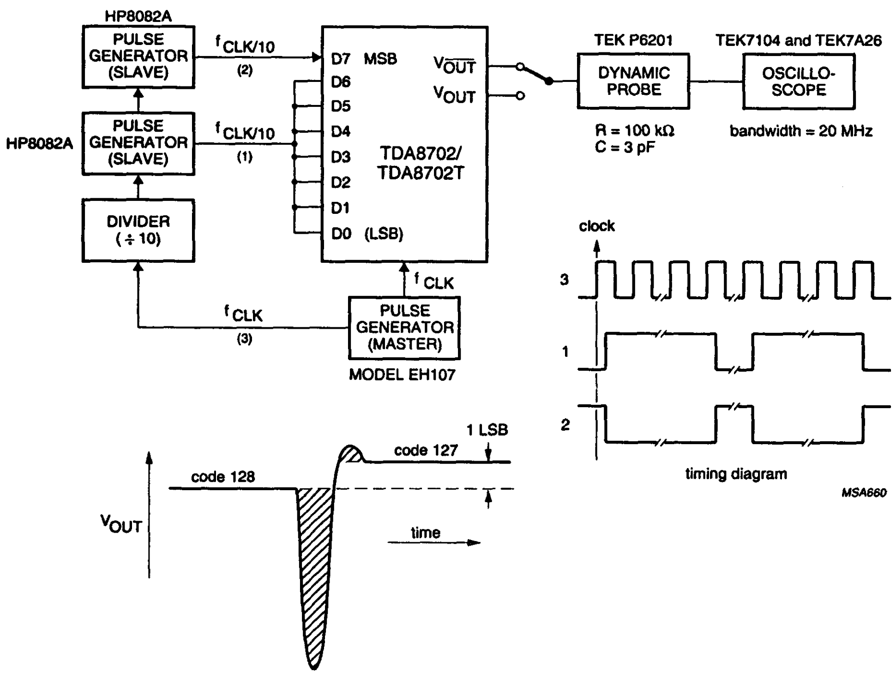


Fig.4 Switching characteristics.



During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable regardless of any change at the input. A change of input data during the latched mode will be seen on the falling edge of the clock (beginning of the transparent mode).

Fig.5 Latched and transparent mode.



The value of the glitch energy is the sum of the shaded area measured in LSB.ns.

Fig.6 Glitch energy measurement.

INTERNAL PIN CONFIGURATIONS

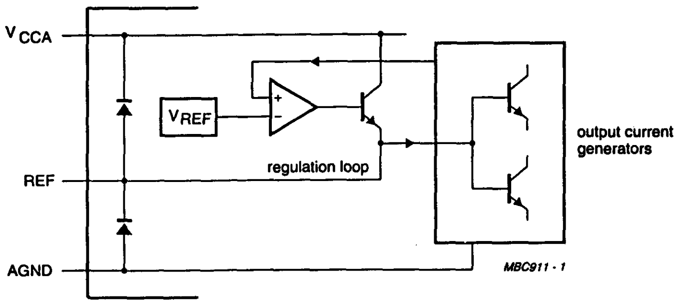


Fig.7 Reference voltage generator decoupling.

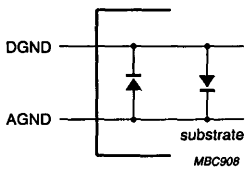


Fig.8 AGND and DGND.

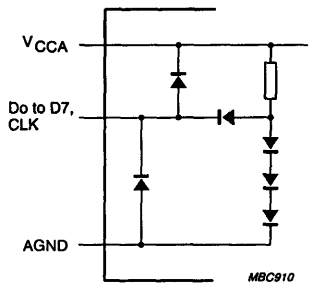


Fig.9 D7 to D0 and CLK.

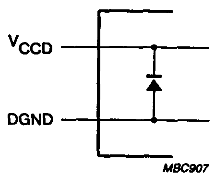


Fig.10 Digital supply.

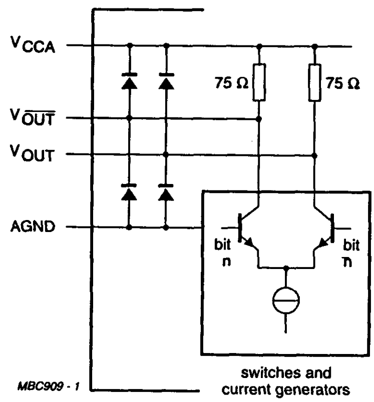


Fig.11 Analog outputs.

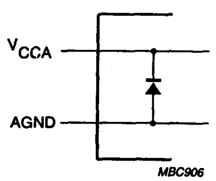
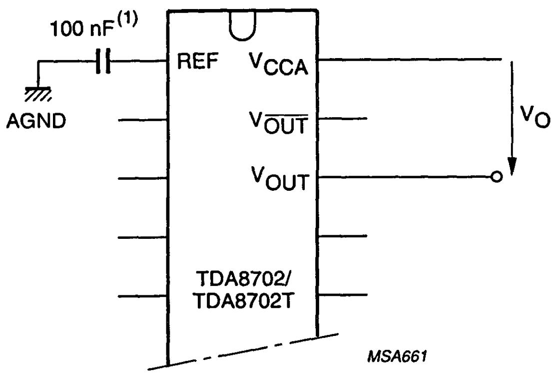


Fig.12 Analog supply.

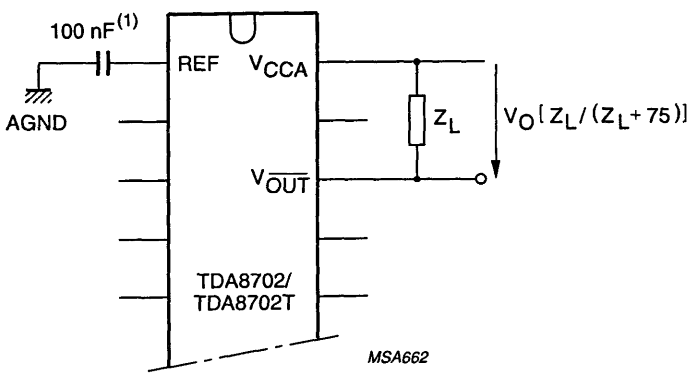
APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).



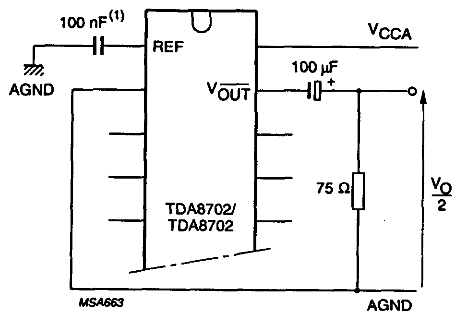
(1) This is a recommended value for decoupling pin 1.

Fig.13 Analog output voltage without external load ($V_O = -V_{\overline{OUT}}$; see Table 1, Z_L = 10 kΩ).



(1) This is a recommended value for decoupling pin 1.

Fig.14 Analog output voltage with external load (external load Z_L = 75 Ω to ∞).



(1) This is a recommended value for decoupling pin 1.

Fig.15 Analog output with AGND as reference.

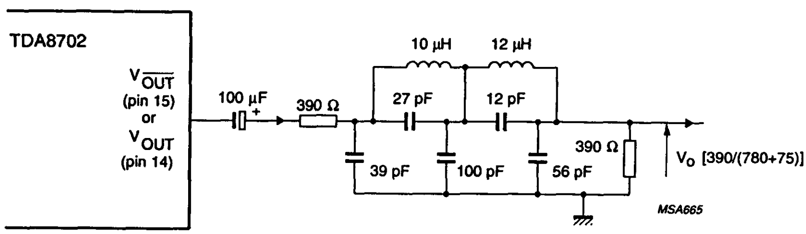
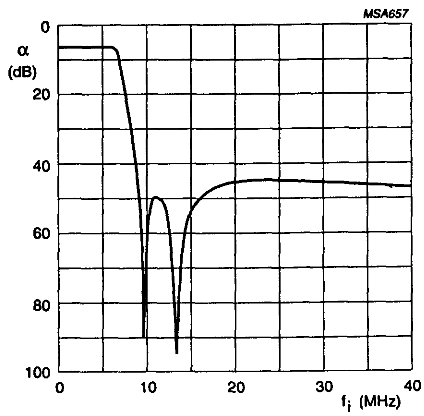


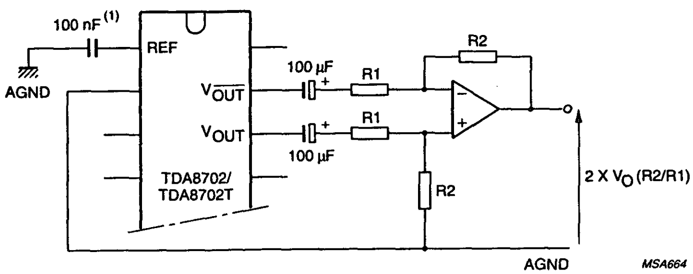
Fig.16 Example of anti-aliasing filter (analog output referenced to AGND).



Characteristics

- Order 5; adapted CHEBYSHEV
- Ripple at ≤ 0.1 dB
- $f_{(-3\ dB)}$ = 6.7 MHz
- $f_{(NOTCH)}$ = 9.7 MHz and 13.3 MHz

Fig.17 Frequency response for filter shown in Fig.16.



(1) This is a recommended value for decoupling pin 1.

Fig.18 Differential mode (improved supply voltage ripple rejection).

8-bit high-speed analog-to-digital converter

TDA8703

FEATURES

- 8-bit resolution
- Sampling rate up to 40 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.1 effective bits at 4.43 MHz full-scale input)
- Binary or two's complement 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Internal reference voltage generator
- Power dissipation only 290 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

- General purpose high-speed analog-to-digital conversion
- Digital TV, IDTV
- Subscriber TV decoder
- Satellite TV decoders
- Digital VCR.

GENERAL DESCRIPTION

The TDA8703 is an 8-bit high-speed analog-to-digital converter (ADC) for video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are TTL compatible, although a low-level AC clock input signal is allowed.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8703	24	DIL	plastic	SOT101
TDA8703T	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	28	36	mA
I_{CCD}	digital supply current		–	19	25	mA
I_{CCO}	output stages supply current		–	11	14	mA
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
AILE	AC integral linearity error	note 1	–	–	±2	LSB
B	–3 dB bandwidth	note 2; f_{CLK} = 40 MHz	–	19.5	–	MHz
$f_{CLK}/f_{\overline{CLK}}$	maximum conversion rate	note 3	40	–	–	MHz
P_{tot}	total power dissipation		–	290	415	mW

Notes

1. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}; $f_{\overline{CLK}}$ = 27 MHz).
2. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at input).
3. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.
   - If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

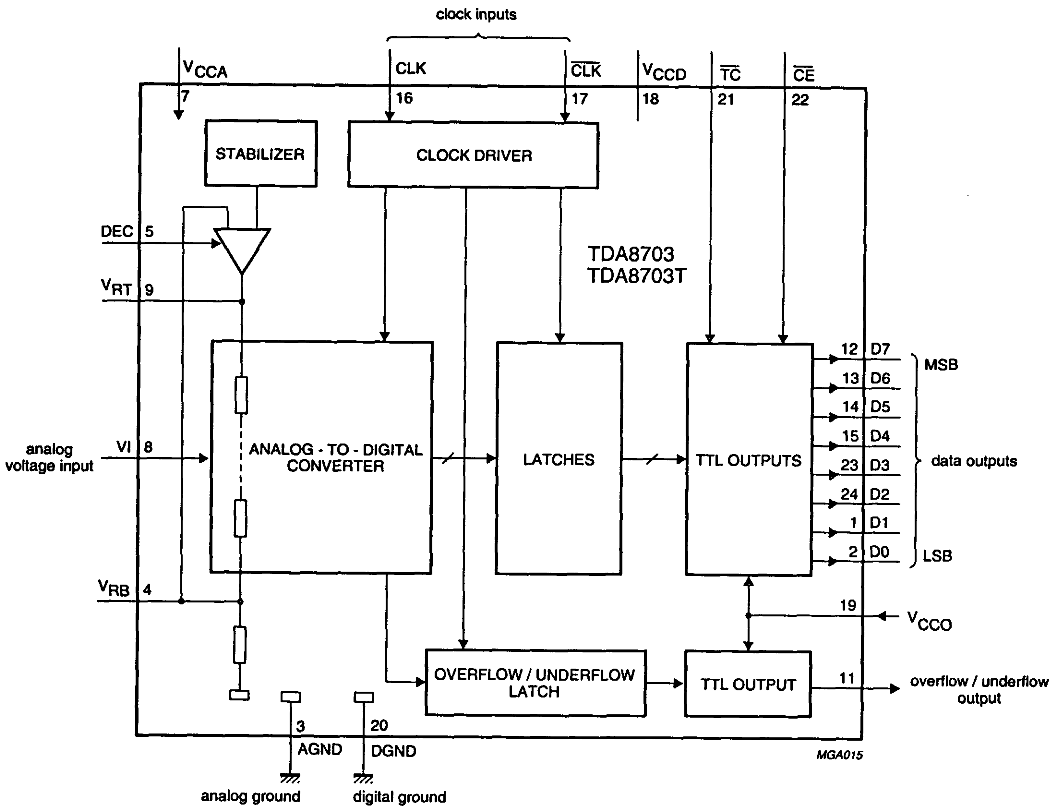


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output; bit 1
D0	2	data output; bit 0 (LSB)
AGND	3	analog ground
V_{RB}	4	reference voltage bottom (decoupling)
DEC	5	decoupling input (internal stabilization loop decoupling)
n.c.	6	not connected
V_{CCA}	7	positive supply voltage for analog circuits (+5 V)
VI	8	analog voltage input
V_{RT}	9	reference voltage top (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output; bit 7 (MSB)
D6	13	data output; bit 6
D5	14	data output; bit 5
D4	15	data output; bit 4
CLK	16	clock input
$\overline{CLK}$	17	complementary clock input
V_{CCD}	18	positive supply voltage for digital circuits (+5 V)
V_{CCO}	19	positive supply voltage for output stages (+5 V)
DGND	20	digital ground
$\overline{TC}$	21	input for two's complement output (TTL level input, active LOW)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output; bit 3
D2	24	data output; bit 2

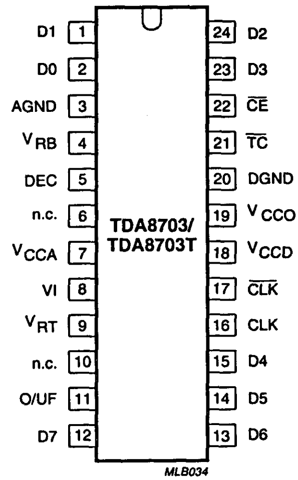


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		−0.3	7.0	V
V_{CCD}	digital supply voltage		−0.3	7.0	V
V_{CCO}	output stages supply voltage		−0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage differences		−1.0	1.0	V
V_{VI}	input voltage range	referenced to AGND	−0.3	7.0	V
$V_{CLK}/V_{\overline{CLK}}$	AC input voltage for switching (peak-to-peak value)	note 1; referenced to DGND	−	2.0	V
I_O	output current		−	+10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+125	°C

Note

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition. If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT101	55 K/W
	SOT137A	75 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7 - V_3 = 4.5$ V to 5.5 V; $V_{CCD} = V_{18} - V_{20} = 4.5$ V to 5.5 V; $V_{CCO} = V_{19} - V_{20} = 4.5$ V to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; T_{amb} = 0 °C to +70 °C; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V and T_{amb} = 25 °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	28	36	mA
I_{CCD}	digital supply current		–	19	25	mA
I_{CCO}	output stage supply current	all outputs LOW	–	11	14	mA
Inputs						
Clock input $\overline{CLK}$ and CLK (note 1; referenced to DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V	−400	–	–	μA
I_{IH}	HIGH level input current	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V	–	–	100	μA
		$V_{CLK}/V_{\overline{CLK}} = V_{CCD}$	–	–	300	μA
Z_i	input impedance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	–	4	–	kΩ
C_i	input capacitance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	–	4.5	–	pF
$V_{CLK} - V_{\overline{CLK}}$	AC input voltage for switching (peak-to-peak value)	note 1; DC level = 1.5 V	0.5	–	2.0	V
$\overline{TC}$ and $\overline{CE}$ (referenced to DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{IL} = 0.4$ V	−400	–	–	μA
I_{IH}	HIGH level input current	$V_{IH} = 2.7$ V	–	–	20	μA
VI (analog input voltage referenced to AGND)						
$V_{VI(B)}$	input voltage (bottom)		1.33	1.41	1.48	V
$V_{VI(0)}$	input voltage	output code = 0	1.455	1.55	1.635	V
$V_{OS(B)}$	offset voltage (bottom)	$V_{VI(0)} - V_{VI(B)}$	0.125	–	0.155	V
$V_{VI(T)}$	input voltage (top)		3.2	3.36	3.5	V
$V_{VI(255)}$	input voltage	output code = 255	3.115	3.26	3.385	V
$V_{OS(T)}$	offset voltage (top)	$V_{VI(T)} - V_{VI(255)}$	0.085	–	0.115	V
$V_{VI(p-p)}$	input voltage amplitude (peak-to-peak value)		1.66	1.71	1.75	V
I_{IL}	LOW level input current	$V_{VI} = 1.4$ V	–	0	–	μA
I_{IH}	HIGH level input current	$V_{VI} = 3.6$ V	60	120	180	μA
Z_i	input impedance	$f_i = 1$ MHz	–	10	–	kΩ
C_i	input capacitance	$f_i = 1$ MHz	–	14	–	pF

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference resistance						
R_{ref}	reference resistance	V_{RT} to V_{RB}	–	220	–	Ω
Outputs						
Digital outputs (D7 - D0) (referenced to DGND)						
V_{OL}	LOW level output voltage	$I_O = 1$ mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	$I_O = -0.4$ mA	2.7	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	$0.4\ V < V_O < V_{CCD}$	–20	–	+20	μA
Switching characteristics (note 2; see Fig.3)						
$f_{CLK}/f_{\overline{CLK}}$	maximum clock frequency		40	–	–	MHz
Analog signal processing (f_{CLK} = 40 MHz)						
B	–3 dB bandwidth	note 3	–	19.5	–	MHz
G_d	differential gain	note 4	–	0.6	–	%
ϕ_d	differential phase	note 4	–	0.8	–	deg
f_1	fundamental harmonics (full-scale)	$f_i = 4.43$ MHz	–	–	0	dB
f_{all}	harmonics (full-scale), all components	$f_i = 4.43$ MHz	–	–55	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	–28	–25	dB
SVRR2	supply voltage ripple rejection	note 5	–	1	2.5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
AILE	AC integral linearity error	note 6	–	–	±2	LSB
EB	effective bits	$f_i = 4.43$ MHz	–	7.1	–	bits
Timing (note 7; see Figs 3 to 6; f_{CLK} = 40 MHz)						
t_{ds}	sampling delay		–	–	2	ns
t_{HD}	output hold time		6	–	–	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	–	8	10	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	–	16	20	ns
t_{dZH}	3-state output delay times	enable-to-HIGH	–	19	25	ns
t_{dZL}	3-state output delay times	enable-to-LOW	–	16	20	ns
t_{dHZ}	3-state output delay times	disable-to-HIGH	–	14	20	ns
t_{dLZ}	3-state output delay times	disable-to-LOW	–	9	12	ns

Notes

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

   If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.
2. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 2 ns.
3. The −3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
4. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
5. Supply voltage ripple rejection:
   - SVRR1; variation of the input voltage producing output code 127 for supply voltage variation of 1 V:

     SVRR1 = 20 log $(\Delta V_{VI(127)} / \Delta V_{CCA})$
   - SVRR2; relative variation of the full-scale range of analog input for a supply voltage variation of 1 V:

     SVR2 = $\{\Delta(V_{VI(0)} - V_{VI(255)}) / (V_{VI(0)} - V_{VI(255)})\} + \Delta V_{CCA}$.
6. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}; $f_{\overline{CLK}}$ = 27 MHz).
7. Output data acquisition:
   - Output data is available after the maximum delay of t_{dHL} and t_{dLH}.

Table 1 Output coding and input voltage (referenced to AGND; typical values).

			BINARY OUTPUT BITS								TWO's COMPLEMENT OUTPUT BITS							
STEP	$V_{VI(p-p)}$	O/UF	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow	< 1.55	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1.55	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
254	•	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	3.26	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow	> 3.26	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

Table 2 Mode selection.

$\overline{TC}$	$\overline{CE}$	D7 - D0	O/UF
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

Where: X = don't care

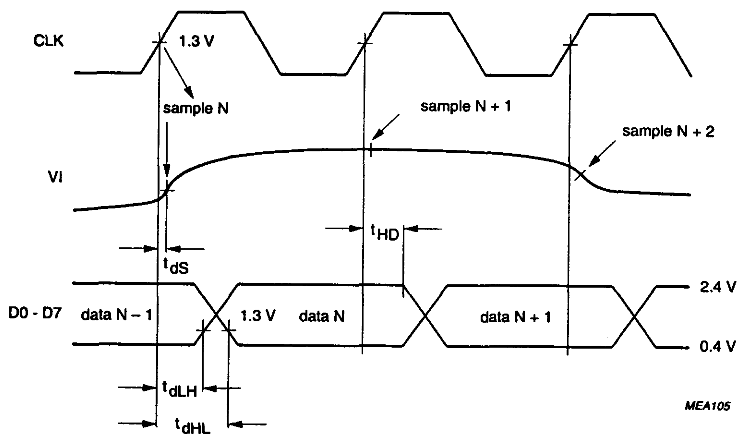


Fig.3 Timing diagram.

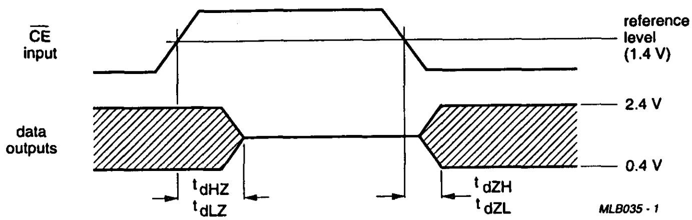


Fig.4 3-state delay timing diagram.

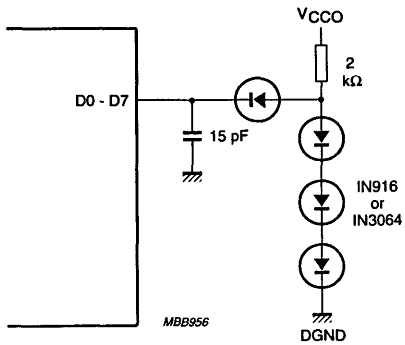


Fig.5 Load circuit for timing measurement; data outputs ($\overline{CE}$ = LOW).

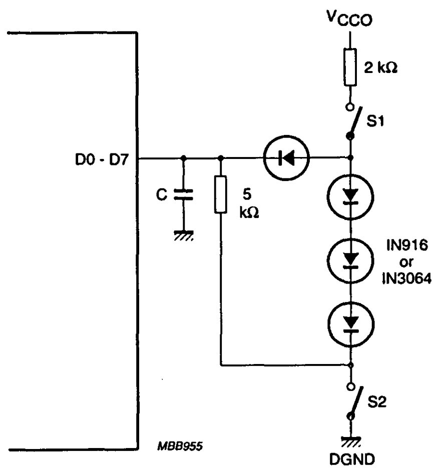


Fig.6 Load circuit for timing measurement; 3-state outputs ($\overline{CE}$: f_i = 1 MHz; V_{VI} = 3 V); see Table 3.

Table 3 Timing measurement for load circuit.

TIMING MEASUREMENT	SWITCH S1	SWITCH S2	CAPACITOR
t_{dZH}	open	closed	15 pF
t_{dZL}	closed	open	15 pF
t_{dHZ}	closed	closed	5 pF
t_{dLZ}	closed	closed	5 pF

INTERNAL PIN CONFIGURATIONS

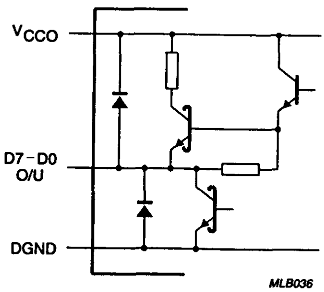


Fig.7 TTL data and overflow/underflow outputs.

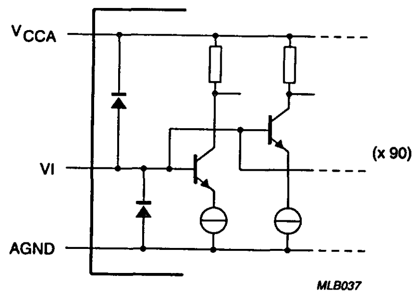


Fig.8 Analog inputs.

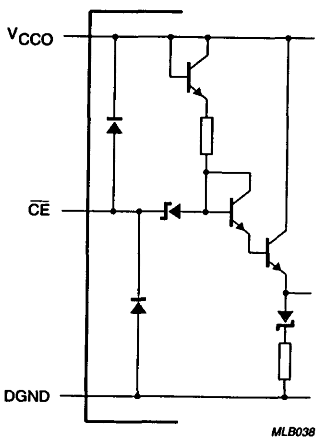


Fig.9 $\overline{CE}$ (3-state) input.

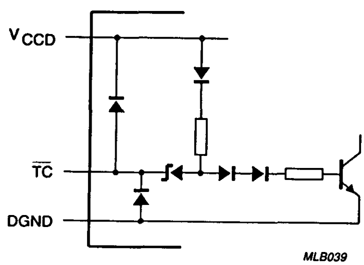


Fig.10 $\overline{TC}$ (two's complement) input.

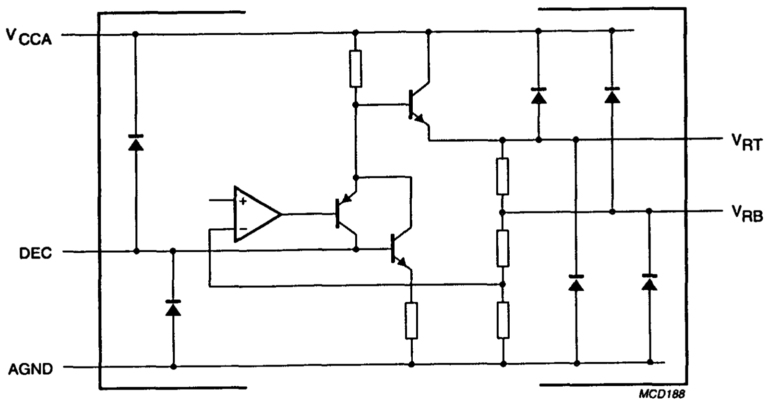


Fig.11 V_{RB}, V_{RT} and DEC.

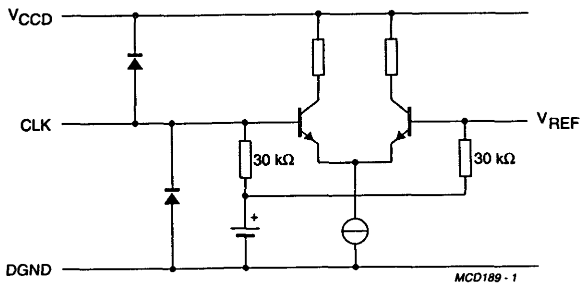


Fig.12 CLK and $\overline{CLK}$ inputs.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

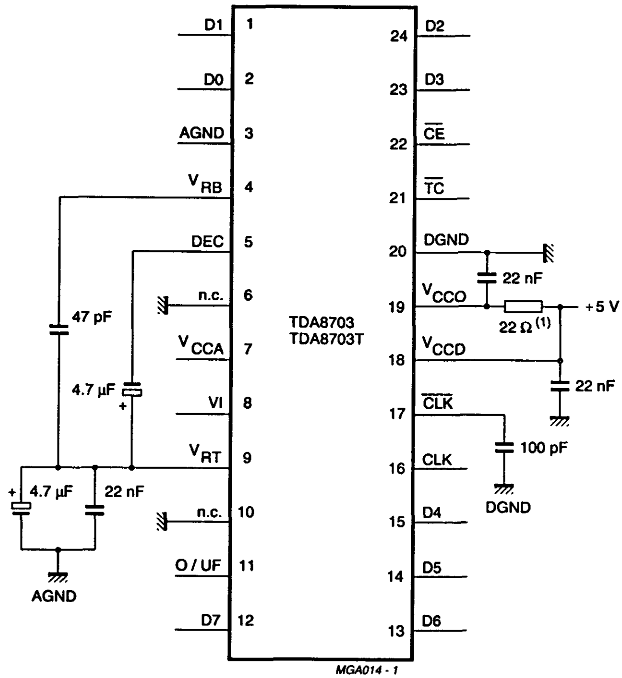


Fig.13 Application diagram.

Notes to Fig.13

1. It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of the TDA8703 interfaces with a capacitive CMOS load device.
2. CLK should be decoupled to the DGND with a 100 nF capacitor, if a TTL signal is used on CLK (see 'Notes to the characteristics', note 1).
3. CLK and $\overline{CLK}$ can be used in a differential mode (see 'Notes to the characteristics', note 1).
4. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder; do not draw current from these pins in order to achieve good linearity.
5. If it is required to use the TDA8703 in a parallel system configuration, the references (V_{RB} and V_{RT}) of each TDA87803 can be connected together. Code 0 will be identical and code 255 will remain in the 1LSB variation for each TDA8703.
6. Analog and digital supplies should be separated and decoupled.
7. Pins 6 and 10 should be connected to AGND in order to prevent noise influence.

6-bit analog-to-digital converter with multiplexer and clamp

TDA8706

FEATURES

- 6-bit resolution
- Binary 3-state TTL outputs
- TTL compatible digital inputs
- 3 multiplexed video inputs
- Luminance and colour difference clamps
- Internal reference
- 300 mW power dissipation
- 20-pin plastic package

APPLICATIONS

- General purpose video applications
- Y, U and V signals
- Colour Picture-in-Picture (PIPCO) for TV
- Videophone
- Frame grabber

GENERAL DESCRIPTION

The TDA8706 is a monolithic bipolar 6-bit analog-to-digital converter (ADC) with a 3 analog input multiplexer and a clamp. All digital inputs and outputs are TTL compatible. Regulator with good temperature compensation.

FUNCTIONAL DESCRIPTION

The TDA8706 is a "like-flash" converter which produces an output code in one clock period. The device can withstand a duty clock cycle of 50 to 66.6% (clock HIGH). Luminance clamping level is fitted with 00 hex. code (output 000000). Chrominance clamping level is fitted with 20 Hex. code (output 100000).

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage (pin 2)		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage (pin 10)		4.5	5.0	5.5	V
I_{CCA}	analog supply current (pin 20)		–	32	39	mA
I_{CCD}	digital supply current (pin 10)		–	28	37	mA
ILE	integral linearity error		–	–	±0.75	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
f_{CLK}	maximum clock frequency		20	–	–	MHz
P_{tot}	total power dissipation		–	300	418	mW
T_{amb}	operating ambient temperature range		0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8706	20	DIL	plastic	SOT146EF4
TDA8706T	20	SO20L	plastic	SOT163AG7

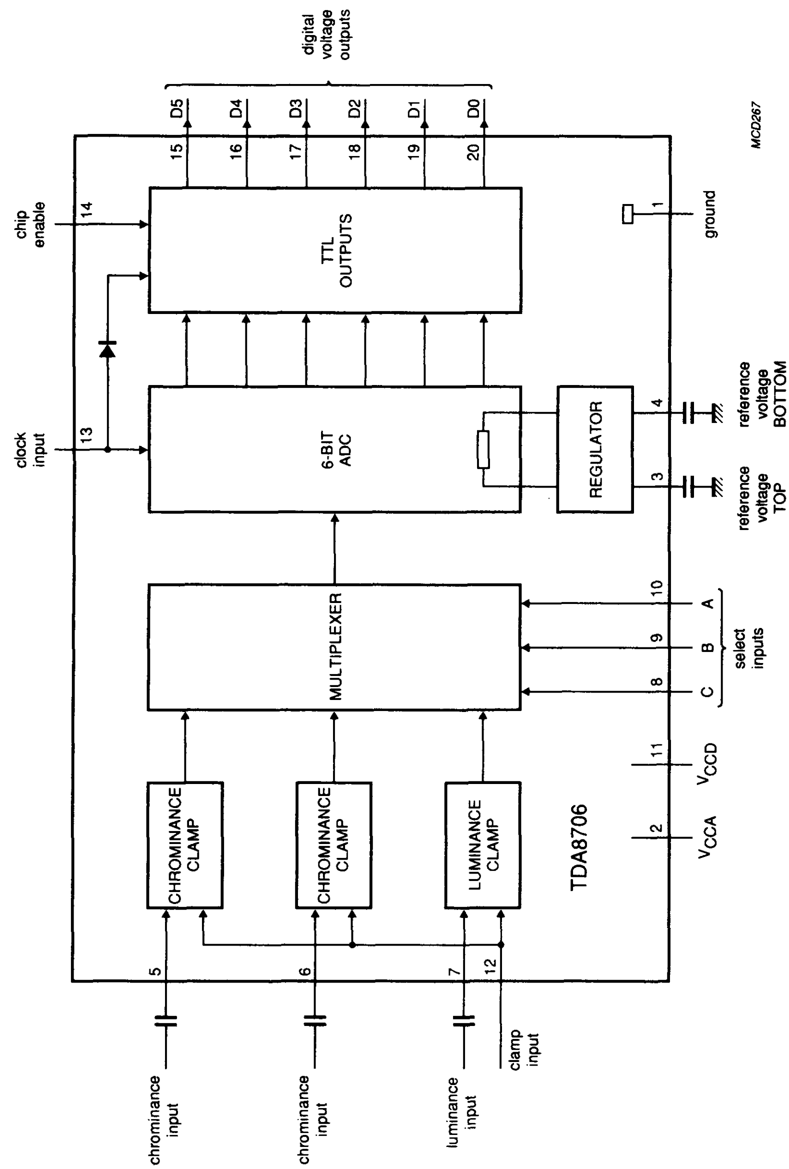


Fig.1 Block diagram.

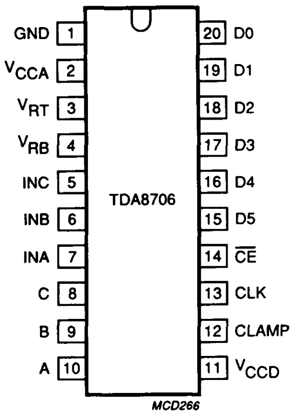


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground
V_{CCA}	2	analog positive supply (+5 V)
V_{RT}	3	reference voltage TOP decoupling
V_{RB}	4	reference voltage BOTTOM decoupling
INC	5	chrominance input
INB	6	chrominance input
INA	7	luminance input
C	8	select input
B	9	select input
A	10	select input
V_{CCD}	11	digital positive supply voltage (+5 V)
CLAMP	12	clamp pulse input (positive pulse)
CLK	13	clock input
$\overline{CE}$	14	chip enable (active LOW)
D5	15	digital voltage output: most significant bit (MSB)
D4	16	digital voltage output
D3	17	digital voltage output
D2	18	digital voltage output
D1	19	digital voltage output
D0	20	digital voltage input: least significant bit (LSB)

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range (pin 2)	−0.3	7.0	V
V_{CCD}	digital supply voltage range (pin 10)	−0.3	7.0	V
V_{CCA}-V_{CCD}	supply voltage difference	1.0	–	V
V_I	input voltage range	−0.3	7.0	V
I_O	output current	–	10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C

CHARACTERISTICS (see Tables 1 and 2)

V_{CCA} = 4.5 V to 5.5 V; V_{CCD} = 4.5 V to 5.5 V = V_{CCD}; T_{amb} = 0 °C to +70°C; C_{VRB} = C_{VR1} = 100 nF; Typical values measured at V_{CCA} = V_{CCD} = 5 V and T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage (pin 2)		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage (pin 10)		4.5	5.0	5.5	V
I_{CCA}	analog supply current (pin 2)		–	32	39	mA
I_{CCD}	digital supply current (pin 10)	all outputs at LOW level	–	28	37	mA
Inputs						
CLOCK INPUT (PIN 13)						
V_{IL}	LOW level input voltage		0	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	µA
Z_I	input impedance	f_{CLK} = 20 MHz	–	4	–	kΩ
C_i	input capacitance	f_{CLK} = 20 MHz	–	2	–	pF
A, B, C, CLAMP AND CEN INPUTS (PINS 8, 9, 10, 12 AND 14)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	20	µA
Reference voltage (pins 3 and 4)						
V_{RT}	reference voltage TOP decoupling		3.22	3.35	3.44	V
V_{RB}	reference voltage BOTTOM decoupling		1.84	1.9	1.96	V
$V_{RT} - V_{RB}$	reference voltage TOP – BOTTOM decoupling		1.36	1.435	1.48	V
Analog inputs INA, INB, INC (pins 7, 6 and 5)						
$V_{I(p-p)}$	input voltage amplitude (peak-to-peak value)		840	900	940	mV
Z_I	input impedance	f_i = 4.43 MHz	100	–	–	kΩ
C_{clamp}	coupling clamp capacitance		1	10	1000	nF
Analog signal processing (pins 5, 6 and 7) (f_{CLK} = 20 MHz)						
f_1	fundamental harmonics (full scale)	f_i = 4.43 MHz	–	–	0	dB
f_{all}	harmonics (full scale); all components	f_i = 4.43 MHz	-	–45	-	dB
G_{diff}	differential gain	note 1	–	0.4	–	%
ϕ_{diff}	differential phase	note 1	–	1.0	–	deg
SVRR	supply voltage ripple rejection	note 2	–	–30	–	dB
Outputs						
DIGITAL VOLTAGE OUTPUTS (PINS 15 TO 20) (SEE TABLE 2)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH level ouptut voltage	$I_O = 0.5$ mA	2.7	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	$0.4\ V < V_O < V_{CCD}$	–20	–	20	μA
Switching characteristics						
CLOCK TIMING (SEE FIG.3)						
f_{CLK}	maximum clock frequency		20	–	–	MHz
f_{mux}	maximum multiplexing frequency		10	–	–	MHz
t_{CLK}	period		50	–	–	ns
	duty cycle	CLK = V_{IH}	45	50	66.6	%
t_{LOW}	LOW time	at 50%	16	–	–	ns
t_{HIGH}	HIGH time	at 50%	22.5	–	–	ns
t_{CLR}	rise time	at 10% to 90%	4	6	–	ns
t_{CLF}	fall time	at 90% to 10%	4	6	–	ns
Select signals, Clamp, Data (see Figs 4 and 5)						
t_S	set-up time select A, B and C		35	–	–	ns
t_r	rise time (A, B and C)	at 10% to 90%	4	6	–	ns
t_f	fall time (A, B and C)	at 90% to 10%	4	6	–	ns
t_{CLPS}	set-up time clamp asynchronous		0	–	–	
t_{CLPH}	hold time clamp asynchronous		0	–	–	
t_{CLPP}	clamp pulse	$C_{CLP} = 10$ nF	–	3	–	μs
t_d	data output delay time		–	15	24	ns
t_{DH}	data hold time		12	–	–	ns
Transfer function						
ILE	DC integral linearity error		–	–	±0.75	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
AILE	AC integral linearity error	note 3	–	–	±2	LSB
EB	effective bits	note 3	–	5.7	–	bits
Timing						
DIGITAL OUTPUTS						
T_d	3-state delay time	see Fig.6	–	16	25	ns
T_{sto}	sampling time offset		–	2	–	ns

Notes to the characteristics

1. Low frequency ramp signal ($V_{VI(p-p)} = 1.8$ V and $f_i = 15$ kHz) combined with a sinewave input voltage ($V_{VI(p-p)} = 0.5$ V and $f_i = 4.43$ MHz) at the input.
2. Supply voltage ripple rejection (SVRR): variation of the input voltage produces output code 31 for a supply voltage variation of 1 V.

$$SVRR = 20 \log \frac{\Delta V_{Vi(31)}}{\Delta V_{CCA}}$$

3. Full-scale sinewave; $f_i = 4.43$ MHz, $f_{CLK} = 20$ MHz.

Table 1 Output coding

STEP	V_I (note 1) (TYP. value)	BINARY OUTPUTS D5 to D0
Underflow	< 2.2 V	000000
0	2.2 V	000000
1	2.215 V	000001
.		......
.		......
.		......
62	3.072 V	111110
63	3.086 V	111111
Overflow	> 3.1 V	111111

Note

1. With clamping capacitance.

Table 2 Mode selection

CEN	D0 to D5
1	high impedance
0	active. Binary

Table 3 Clamp input A

A	CLAMP	DIGITAL OUTPUTS	$V_{in}A$
0	1	X	2.2
1	1	0	2.2

Note

X = don't care.

Table 4 Clamp input B and C

B/C	CLAMP	DIGITAL OUTPUTS	$V_{in}B/V_{in}C$
0	1	X	2.65
1	1	32	2.65

Note

X = don't care.

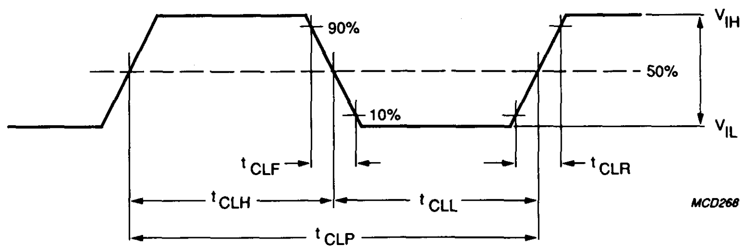


Fig.3 AC clock characteristics.

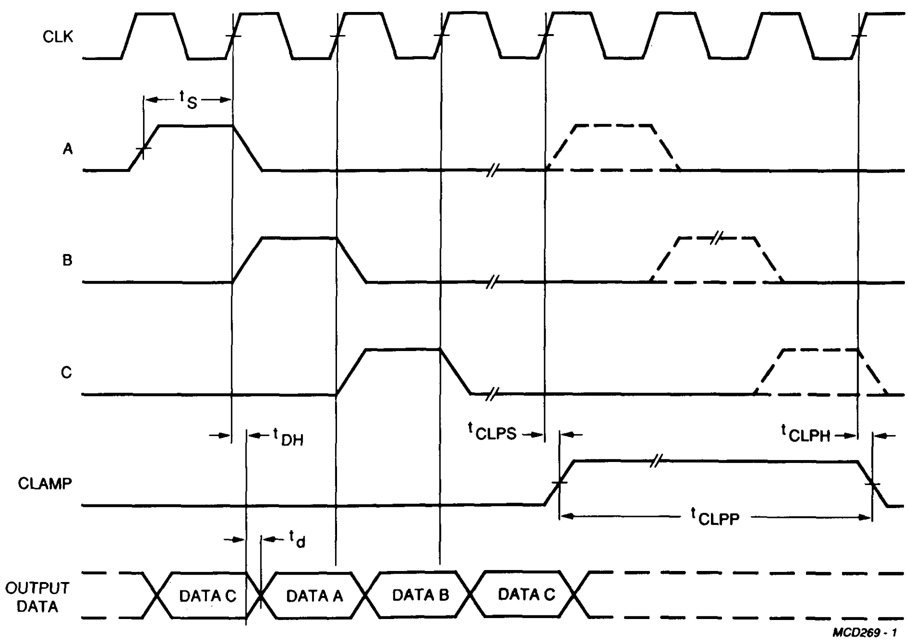


Fig.4 AC characteristics select signals; Clamp, Data.

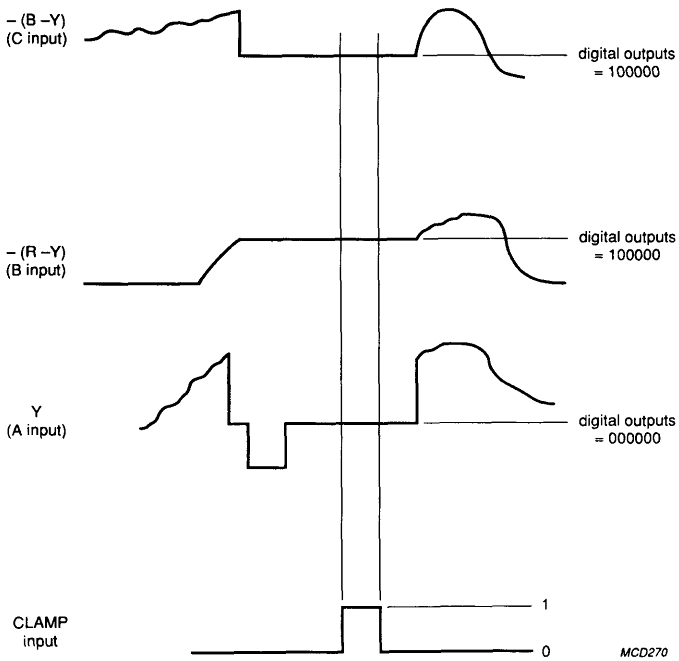


Fig.5 AC characteristics select signals; Clamp, Data.

Table 5 Clamp characteristic related to TV signals

PARAMETER	MIN.	TYP.	MAX.	UNIT
clamping time per line (signal active)	2.2	3.0	3.3	μs
input signals clamped to correct level after	–	3	10	lines

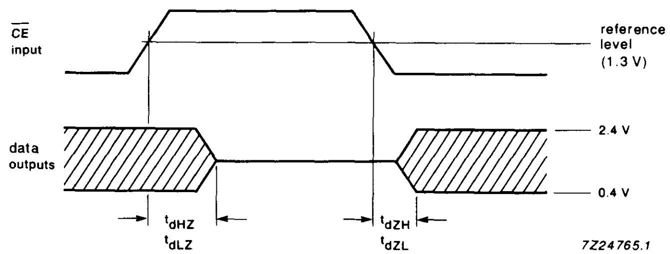


Fig.6 Timing diagram of 3-state delay.

Application information

Additional application information will be supplied on request (please quote reference number FTV/9112).

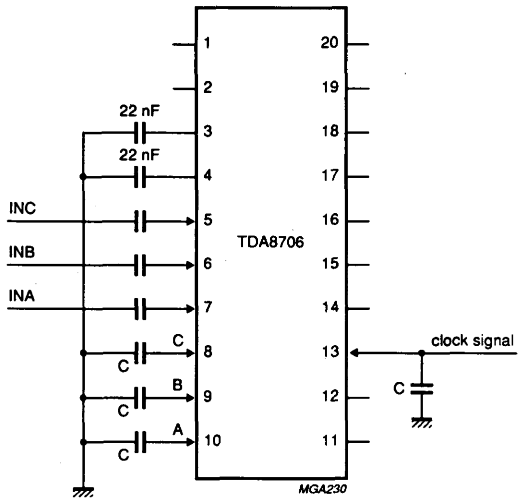


Fig.7 Application diagram.

Notes to figure 7

1. 'C' capacitors must be determined on the output capacitance of the circuits driving A, B and C or CLK pins
2. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder. Do not draw current from these pins in order to achieve good linearity
3. Analog and digital supplies should be separated and decoupled.

Video analog input interface — TDA8708A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS and Y signals
- No sample-and-hold circuit required.

APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing.

GENERAL DESCRIPTION

The TDA8708A is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	37	45	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (AGC amplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	365	500	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8708A	28	DIL	plastic	SOT117
TDA8708AT	28	SO28	plastic	SOT136A

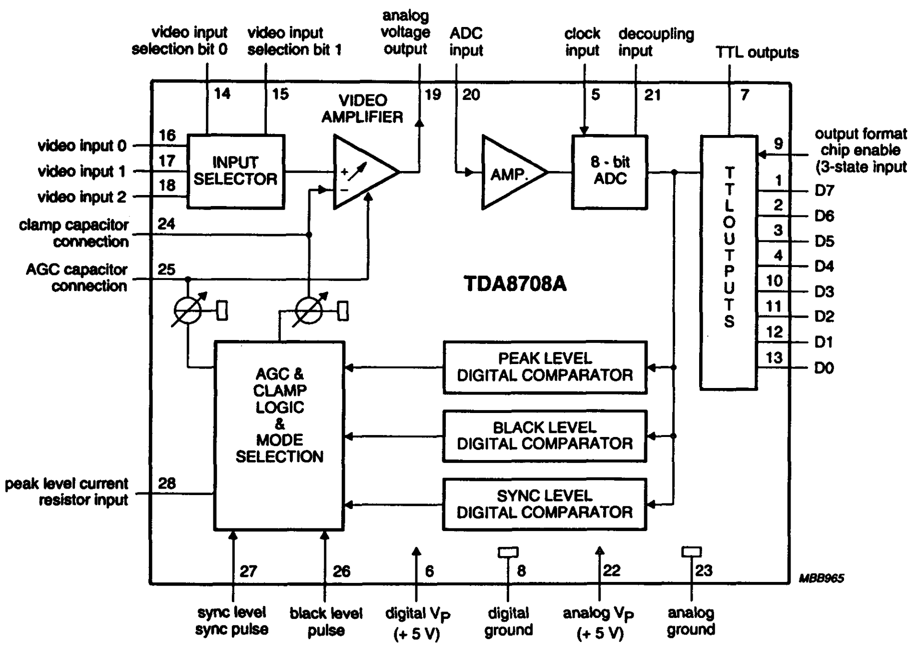


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V_{CCD}	6	digital positive supply voltage (5 V)
V_{CCO}	7	TTL outputs positive supply voltage (5 V)
DGND	8	digital ground
OF	9	output format/chip enable (3-state input)
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog positive supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
AGC	25	AGC capacitor connection
GATE B	26	black level synchronization pulse
GATE A	27	sync level synchronization pulse
RPEAK	28	peak level current resistor input

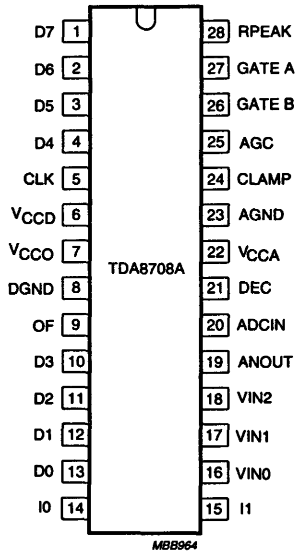


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8708A provides a simple interface for decoding video signals.

The TDA8708A operates in configuration mode 1 (see Fig.4) when the video signals are weak (i.e. when the gain of the AGC amplifier has not yet reached its optimum value). This enables a fast recovery of the synchronization pulses in the decoder circuit. When the pulses at the GATE A and GATE B inputs become distinct (GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively) the TDA8708A automatically switches to configuration mode 2.

When the TDA8708A is in configuration mode 1, the gain of the AGC amplifier will be roughly adjusted (sync level to a digital output level of 0 and the peak level to a digital output level of 255).

In configuration mode 2 the digital output of the ADC is compared to internal digital reference levels. The resultant outputs control the charge or discharge current of a capacitor connected to the AGC pin. The voltage across this capacitor controls the gain of the video amplifier. This is the gain control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that the sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 0 at the converter output. As the black level is at digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The peak-white control loop is always active. If the video signal tends to exceed the digital code of 248, the gain will be limited to avoid any over-range of the converter.

The use of nominal signals will prevent the output from exceeding a digital code of 213 and the peak-white control loop will be non-active.

The clamp level control is accomplished by using the same techniques as used for the gain control. The black-level digital comparator is active during a positive-going pulse at the GATE B input. The clamp capacitor will be charged or discharged to adjust the digital output to code 64.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
V_{CCO}	output supply voltage	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage difference	−1.0	+1.0	V
$V_{CCO} - V_{CCD}$	supply voltage difference	−1.0	+1.0	V
$V_{CCA} - V_{CCO}$	supply voltage difference	−1.0	+1.0	V
V_I	input voltage	−0.3	V_{CCA}	V
I_O	output current	0	+10	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT117	55 K/W
	SOT136A	70 K/W

CHARACTERISTICS

$V_{CCA} = V_{22} - V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6 - V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7 - V_8 = 4.2$ to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCA} - V_{CCO} = -0.5$ to +0.5 V; $T_{amb} = 0$ to +70 °C; Typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	37	45	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	output supply current	TTL load (see Fig.8)	–	12	16	mA
Video amplifier inputs						
VIN(0-2) inputs						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	AGC load with external capacitor; note 1	0.6	–	1.5	V
$\|Z_I\|$	input impedance	f = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
I0 and I1 TTL inputs (see Table 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	−400	–	–	μA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	μA
Gate A and gate B TTL inputs (see Figs 4 and 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	−400	–	–	μA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	μA
t_W	pulse width	see Fig.5	2	–	–	μs
RPEAK input (pin 28)						
I_{28}	minimum peak level current	$R_{28} = 0$ Ω	–	80	150	μA
AGC input (pin 25)						
V_{25}	AGC voltage for minimum gain		–	2.8	–	V
V_{25}	AGC voltage for maximum gain		–	4.0	–	V
	AGC output current	see Table 2	–	–	–	
CLAMP input (pin 24)						
V_{24}	CLAMP voltage for code 128 output		–	3.5	–	V
I_{24}	CLAMP output current	see Table 3	–	–	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT output (pin 19)						
$V_{19(p-p)}$	output AC voltage (peak-to-peak value)	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1.33 V (p-p); note 2	-	-	1.0	mA
V_{19}	output DC voltage for black level	note 3	–	V_{CCA}–2.24	–	V
Z_{19}	output impedance		–	20	–	Ω
Video amplifier dynamic characteristics						
α	crosstalk between VIN inputs	V_{CCA} = 4.75 to 5.25 V	–	–50	–45	dB
G_{diff}	differential gain	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	2	–	%
ϕ_{diff}	differential phase	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	0.8	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range	see Fig.10	–4.5	–	6.0	dB
G_{stab}	gain stability as a function of supply voltage and temperature	see Fig.10	–	–	5	%
Analog-to-digital converter inputs						
CLK input (pin 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{CLK} = 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{CLK} = 10 MHz	–	4.5	–	pF
OF input (3-state; see Table 4)						
V_{IL}	LOW level input voltage		0	–	0.2	V
V_{IH}	HIGH level input voltage		2.6	–	V_{CCD}	V
V_9	input voltage in HIGH-Z state		–	1.15	–	V
I_{IL}	LOW level input current		–370	–300	–	μA
I_{IH}	HIGH level input current		–	360	450	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN input (pin 20; see Table 5)						
V_{20}	input voltage	digital output = 00	–	V_{CCA}–2.41	–	V
V_{20}	input voltage	digital output = 255	–	V_{CCA}–1.41	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f = 6 MHz	–	50	–	MΩ
C_i	input capacitance	f = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
Digital outputs D(0-7)						
V_L	LOW level output voltage	I_O = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	μA
Switching characteristics						
f_{CLK}	CLK input maximum frequency	see Fig.6; note 6	30	32	–	MHz
Analog signal processing (f_{CLK} = 32 MHz; see Fig.8)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); note 7; Fig.3	–	2	–	%
ϕ_{diff}	differential phase	note 7; Fig.3	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz; note 7	–	–55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function (see Fig.8)						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{CLK} = 32 MHz; see Figs 6, 7 and 8)						
Digital outputs (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ)						
t_{ds}	sampling delay		–	2	–	ns
t_{HD}	output hold time		6	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time - output enable		–	19	25	ns
t_{dDZ}	3-state delay time - output disable		–	14	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converter inputs						
CLK input (pin 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	µA
$\|Z_i\|$	input impedance	f_{CLK} = 10 MHz	–	4	–	kΩ
C_i	input capacitance	f_{CLK} = 10 MHz	–	4.5	–	pF
OF input (3-state; see Table 4)						
V_{IL}	LOW level input voltage		0	–	0.2	V
V_{IH}	HIGH level input voltage		2.6	–	V_{CCD}	V
V_9	input voltage in HIGH-Z state		–	1.15	–	V
I_{IL}	LOW level input current		–370	–300	–	µA
I_{IH}	HIGH level input current		–	360	450	µA
ADCIN input (pin 20; see Table 5)						
V_{20}	input voltage	digital output = 00	–	V_{CCA}–2.41	–	V
V_{20}	input voltage	digital output = 255	–	V_{CCA}–1.41	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	µA
$\|Z_i\|$	input impedance	f = 6 MHz	–	50	–	MΩ
C_i	input capacitance	f = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
Digital outputs D(0-7)						
V_L	LOW level output voltage	I_O = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	µA
Switching characteristics						
f_{CLK}	CLK input maximum frequency	see Fig.6; note 6	30	32	–	MHz
Analog signal processing (f_{CLK} = 32 MHz; see Fig.8)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); note 7; Fig.3	–	2	–	%
ϕ_{diff}	differential phase	note 7; Fig.3	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz; note 7	–	–55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transfer function (see Fig.8)						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{CLK} = 32 MHz; see Figs 6, 7 and 8)						
Digital outputs (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ)						
t_{ds}	sampling delay		–	2	–	ns
t_{HD}	output hold time		6	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time - output enable		–	19	25	ns
t_{dDZ}	3-state delay time - output disable		–	14	20	ns

Notes

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)}$ = 1.33 V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referred to V_{CC} and defined as:

   AC impedance ≥ 1 kΩ and the DC impedance > 2.7 kΩ.

   The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Control mode 2 is selected.
4. Signal-to-noise ratio measured with 5 MHz bandwidth

$$SN = 20\log\frac{V_{ANNOUT(p-p)}}{V_{ANNOUT}\ noise\ RMS\ (B = 5\ MHz)}$$

5. The voltage ratio is expressed as:

$$SVRR1 = 20\log\frac{\Delta V_{CCA}/V_{CCA}}{\Delta G/G}$$

   for V_i = 1 V (p-p), 100 kHz gain = 1 and 1 V supply variation.
6. It is recommended that the rise and fall times of the clock are not less than 2 ns. In addition, a 'good lay-out' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

$$SVRR2 = \frac{\Delta[V_{IN(00)} - V_{IN(FF)}] + [V_{IN(00)} - V_{IN(FF)}]}{\Delta V_{CCA}}$$

9. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}, $\overline{f_{CLK}}$ = 27 MHz).

Table 1 Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 2 AGC output current.

GATE A	GATE B	DIGITAL OUTPUT	I_{AGC}	MODE
1	1	output < 255 output > 255	−2.5 μA I_{PEAK}	1
0	X	output < 248 output > 248	0 I_{PEAK}	2; note 2
1	0	output < 0 0 < output < 248 output > 248	+2.5 μA −2.5 μA I_{PEAK}	2; note 2

Notes to Table 2

1. Where X = don't care.
2. Mode 2 can only be initialized with successive pulses on GATE A and GATE B (see Fig.5).

Table 3 CLAMP output current.

GATE A	GATE B	DIGITAL OUTPUT	I_{CLAMP}	MODE
1	1	output < 0 output > 0	I_{PEAK} −2.5 μA	1
X	0	X	0	2
0	1	output < 64 64 < output	+50 μA −50 μA	2

Note to Table 3

1. Where X = don't care.

Table 4 OF input coding.

OF	D0 TO D7
0	active, two's complement
1	high impedance
open circuit (note 1)	active, binary

Note to Table 4

1. Use C ≥ 10 pF to DGND.

Table 5 Output coding and input voltage (typical values).

		BINARY OUTPUTS								TWO'S COMPLEMENT							
STEP	V_{ADCIN}	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} - 2.41 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1		0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
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.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254		1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} - 1.41 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow		1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

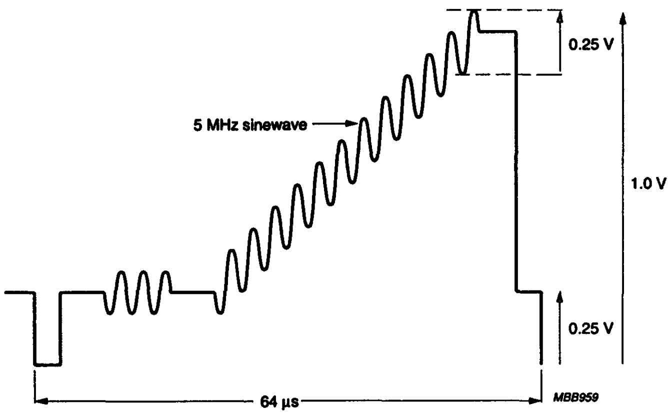


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

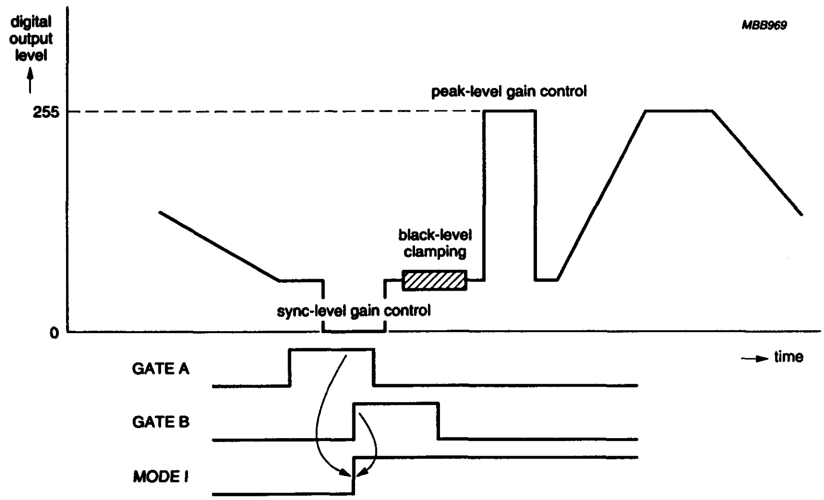


Fig.4 Control mode 1.

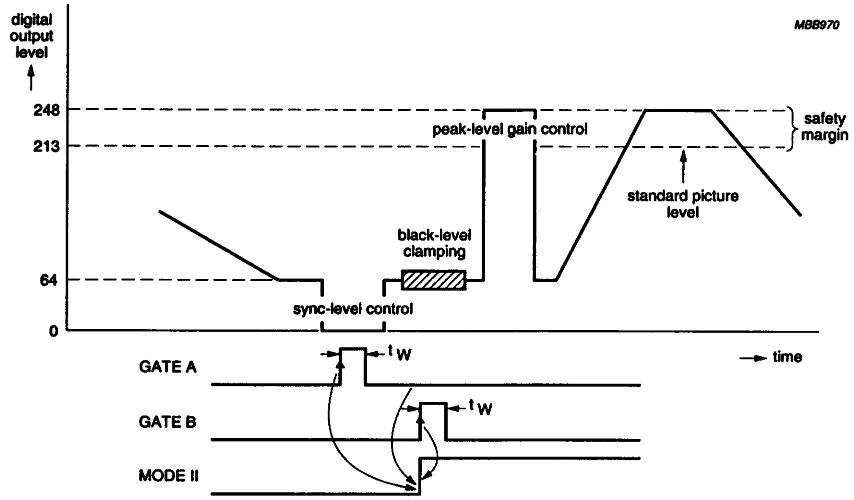


Fig.5 Control mode 2.

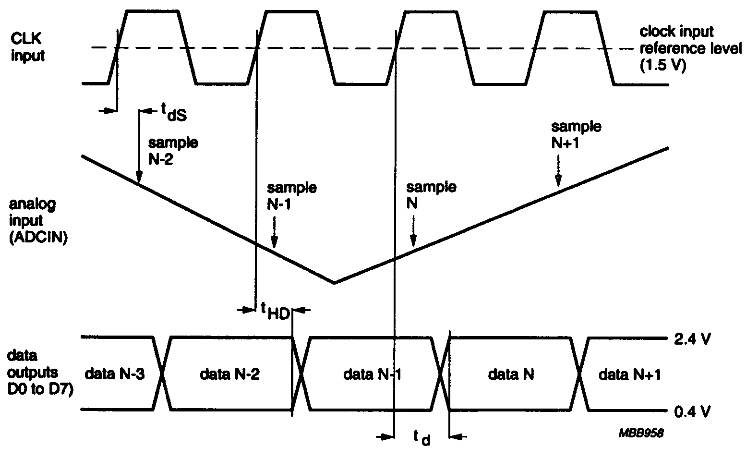


Fig.6 Timing diagram.

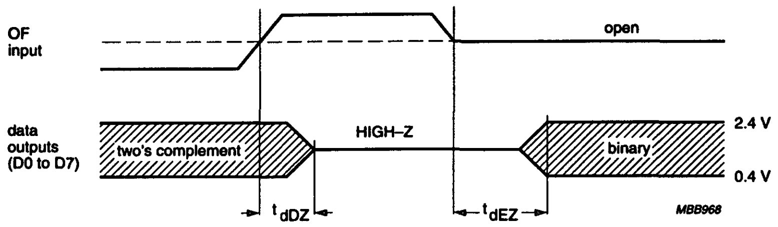


Fig.7 Output format timing diagram.

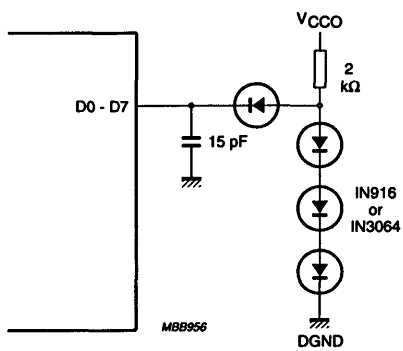


Fig.8 Load circuit for timing measurement; data outputs (OF = LOW or open-circuit).

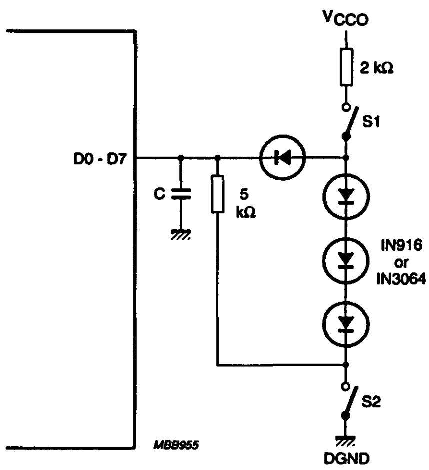
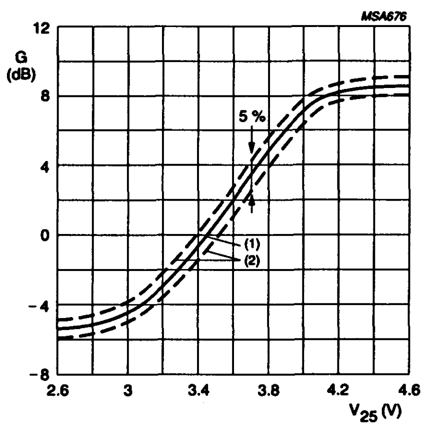


Fig.9 Load circuit for timing measurement; 3-state outputs (OF: f_i = 1 MHz; V_{OF} = 3 V).



(1)Typical value (V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25°C)(2)Minimum and maximum values (temperature and supply)

Fig.10 Gain control curve.

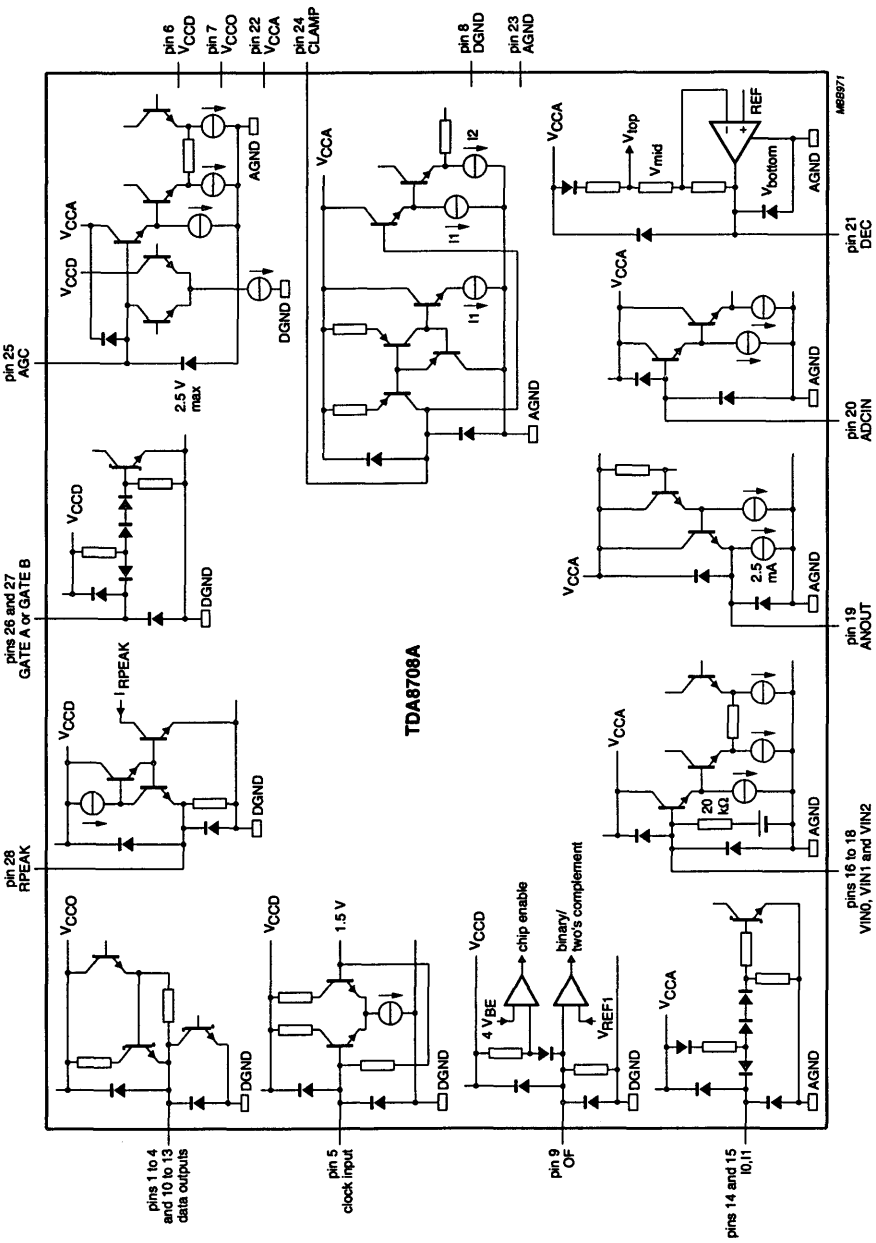
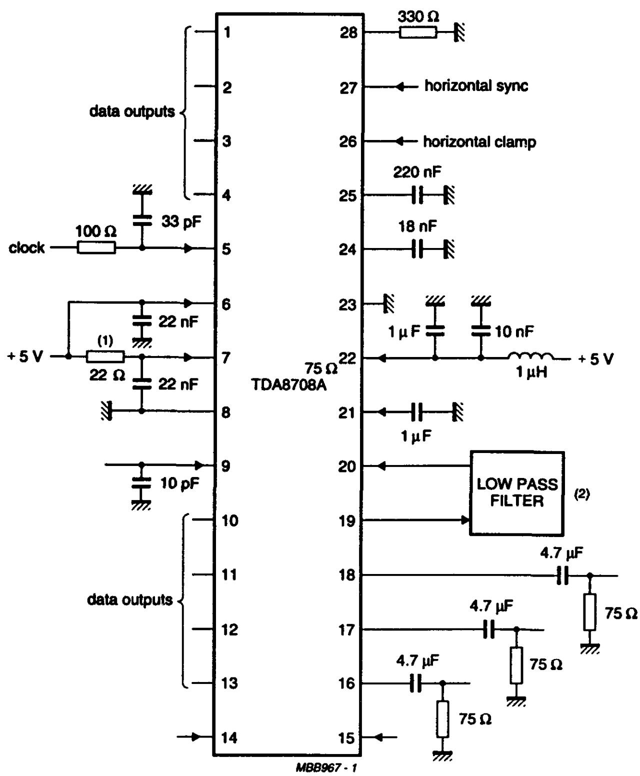


Fig.11 Internal pin configuration.

APPLICATION INFORMATION

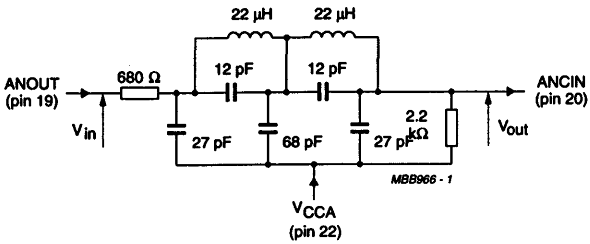
Additional information can be found in the laboratory report FTV/8902.



(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8708A interfaces with a capacitive CMOS load device.

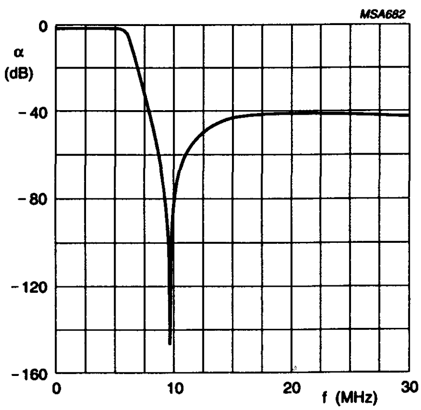
(2) See Figs 13 and 15 for examples of the low-pass filters.

Fig.12 Application diagram.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ respectively must in any event be applied.

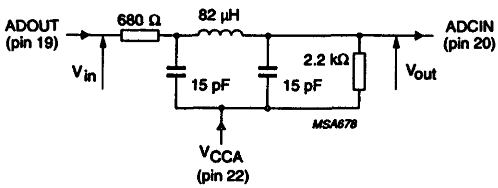
Fig.13 Example of a low-pass filter for CVBS and Y signals.



Characteristics

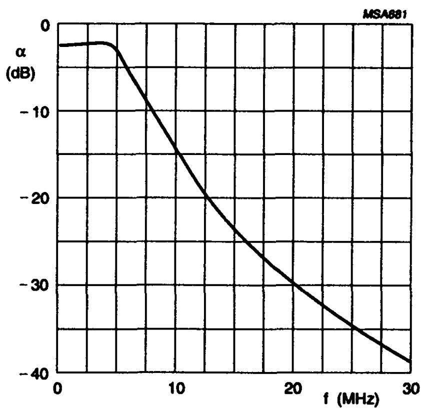
- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- $f_{(-3\ dB)} = 6.5$ MHz
- $f_{(NOTCH)} = 9.75$ MHz

Fig.14 Frequency response for filter shown in Fig.13.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ respectively must in any event be applied.

Fig.15 Example of an economical low-pass filter for CVBS and Y signals.



Characteristics

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- $f_{(-3\ dB)} = 6.5$ MHz

Fig.16 Frequency response for filter shown in Fig.15.

Video analog input interface

TDA8708B

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS and Y signals
- No sample-and-hold circuit required
- The TDA8708B has no white peak control in mode 2 whereas the TDA8708A has one
- In-range output (not TTL) levels.

APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing.

GENERAL DESCRIPTION

The TDA8708B is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	37	45	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (AGC amplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	365	500	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8708B	28	DIL	plastic	SOT117
TDA8708BT	28	SO28	plastic	SOT136A

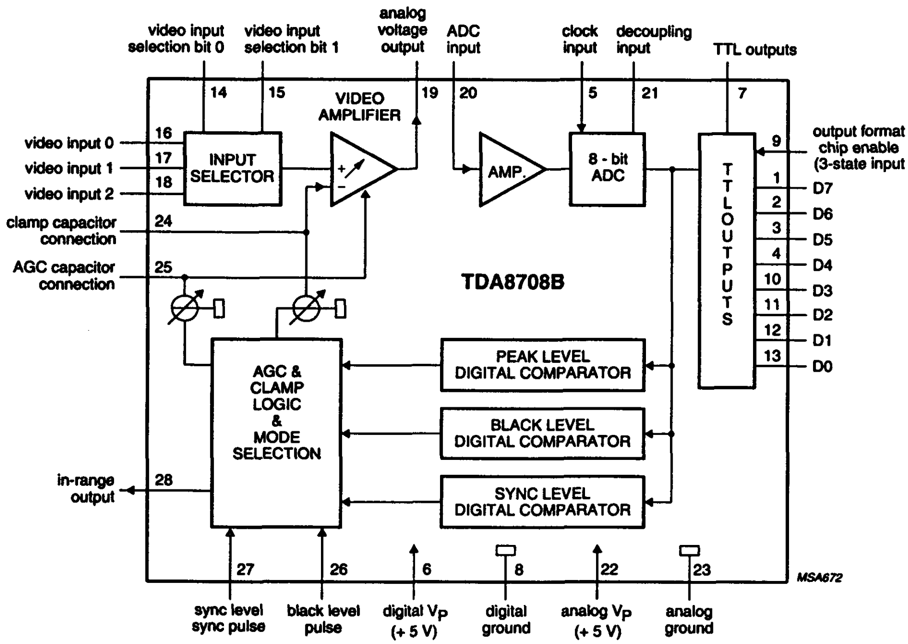


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V_{CCD}	6	digital positive supply voltage (5 V)
V_{CCO}	7	TTL outputs positive supply voltage (5 V)
DGND	8	digital ground
OF	9	output format/chip enable (3-state input)
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog positive supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
AGC	25	AGC capacitor connection
GATE B	26	black level synchronization pulse
GATE A	27	sync level synchronization pulse
IR	28	in-range output

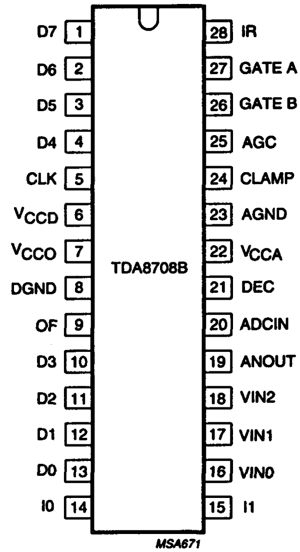


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8708B provides a simple interface for decoding video signals.

The TDA8708B operates in configuration mode 1 (see Fig.4) when the video signals are weak (i.e. when the gain of the AGC amplifier has not yet reached its optimum value). This enables a fast recovery of the synchronization pulses in the decoder circuit. When the pulses at the GATE A and GATE B inputs become distinct (GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively) the TDA8708B automatically switches to configuration mode 2.

When the TDA8708B is in configuration mode 1, the gain of the AGC amplifier will be roughly adjusted (sync level to a digital output level of 0 and the peak level to a digital output level of 255).

In configuration mode 2 the digital output of the ADC is compared to internal digital reference levels. The voltage across the capacitor connected to the AGC pin controls the gain of the video amplifier. This is the gain control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that the sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 0 at the converter output. As the black level is at digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The use of nominal signals will prevent the output from exceeding a digital code of 213.

The clamp level control is accomplished by using the same techniques as used for the gain control. The black-level digital comparator is active during a positive-going pulse at the GATE B input. The clamp capacitor will be charged or discharged to adjust the digital output to code 64.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
V_{CCO}	output supply voltage	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage difference	−1.0	+1.0	V
$V_{CCO} - V_{CCD}$	supply voltage difference	−1.0	+1.0	V
$V_{CCA} - V_{CCO}$	supply voltage difference	−1.0	+1.0	V
V_I	input voltage	−0.3	V_{CCA}	V
I_O	output current	0	+10	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT117	55 K/W
	SOT136A	70 K/W

CHARACTERISTICS

$V_{CCA} = V_{22} - V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6 - V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7 - V_8 = 4.2$ to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ to $+0.5$ V; $V_{CCO} - V_{CCD} = -0.5$ to $+0.5$ V; $V_{CCA} - V_{CCO} = -0.5$ to $+0.5$ V; $T_{amb} = 0$ to $+70$ °C; Typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	37	45	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	output supply current	TTL load (see Fig.8)	–	12	16	mA
Video amplifier inputs						
VIN(0-2) inputs						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	AGC load with external capacitor; note 1	0.6	–	1.5	V
$\|Z_i\|$	input impedance	f = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
I0 and I1 TTL inputs (see Table 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	µA
Gate A and Gate B TTL inputs (see Figs 4 and 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	µA
t_W	pulse width	see Fig.5	2	–	–	µs
AGC input (pin 25)						
V_{25}	AGC voltage for minimum gain		–	2.8	–	V
V_{25}	AGC voltage for maximum gain		–	4.0	–	V
	AGC output current	see Table 2	–	–	–	
Clamp input (pin 24)						
V_{24}	CLAMP voltage for code 128 output		–	3.5	–	V
I_{24}	CLAMP output current	see Table 3	–	–	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT output (pin 19)						
$V_{19(p-p)}$	output AC voltage (peak-to-peak value)	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1.33 V (p-p); note 2	-	-	1.0	mA
V_{19}	output DC voltage for black level	note 3	–	V_{CCA}–2.24	–	V
Z_{19}	output impedance		–	20	–	Ω
Video amplifier dynamic characteristics						
α	crosstalk between VIN inputs	V_{CCA} = 4.75 to 5.25 V	–	–50	–45	dB
G_{diff}	differential gain	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	2	–	%
ϕ_{diff}	differential phase	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	0.8	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range	see Fig.10	–4.5	–	6.0	dB
G_{stab}	gain stability as a function of supply voltage and temperature	see Fig.10	–	–	5	%
Analog-to-digital converter inputs						
CLK input (pin 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{CLK} = 10 MHz	–	4	–	kΩ
C_i	input capacitance	f_{CLK} = 10 MHz	–	4.5	–	pF
OF input (3-state; see Table 4)						
V_{IL}	LOW level input voltage		0	–	0.2	V
V_{IH}	HIGH level input voltage		2.6	–	V_{CCD}	V
V_9	input voltage in HIGH-Z state		–	1.15	–	V
I_{IL}	LOW level input current		–370	–300	–	μA
I_{IH}	HIGH level input current		–	360	450	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN input (pin 20; see Table 5)						
V_{20}	input voltage	digital output = 00	–	V_{CCA}–2.41	–	V
V_{20}	input voltage	digital output = 255	–	V_{CCA}–1.41	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
IR output (pin 28)						
V_{OL}	LOW level output voltage		–	–	1.7	V
V_{OH}	HIGH level output voltage		1.9	–	–	V
I_O	output current		-500	–	–	μA
Digital outputs D(0-7)						
V_L	LOW level output voltage	I_O = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	μA
Switching characteristics						
f_{CLK}	CLK input maximum frequency	see Fig.6; note 6	30	32	–	MHz
Analog signal processing (f_{CLK} = 32 MHz; see Fig.8)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); note 7; Fig.3	–	2	–	%
ϕ_{diff}	differential phase	note 7; Fig.3	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz; note 7	–	–55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function (see Fig.8)						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{CLK} = 32 MHz; see Figs 6, 7 and 8)						
Digital outputs (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ)						
t_{ds}	sampling delay		–	2	–	ns
t_{HD}	output hold time		6	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time - output enable		–	19	25	ns
t_{dDZ}	3-state delay time - output disable		–	14	20	ns

Notes

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)}$ = 1.33 V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referred to V_{CC} and defined as:

   AC impedance ≥ 1 kΩ and the DC impedance > 2.7 kΩ.

   The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Control mode 2 is selected.
4. Signal-to-noise ratio measured with 5 MHz bandwidth

   $$SN = 20\log\frac{V_{ANNOUT(p-p)}}{V_{ANNOUT}\ noise\ RMS\ (B = 5\ MHz)}$$
5. The voltage ratio is expressed as:

   $$SVRR1 = 20\log\frac{\Delta V_{CCA}/V_{CCA}}{\Delta G/G}$$

   for V_I = 1 V (p-p), 100 kHz gain = 1 and 1 V supply variation.
6. It is recommended that the rise and fall times of the clock are not less than 2 ns. In addition, a 'good lay-out' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

   $$SVRR2 = \frac{\Delta[V_{IN(00)} - V_{IN(FF)}] + [V_{IN(00)} - V_{IN(FF)}]}{\Delta V_{CCA}}$$
9. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}, $\overline{f_{CLK}}$ = 27 MHz).

Table 1 Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 2 AGC output current.

GATE A	GATE B	DIGITAL OUTPUT	I_{AGC}	MODE
1	1	output < 255 output > 255	−2.5 μA 130 μA	1
0	X		0	2; note 2
1	0	output < 0 output > 0	+2.5 μA −2.5 μA	2; note 2

Notes to Table 2

1. Where X = don't care.
2. Mode 2 can only be initialized with successive pulses on GATE A and GATE B (see Fig.5).

Table 3 CLAMP output current.

GATE A	GATE B	DIGITAL OUTPUT	I_{CLAMP}	MODE
1	1	output < 0 output > 0	130 μA −2.5 μA	1
X	0	X	0	2
0	1	output < 64 64 < output	+50 μA −50 μA	2

Note to Table 3

1. Where X = don't care.

Table 4 OF input coding.

OF	D0 TO D7
0	active, two's complement
1	high impedance
open circuit (note 1)	active, binary

Note to Table 4

1. Use C ≥ 10 pF to DGND.

Table 5 Output coding and input voltage (typical values).

		BINARY OUTPUTS								TWO'S COMPLEMENT							
STEP	V_{ADCIN}	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} - 2.41 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1		0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254		1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} - 1.41 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow		1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

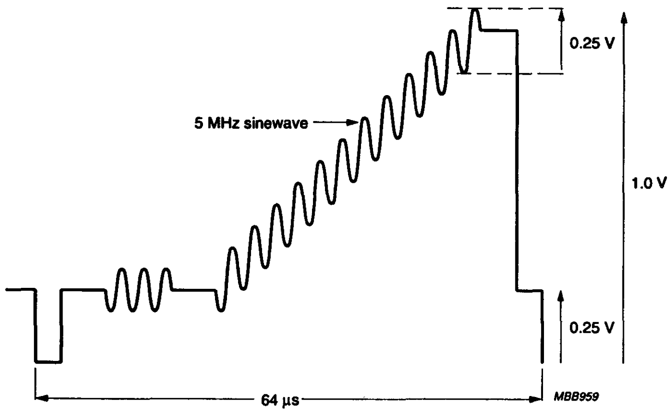


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

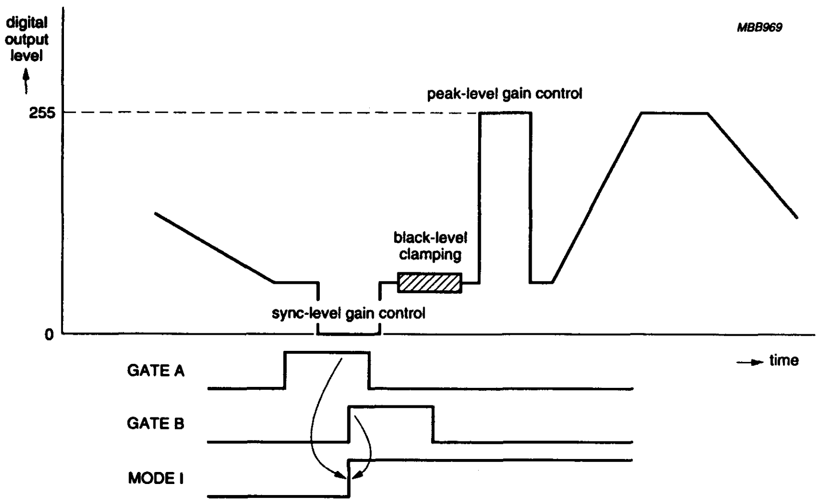


Fig.4 Control mode 1.

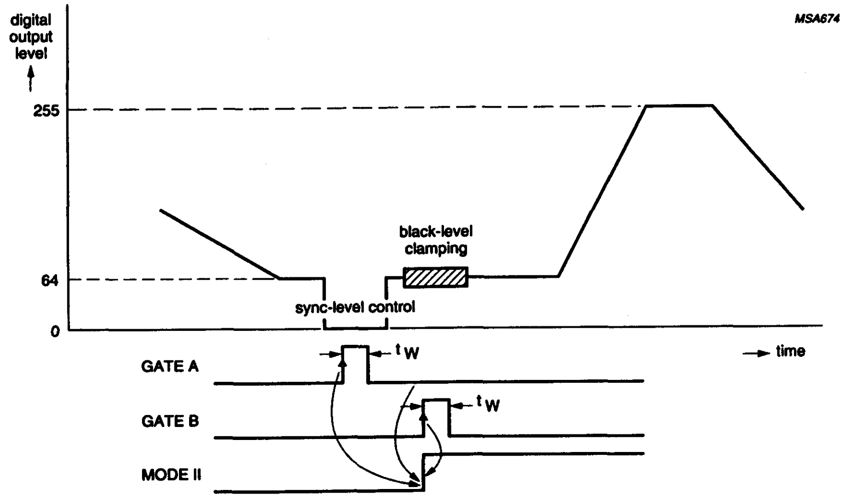


Fig.5 Control mode 2.

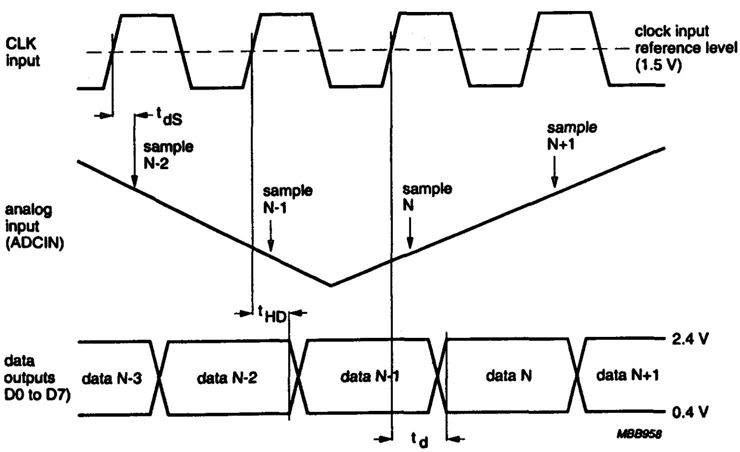


Fig.6 Timing diagram.

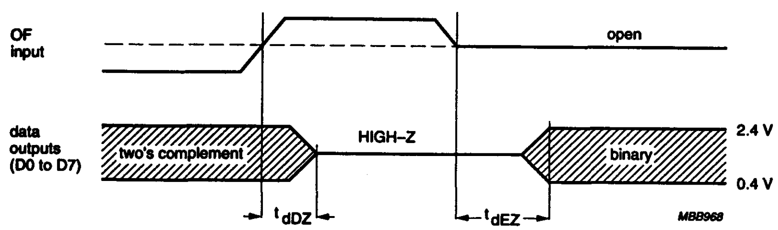


Fig.7 Output format timing diagram.

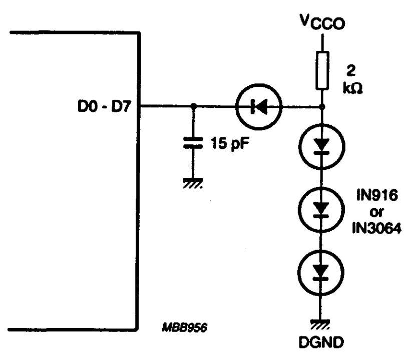


Fig.8 Load circuit for timing measurement; data outputs (OF = LOW or open-circuit).

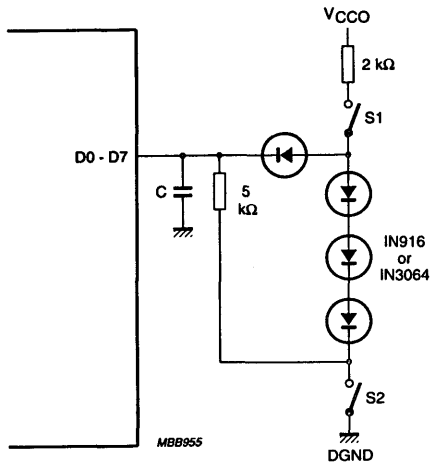
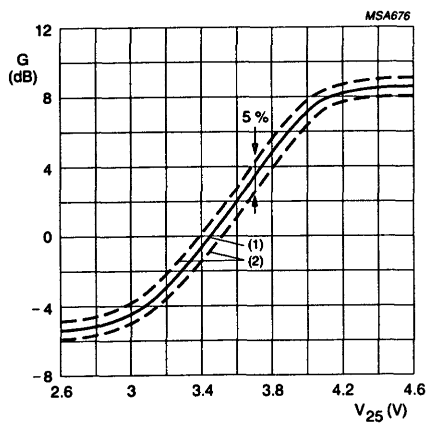


Fig.9 Load circuit for timing measurement; 3-state outputs (OF: f_i = 1 MHz; V_{OF} = 3 V).



(1)Typical value (V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25°C)(2)Minimum and maximum values (temperature and supply)

Fig.10 Gain control curve.

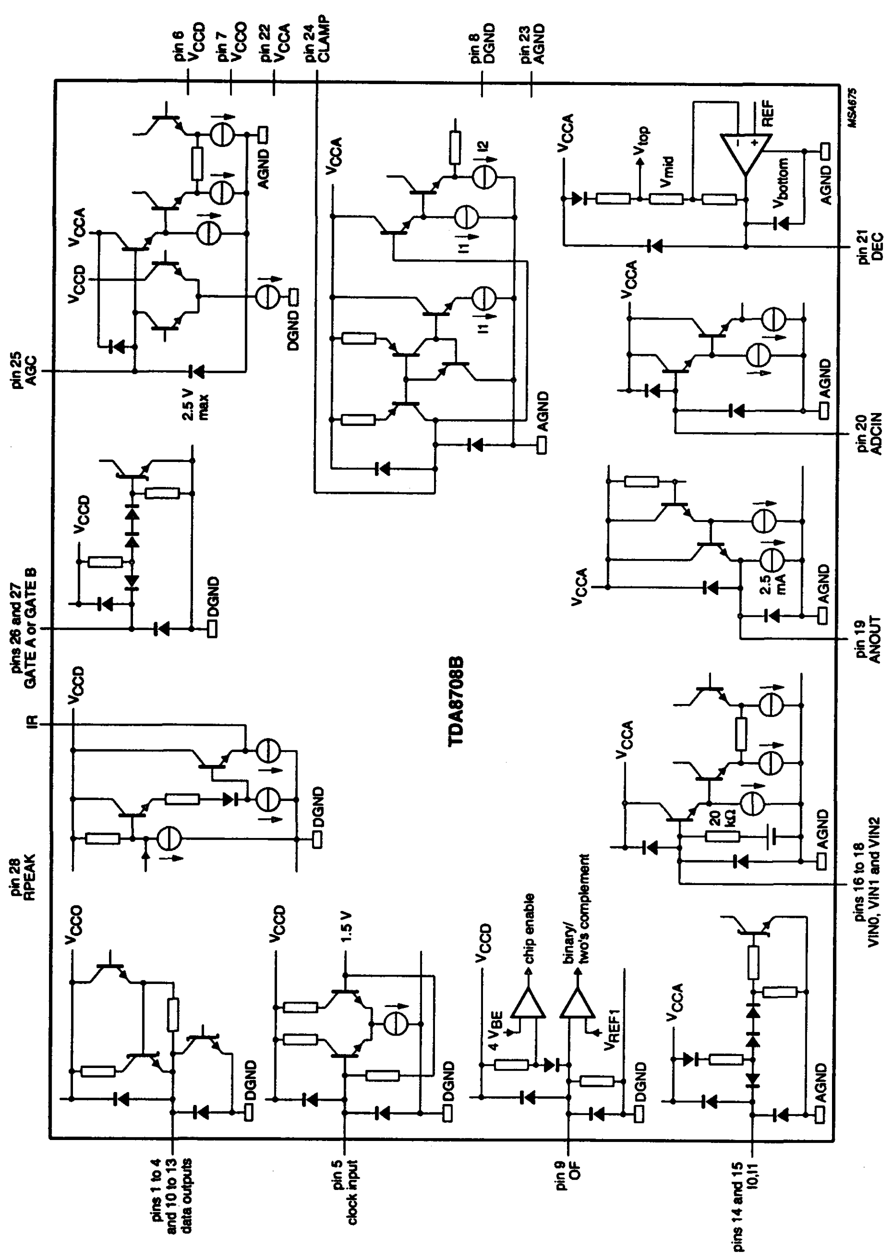
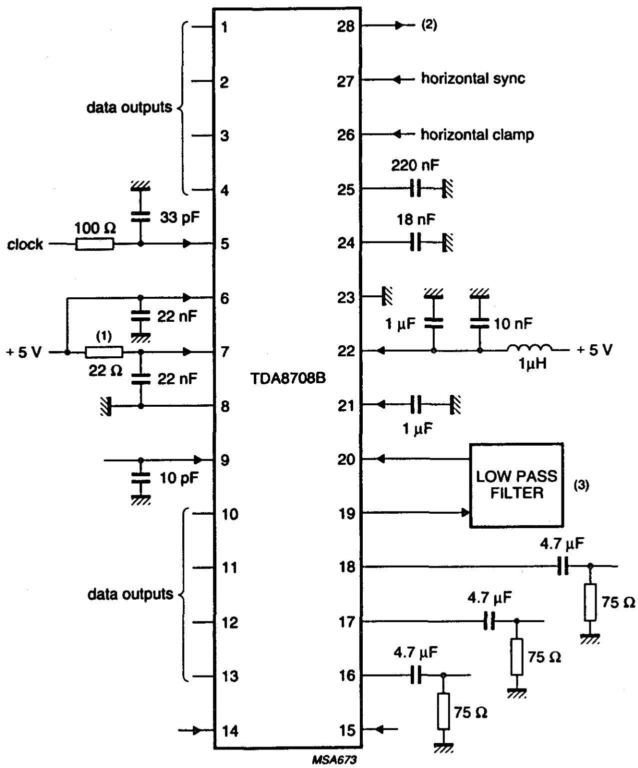


Fig.11 Internal pin configuration.

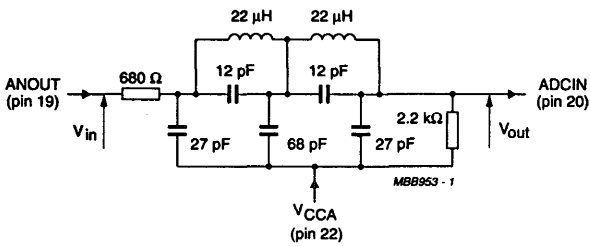
APPLICATION INFORMATION

Additional information can be found in the laboratory report FTV/8902.



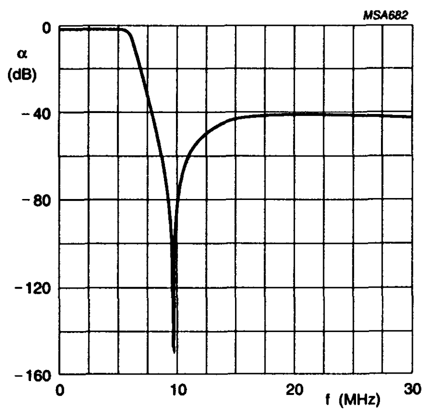
(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8708B interfaces with a capacitive CMOS load device.
(2) When IR is not used, it must be connected to ground via a 47 pF capacitor.
(3) See Figs 13 and 15 for examples of the low-pass filters.

Fig.12 Application diagram.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ respectively must in any event be applied.

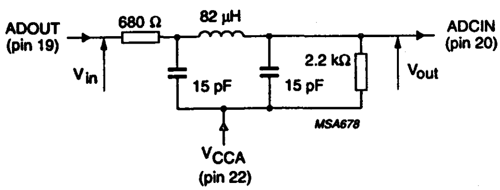
Fig.13 Example of a low-pass filter for CVBS and Y signals.



Characteristics

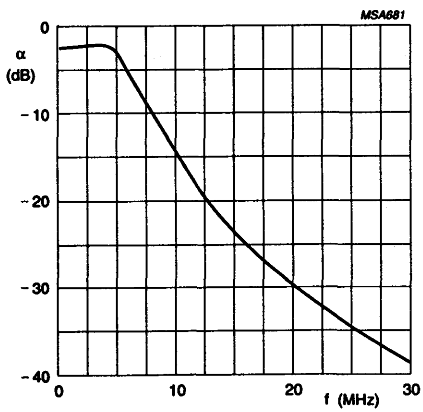
- Order 5; adapted CHEBYSHEV
- Ripple at ≤ 0.4 dB
- $f_{(-3\ dB)}$ = 6.5 MHz
- $f_{(NOTCH)}$ = 9.75 MHz

Fig.14 Frequency response for filter shown in Fig.13.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ respectively must in any event be applied.

Fig.15 Example of an economical low-pass filter for CVBS and Y signals.



Characteristics

- Order 3; adapted CHEBYSHEV
- Ripple at ≤ 0.4 dB
- $f_{(-3\ dB)}$ = 6.5 MHz

Fig.16 Frequency response for filter shown in Fig.15.

Video analog input interface — TDA8709A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Low level AC clock inputs and outputs
- Clamp function with selection for '16' or '128'
- No sample-and-hold circuit required
- Three selectable video inputs

APPLICATIONS

- Video signal processing
- Digital picture processing
- Frame grabbing
- Colour difference signals (U, V)
- R, G, B signals
- Chrominance signal (C).

GENERAL DESCRIPTION

The TDA8709A is an analog input interface for video signal processing. It includes an input selector (1 out of three video signals), video amplifier with clamp and external gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	40	47	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (preamplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	380	512	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8709A	28	DIL	plastic	SOT117
TDA8709AT	28	SO28	plastic	SOT136A

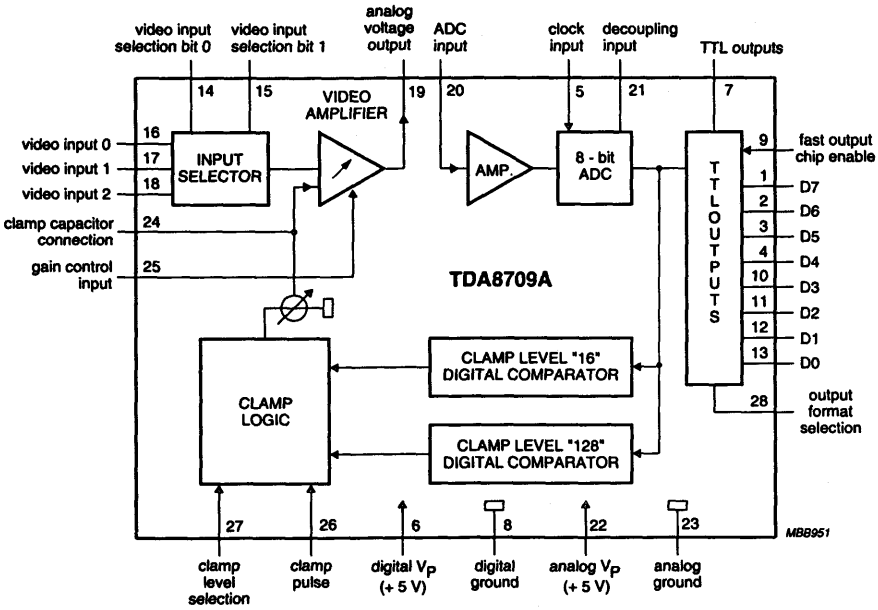


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V_{CCD}	6	digital positive supply voltage (+5 V)
V_{CCO}	7	TTL outputs positive supply voltage (+5 V)
DGND	8	digital ground
FOEN	9	fast output chip enable
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection; bit 0
I1	15	video input selection; bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog positive supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
GAIN	25	gain control input
CLP	26	clamp pulse
CLS	27	clamp level selection
OFS	28	output format selection

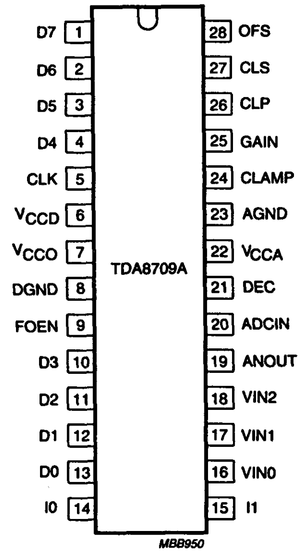


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8709A is an 8-bit ADC with internal clamping and a preamplifier with adjustable gain.

The clamping value is switched via pin 27 between digital 16 (for R, G, B signals) and digital 128 (for chrominance or colour difference signals). While clamping pulse at pin 27 is logic 1, the device will adjust the clamp level to the chosen value. The output format can be selected between binary and two's complement at pin 28.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
V_{CCO}	output supply voltage	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage difference	−0.5	+0.5	V
$V_{CCO} - V_{CCD}$	supply voltage difference	−0.5	+0.5	V
$V_{CCA} - V_{CCO}$	supply voltage difference	−1.0	+1.0	V
V_I	input voltage	−0.3	+7.0	V
I_O	output current	−	+10	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT117	55 K/W
	SOT136A	70 K/W

CHARACTERISTICS

$V_{CCA} = V_{22} - V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6 - V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7 - V_8 = 4.2$ to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCA} - V_{CCO} = -0.5$ to +0.5 V; $T_{amb} = 0$ to +70 °C; Typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	40	47	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	output supply current	TTL load (see Fig.8)	–	12	16	mA
Preamplifier inputs						
VIN(0-2) inputs						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	note 1	0.6	–	1.5	V
$\|Z_I\|$	input impedance	f = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
I0 and I1 TTL inputs (see Table 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	−400	–	–	μA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	μA
CLS, OFS, CLP TTL inputs (see Fig.5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	−400	–	–	μA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	μA
t_{CLP}	clamp pulse width	see Fig.5	2	–	–	μs
GAIN input						
V_{25}	voltage for minimum gain	see Fig.3	–	1.8	–	V
V_{25}	voltage for maximum gain	see Fig.3	–	3.8	–	V
I_I	input current		–	1.0	–	μA
CLAMP input						
I_{24}	clamping output current	see Table 2	–	–	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT output						
$V_{19(p-p)}$	output AC voltage (peak-to-peak value)	V_{OF} = 1.33 V (p-p); V_{25} = 3 V	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1.33 V (p-p); note 2	–	–	1.0	mA
V_{19}	output DC voltage for black level	CLS = logic 1	–	V_{CCA}–2.02	–	V
V_{19}	output DC voltage for black level	CLS = logic 0	–	V_{CCA}–2.6	–	V
Z_{19}	output impedance		–	20	–	Ω
Preamplifier dynamic characteristics						
α	crosstalk between VIN inputs	note 3; V_{CCA} = 4.75 V to 5.25 V	–	–50	–45	dB
G_d	differential gain	V_{VIN} = 1.33 V (p-p); V_{25} = 3 V	–	2	–	%
ϕ_d	differential phase	V_{VIN} = 1.33 V (p-p); V_{25} = 3 V	–	0.8	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range	see Fig.3	–4.5	–	+6	dB
G_{stab}	gain stability as a function of supply and temperature	see Fig.3	–	–	5	%
Analog-to-digital converter inputs						
CLK input						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	μA
$\lvert Z_I \rvert$	input impedance	f_{CLK} = 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{CLK} = 10 MHz	–	4.5	–	pF
FOEN TTL input (see Table 3)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_9 = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_9 = 2.7 V	–	–	+20	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN input (see Table 4)						
V_{20}	input voltage	digital output = 00	–	V_{CCA}–2.52	–	V
V_{20}	input voltage	digital output = 255	–	V_{CCA}–1.52	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	µA
$\|Z_I\|$	input impedance	f = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
Digital outputs D(0-7)						
V_{OL}	LOW level output voltage	I_O = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	µA
Switching characteristics						
f_{CLK}	CLK input maximum frequency	see Fig.6; note 6	30	32	–	MHz
Analog signal processing (f_{CLK} = 32 MHz; see Fig.8)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); note 7; see Fig.4	–	2	–	%
ϕ_{diff}	differential phase	note 7; see Fig.4	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz; note 7	–	–55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{CLK} = 32 MHz; see Figs 6, 7 and 8)						
Digital outputs (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ)						
t_{dS}	sampling delay		–	2	–	ns
t_{HD}	output hold time		–	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time; output enable		–	16	25	ns
t_{dDZ}	3-state delay time; output disable		–	12	25	ns

Notes

1. 0 dB is obtained at the AGC amplifier when applying $V_{i\,(p\text{-}p)} = 1.33$ V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referred to V_{CC} and is defined as:
   AC impedance ≥ 1 kΩ and DC impedance > 2.7 kΩ
   The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Input signals with the same amplitude. Gain is adjusted to obtain ANOUT = 1.33 V (p-p).
4. Signal-to-noise ratio measured with 5 MHz bandwidth
   $$SN = 20\log\frac{V_{ANNOUT(p\text{-}p)}}{V_{ANNOUT}\ noise\ RMS\ (B = 5\ MHz).}$$
5. The voltage ratio is expressed as:
   $$SVRR1 = 20\log\frac{\Delta V_{CCA}/V_{CCA}}{\Delta G/G}$$
   for $V_i = 1$ V (p-p), 100 kHz gain = 1 and 1 V supply variation.
6. It is recommended that the rise and fall times of the clock are not less than 2 ns. In addition, a 'good lay-out' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:
   $$SVRR2 = \frac{\Delta[V_{IN(00)} - V_{IN(FF)}] + [V_{IN(00)} - V_{IN(FF)}]}{\Delta V_{CCA}}$$
9. Full-scale sinewave ($f_i = 4.4$ MHz; f_{CLK}, $f_{\overline{CLK}} = 27$ MHz).

Table 1 Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
1	0	VIN2
0	1	VIN1
1	1	VIN1

Table 2 CLAMP output current.

CLS	CLP	DIGITAL OUTPUT	I_{CLAMP}
1	1	output < 128 output > 128	+50 µA −50 µA
X	0	X	0
0	1	output < 16 16 < output	+50 µA −50 µA

Note

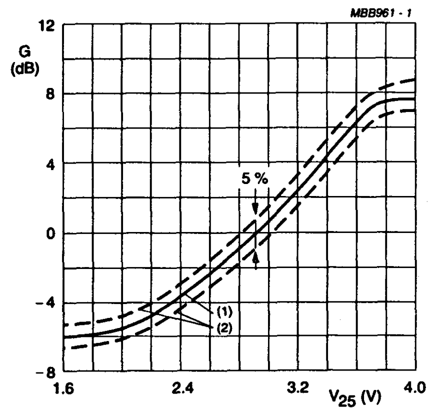
Where; X = don't care

Table 3 FOEN input current.

FOEN	D0 TO D7
0	active
1	high impedance

Table 4 Output coding and input voltage (typical values).

		OFS = 0 BINARY OUTPUTS								OFS = 1 TWO'S COMPLEMENT							
STEP	V_{ADCIN}	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} − 2.52 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1		0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254		1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} − 1.52 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow		1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1



(1) Typical (V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C).
(2) Minimum and maximum (temperature and supply).

Fig.3 Typical gain control curve as a function of gain voltage .

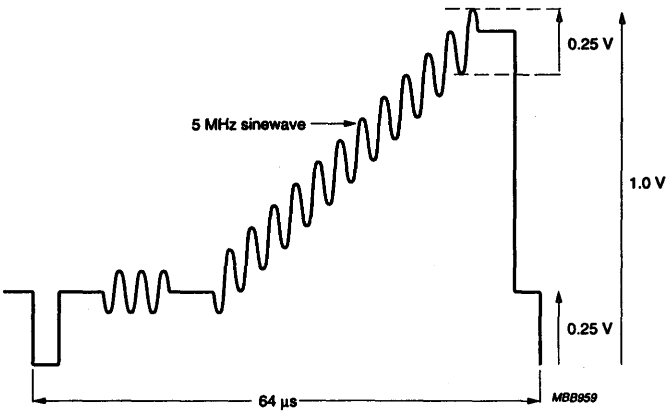


Fig.4 Test signal on the ADCIN pin for differential gain and phase measurements.

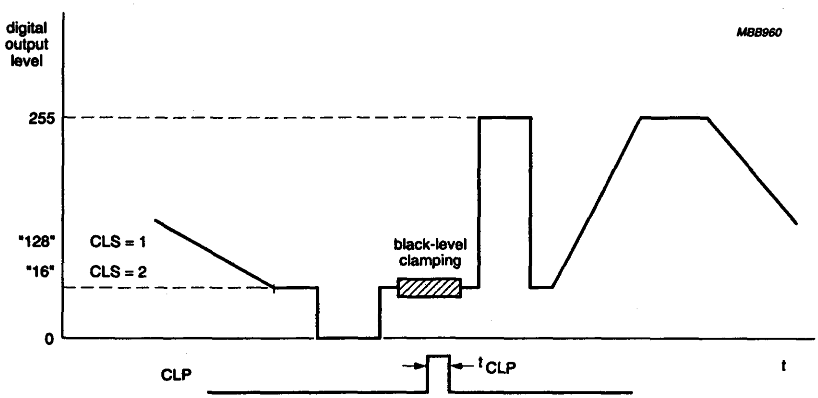


Fig.5 Control mode selection.

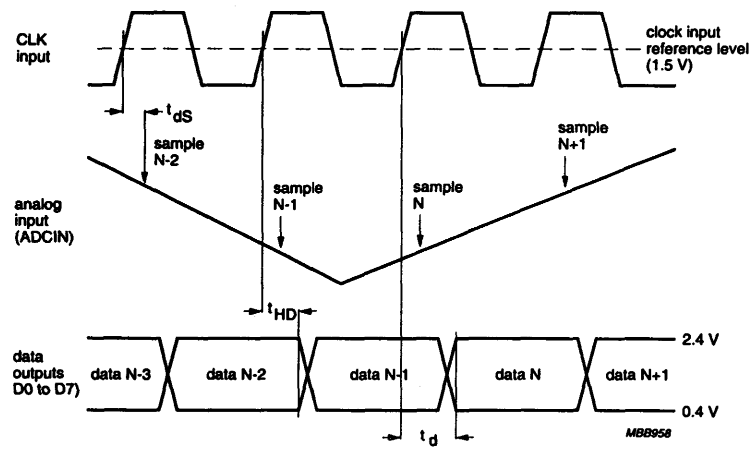


Fig.6 Timing diagram.

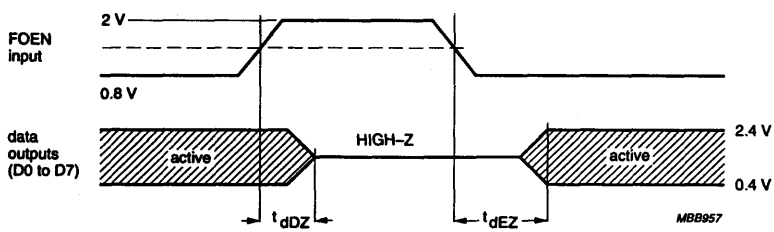


Fig.7 Output format timing diagram.

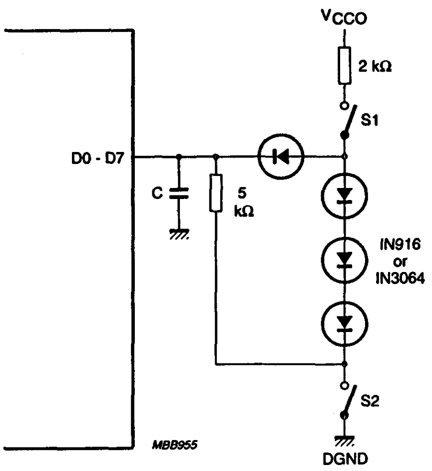


Fig.8 Load circuit for timing measurement; data outputs (FOEN = LOW).

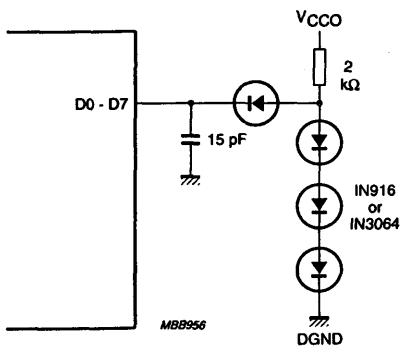


Fig.9 Load circuit for timing measurement; 3-state outputs (FOEN: f_i = 1 MHz; V_{FOEN} = 3 V).

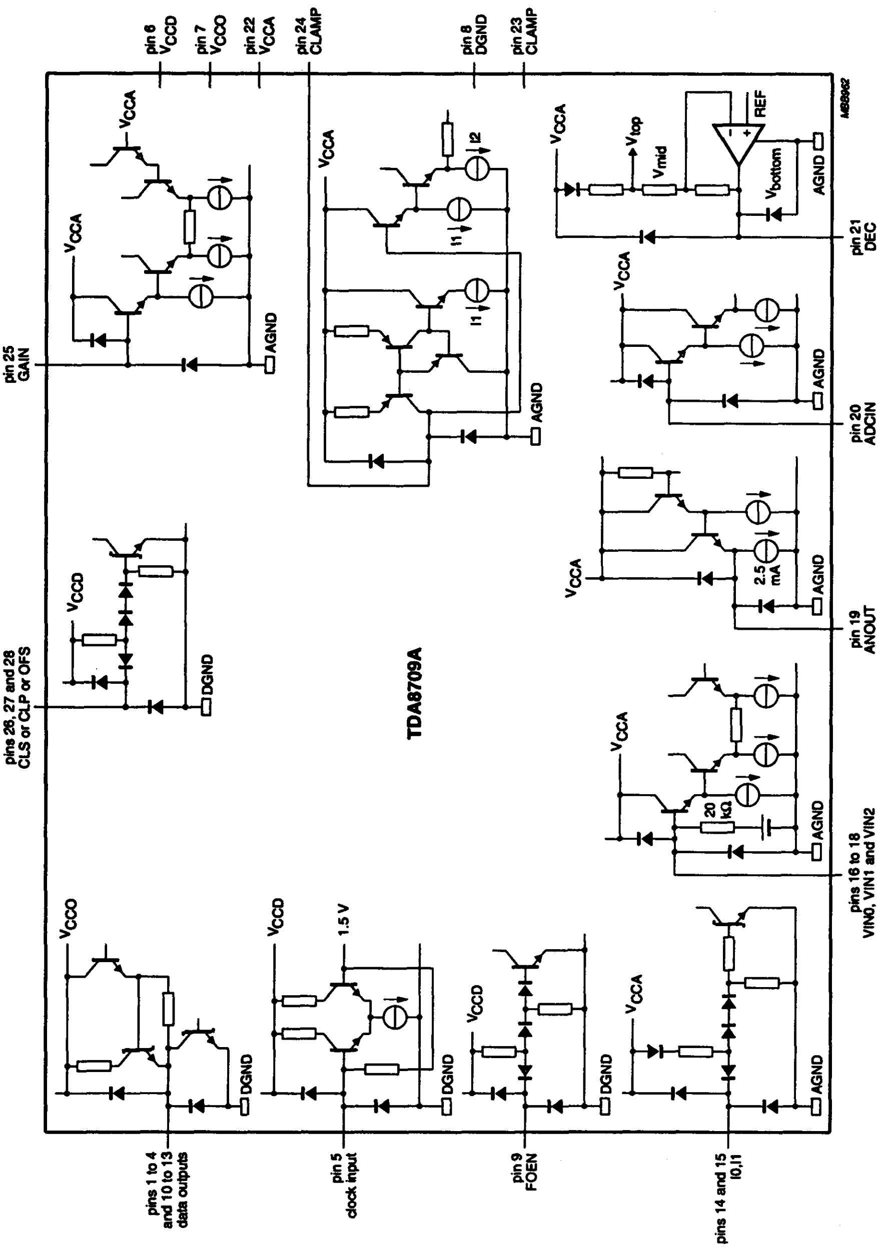
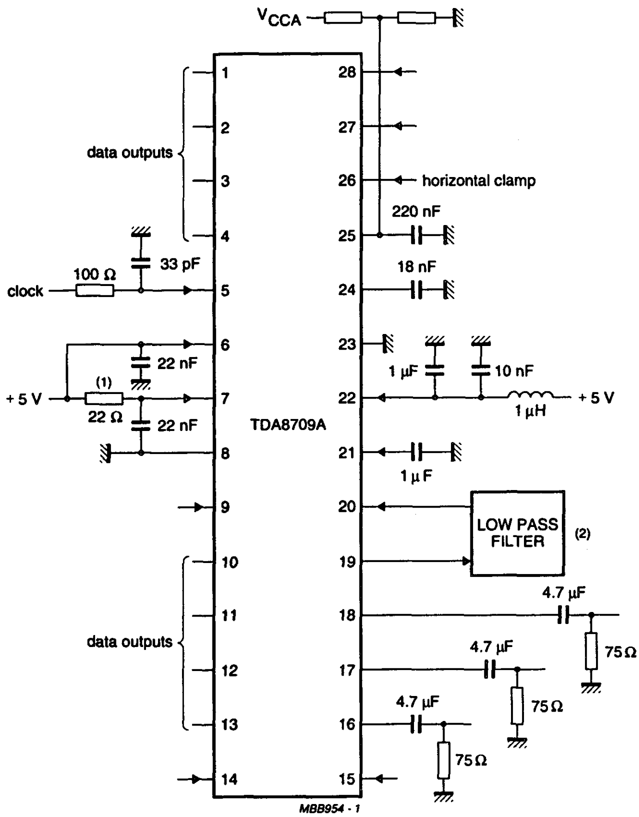


Fig.10 Internal pin configuration.

APPLICATION INFORMATION

Additional information can be found in the laboratory report FTV/9002.



(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8709A interfaces with a capacitive CMOS load device.

(2) *See Figs 12, 14, 16 and 18 for filter examples.*

Fig.11 Application diagram.

Filters

The filters shown in Figs 12, 14, 16 and 18 can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ respectively must be applied.

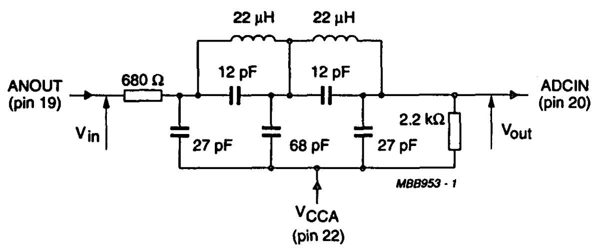
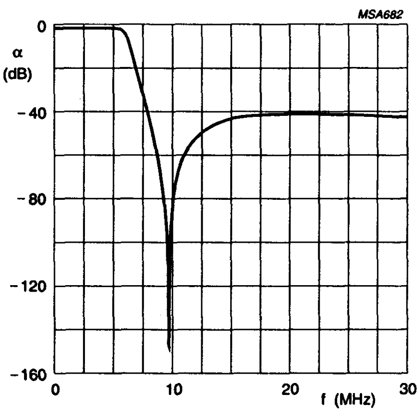


Fig.12 Example of a low-pass filter for RGB and C signals.



Characteristics

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- $f_{(-3\ dB)} = 6.5$ MHz
- $f_{(NOTCH)} = 9.65$ MHz

Fig.13 Frequency response for filter shown in Fig.12.

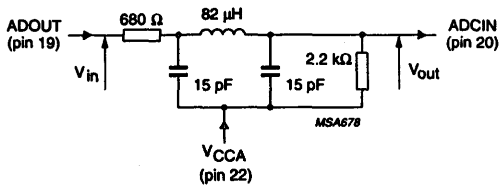
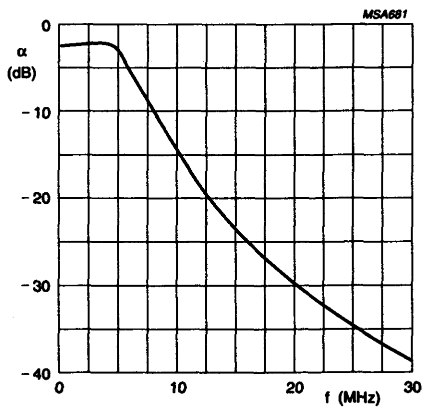


Fig.14 Example of an economical low-pass filter for RGB and C signals.



Characteristics

- Order 3; adapted CHEBYSHEV
- Ripple ρ ≤ 0.4 dB
- $f_{(-3\ dB)}$ ≈ 6.5 MHz

Fig.15 Frequency response for filter shown in Fig.14.

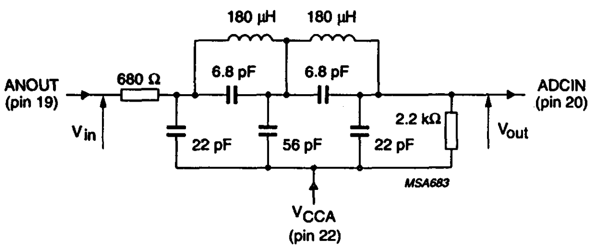
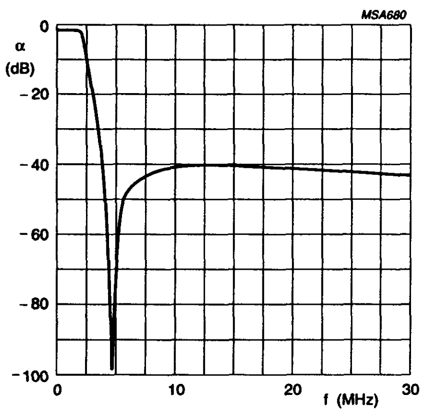


Fig.16 Example of a low-pass filter for U and V signals.



Characteristics

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- $f_{(-3\ dB)} = 2.3$ MHz
- $f_{(NOTCH)} = 4.5$ MHz

Fig.17 Frequency response for filter shown in Fig.16.

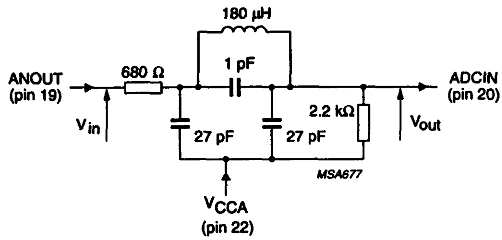
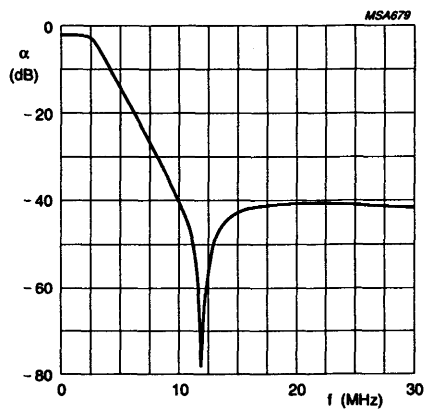


Fig.18 Example of an economical low-pass filter for U and V signals.



Characteristics

- Order 3; adapted CHEBYSHEV
- Ripple $\rho \leq 0.3$ dB
- $f_{(-3\ dB)} = 2.8$ MHz
- $f_{(NOTCH)} = 11.9$ MHz

Fig.19 Frequency response for filter shown in Fig.18.

8-bit video digital-to-analog converter

TDA8712

FEATURES

- 8-bit resolution
- Conversion rate up to 50 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High-speed digital-to-analog conversion
- Digital TV including:
  - field progressive scan
  - line progressive scan
- Subscriber TV decoders
- Satellite TV decoders
- Digital VCRs.

DESCRIPTION

The TDA8712 is an 8-bit digital-to-analog converter (DAC) for video and other applications. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 50 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	–	26	32	mA
I_{CCD}	digital supply current	note 1	–	23	30	mA
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltage (peak-to-peak value)	note 2				
		Z_L = 10 kΩ	−1.45	−1.60	−1.75	V
		Z_L = 75 kΩ	−0.72	−0.80	−0.88	V
ILE	DC integral linearity error		–	–	±1/2	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
f_{CLK}	maximum conversion rate		–	–	50	MHz
B	−3 dB analog bandwidth	f_{CLK} = 50 MHz; note 3	–	150	–	MHz
P_{tot}	total power dissipation		–	250	340	mW

Notes

1. D0 to D7 connected to V_{CCD} and CLK connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The −3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8712	16	DIL	plastic	SOT38
TDA8712T	16	SO16	plastic	SOT162A

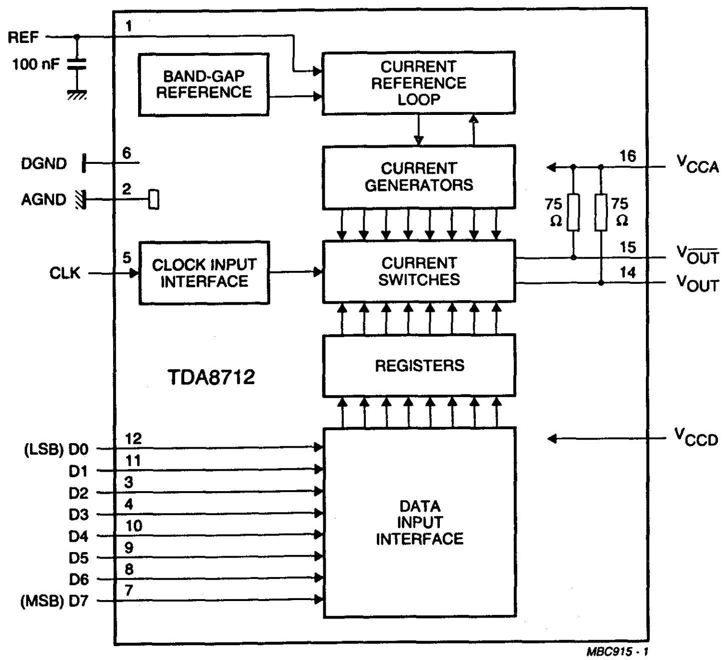


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input; bit 2
D3	4	data input; bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input; bit 7
D6	8	data input; bit 6
D5	9	data input; bit 5
D4	10	data input; bit 4
D1	11	data input; bit 1
D0	12	data input; bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$V_{\overline{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

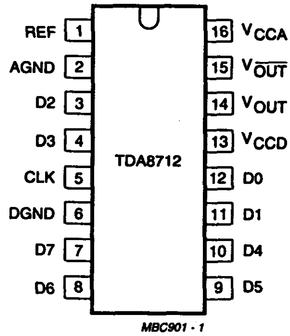


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differential	−0.5	+0.5	V
AGND − DGND	ground voltage differential	−0.1	+0.1	V
V_I	input voltage (pins 3 to 5 and 7 to 12)	−0.3	V_{CCD}	V
$I_{OUT}/\overline{I_{OUT}}$	total output current (pins 14 and 15)	−5	+26	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambienttemperature	0	+70	°C
T_j	junction temperature	−	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT38	70 K/W
	SOT162A	90 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_{16} - V_2$ = 4.5 V to 5.5 V; $V_{CCD} = V_{13} - V_6$ = 4.5 V to 5.5 V; $V_{CCA} - V_{CCD}$ = −0.5 V to +0.5 V; V_{REF} decoupled to AGND by a 100 nF capacitor; T_{amb} = 0 °C to +70 °C; AGND and DGND shorted together; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and T_{amb} = 25 °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	–	26	32	mA
I_{CCD}	digital supply current	note 1	–	23	30	mA
AGND – DGND	ground voltage differential		−0.1	–	+0.1	V
Inputs						
DIGITAL INPUTS (D7 TO D0) AND CLOCK INPUT (CLK)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	–	−0.3	−0.4	mA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	0.01	20	μA
f_{CLK}	maximum clock frequency		30	–	–	MHz
Outputs (note 2; referenced to V_{CCA})						
$V_{OUT} - \overline{V_{OUT}}$	full-scale analog output voltages (peak-to-peak value)					
		Z_L = 10 kΩ	−1.45	−1.60	−1.75	V
		Z_L = 75 Ω	−0.72	−0.80	−0.88	V
V_{OS}	analog offset output voltage	code = 0	–	−3	−25	mV
V_{OUT}/TC	full-scale analog output voltage temperature coefficient		–	–	200	μV/K
V_{OS}/TC	analog offset output voltage temperature coefficient		–	–	20	μV/K
B	−3 dB analog bandwidth	note 3; f_{CLK} = 30 MHz	–	150	–	MHz
G_{diff}	differential gain		–	0.6	–	%
Φ_{diff}	differential phase		–	1	–	deg
Z_O	output impedance		–	75	–	Ω
Transfer function (f_{CLK} = 30 MHz)						
ILE	DC integral linearity error		–	–	±1/2	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB

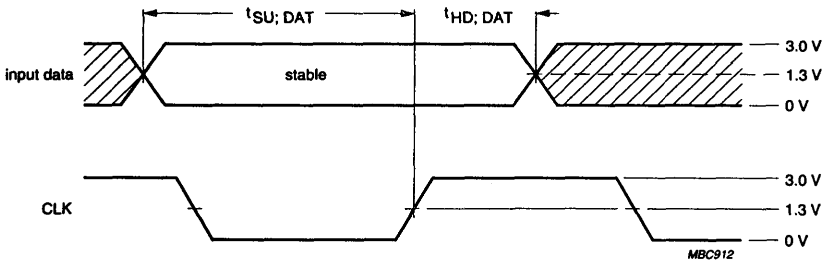
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics (f_{CLK} = 30 MHz; notes 4 and 5; see Figs 3, 4 and 5)						
$t_{SU;DAT}$	data set-up time		−0.3	–	–	ns
$t_{HD;DAT}$	data hold time		2.0	–	–	ns
t_{PD}	propagation delay time		–	–	1.0	ns
t_{S1}	settling time	10% to 90% full-scale change to ±1 LSB	–	1.1	1.5	ns
t_{S2}	settling time	10% to 90% full-scale change to ±1 LSB	–	6.5	8.0	ns
t_d	input to 50% output delay time		–	3.0	5.0	ns
Output transients (glitches; (f_{CLK} = 30 MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	–	–	30	LSB.ns

Notes

1. D0 to D7 are connected to V_{CCD}, CLK is connected to DGND.
2. The analog output voltages (V_{OUT} and $\overline{V_{OUT}}$ are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is 75 Ω (typ.).
3. The −3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).
4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $\overline{V_{OUT}}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data is latched at the rising edge of the clock. The output voltage remains stable (independent of input data variations) during the HIGH level of the clock (CLK = HIGH). During a LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages (see Fig.5).
5. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising edge of the clock and still be recognized. The data hold time ($t_{HD;DAT}$) is the minimum period following the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising edge of the clock and still be recognized.
6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 to 128 and on the falling edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of the offset voltage).

CODE	INPUT DATA (D7 to D0)	DAC OUTPUT VOLTAGES			
		Z_L = 10 kΩ		Z_L = 75 Ω	
		V_{OUT}	$\overline{V_{OUT}}$	V_{OUT}	$\overline{V_{OUT}}$
0	000 00 00	0	−1.6	0	−0.8
1	000 000 01	−0.006	−1.594	−0.003	−0.797
.	....				
128	100 000 00	−0.8	−0.8	−0.4	−0.4
.	....				
254	111 111 10	−1.594	−0.006	−0.797	−0.003
255	111 111 11	−1.6	0	−0.8	0



The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns after the first rising edge of the clock ($t_{SU;DAT}$ is negative; −0.3 ns). Data must be held at least 2 ns after the rising edge ($t_{HD;DAT}$ = +2 ns).

Fig.3 Data set-up and hold times.

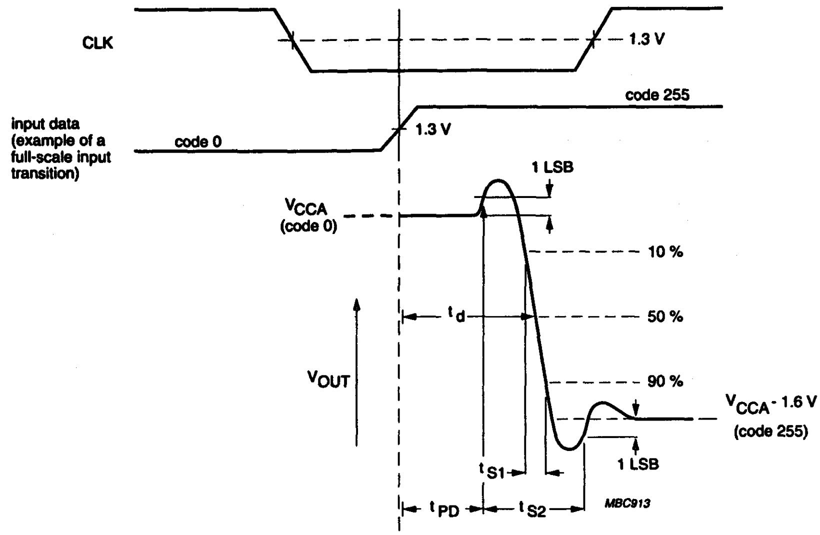
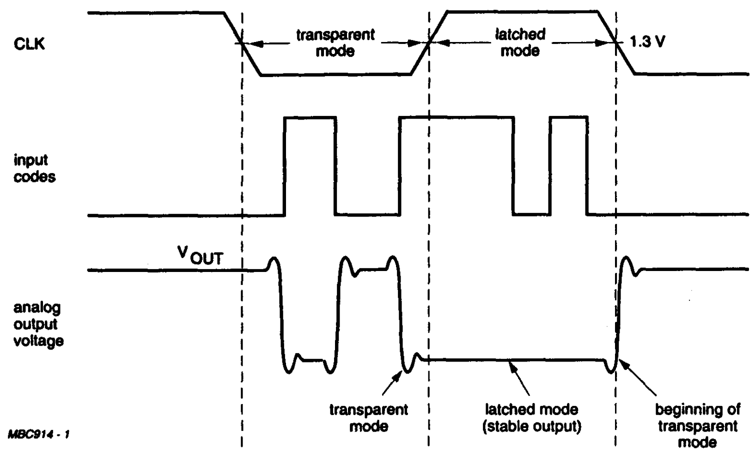
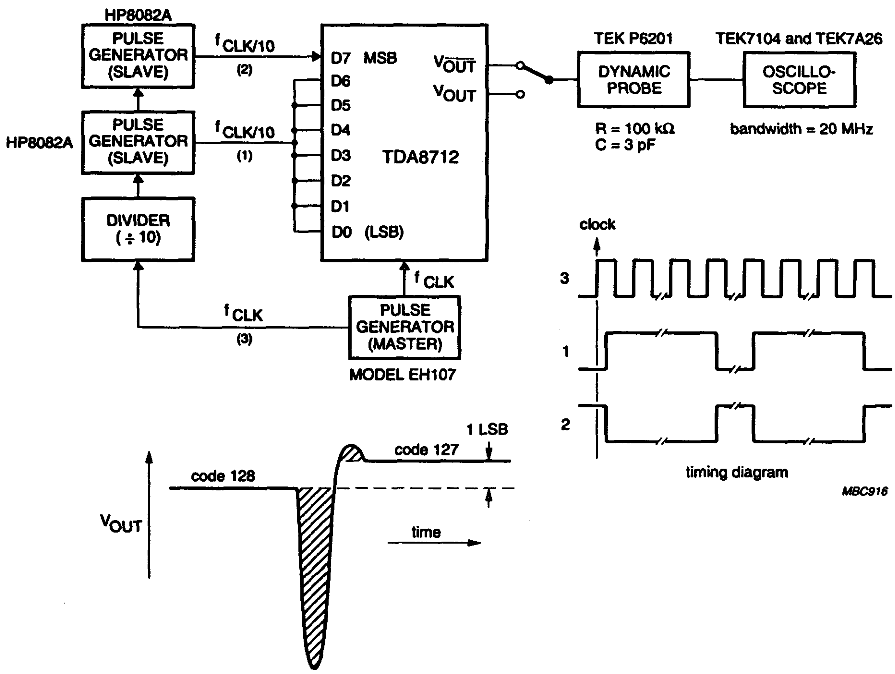


Fig.4 Switching characteristics.



During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable regardless of any change at the input. A change of input data during the latched mode will be seen on the falling edge of the clock (beginning of the transparent mode).

Fig.5 Latched and transparent mode.



The value of the glitch energy is the sum of the shaded area measured in LSB.ns.

Fig.6 Glitch energy measurement.

INTERNAL PIN CONFIGURATIONS

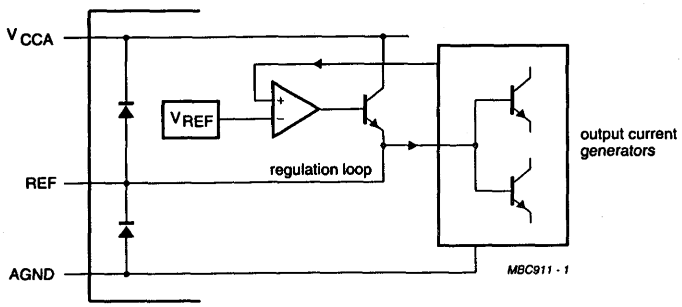


Fig.7 Reference voltage generator decoupling.

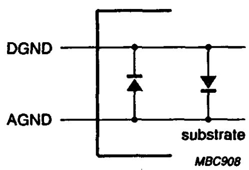


Fig.8 AGND and DGND.

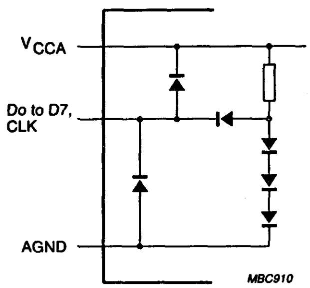


Fig.9 D7 to D0 and CLK.

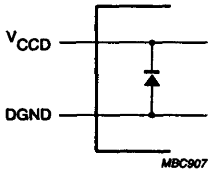


Fig.10 Digital supply.

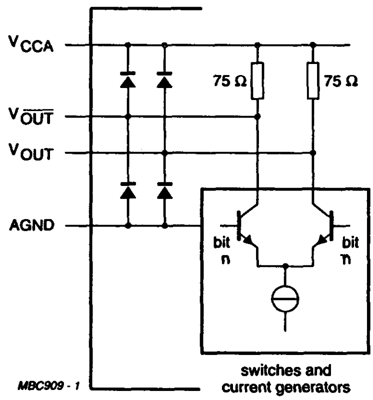


Fig.11 Analog outputs.

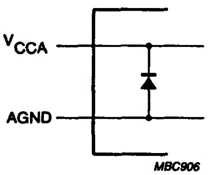
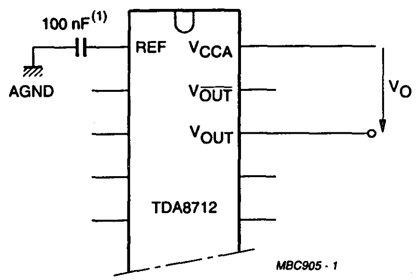


Fig.12 Analog supply.

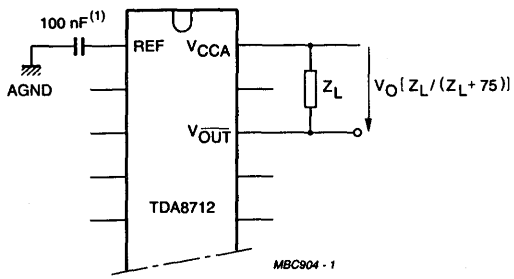
APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).



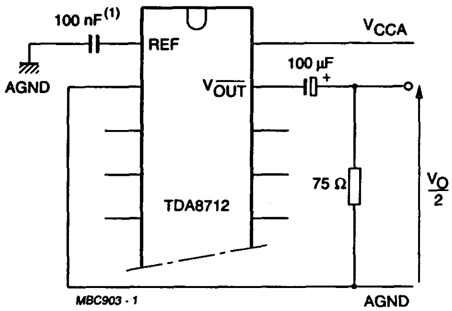
(1) This is a recommended value for decoupling pin 1.

Fig.13 Analog output voltage without external load ($V_O = -V_{\overline{OUT}}$; see Table 1, Z_L = 10 kΩ).



(1) This is a recommended value for decoupling pin 1.

Fig.14 Analog output voltage with external load (external load Z_L = 75 Ω to ∞).



(1) This is a recommended value for decoupling pin 1.

Fig.15 Analog output with AGND as reference.

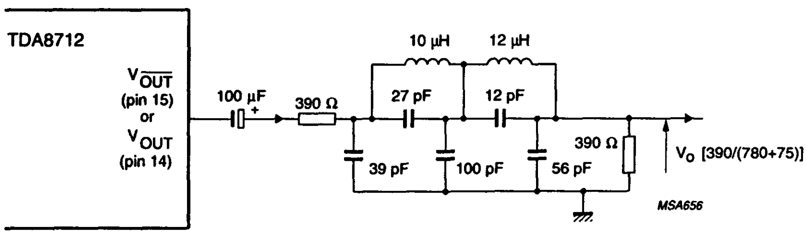
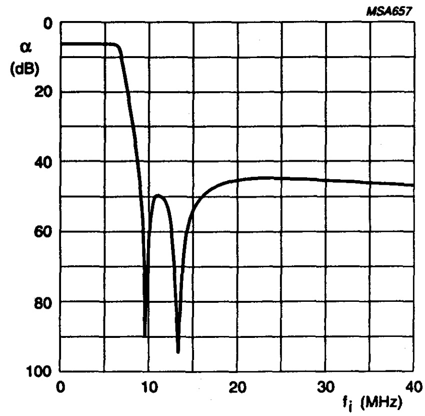


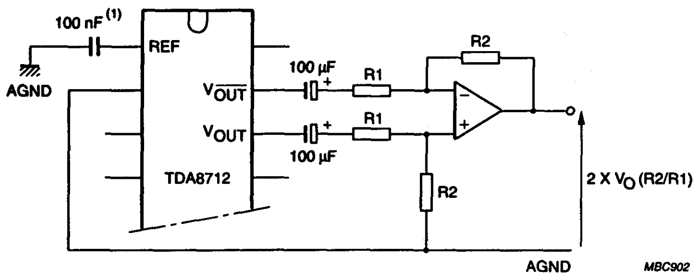
Fig.16 Example of anti-aliasing filter (analog output referenced to AGND).



Characteristics

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.1$ dB
- $f_{(-3\ dB)}$ = 6.7 MHz
- $f_{(NOTCH)}$ = 9.7 MHz and 13.3 MHz

Fig.17 Frequency response for filter shown in Fig.16.



(1) This is a recommended value for decoupling pin 1.

Fig.18 Differential mode (improved supply voltage ripple rejection).

8-bit high-speed analog-to-digital converter TDA8714

FEATURES

- 8-bit resolution
- Sampling rate up to 75 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.6 effective bits at 4.43 MHz full-scale input at a 75 MHz clock frequency.
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- External reference voltage generator
- Power dissipation only 325 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

- High-speed analog-to-digital conversion for:
  -video data digitizing
  -radar pulse analysis
  -transient signal analysis
  -high energy physics research
  -ΣΔ modulators
  -medical imaging.

DESCRIPTION

The TDA8714 is an 8-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 75 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	25	tbf	mA
I_{CCD}	digital supply current		–	20	tbf	mA
I_{CCO}	output stages supply current		–	20	tbf	mA
ILE	DC integral linearity error		–	–	±0.75	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ALE	AC integral linearity error	note 1	–	–	±2	LSB
f_{CLK}	maximum clock frequency	TDA8714/7	75	–	–	MHz
		TDA8714/6	60	–	–	MHz
		TDA8714/4	40	–	–	MHz
P_{tot}	total power dissipation		–	325	tbf	mW

Note

1. Full-scale sinewave (f_i = 4.43 MHz; f_{CLK} = 75 MHz).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				
	PINS	PIN POSITION	MATERIAL	CODE	SAMPLING FREQUENCY (MHZ)
TDA8714/4	24	DIL	plastic	SOT101	40
TDA8714T/4	24	SO24	plastic	SOT137A	40
TDA8714/6	24	DIL	plastic	SOT101	60
TDA8714T/6	24	SO24	plastic	SOT137A	60
TDA8714/7	24	DIL	plastic	SOT101	75
TDA8714T/7	24	SO24	plastic	SOT137A	75

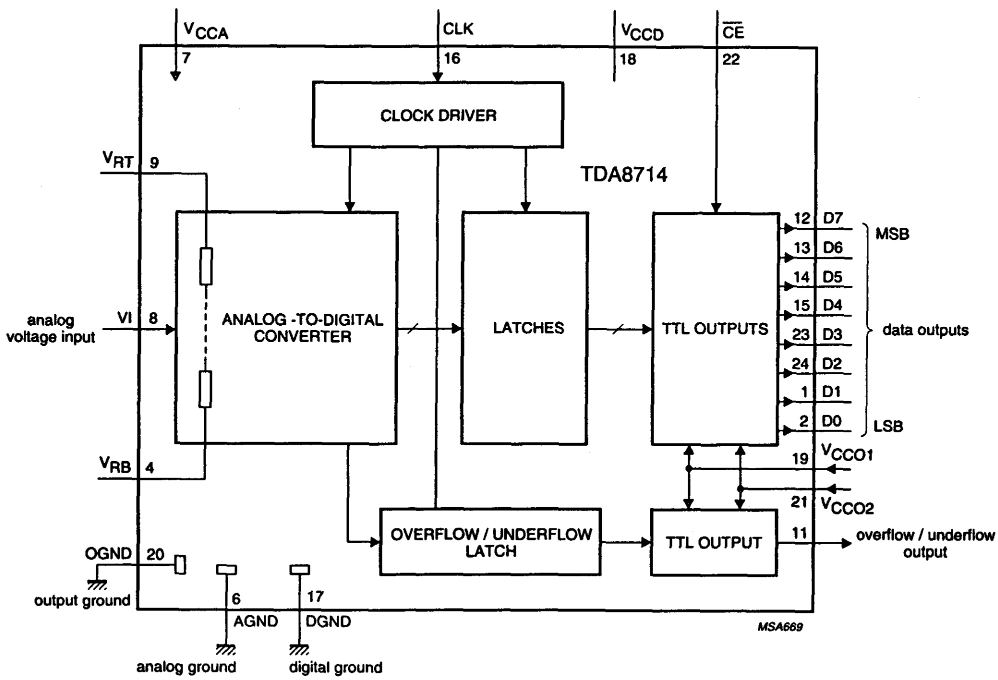


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output; bit 1
D0	2	data output; bit 0 (LSB)
n.c.	3	not connected
V_{RB}	4	reference voltage BOTTOM (decoupling)
n.c.	5	not connected
AGND	6	analog ground
V_{CCA}	7	analog supply voltage (+5 V)
VI	8	analog voltage input
V_{RT}	9	reference voltage TOP (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output; bit 7 (MSB)
D6	13	data output; bit 6
D5	14	data output; bit 5
D4	15	data output; bit 4
CLK	16	clock input
DGND	17	digital ground
V_{CCD}	18	digital supply voltage (+5 V)
V_{CCO1}	19	output stages supply voltage 1 (+5 V)
OGND	20	output ground
V_{CCO2}	21	output stages supply voltage 2 (+5 V)
$\overline{CE}$	22	chip enable input (TTL level input; active LOW)
D3	23	data output; bit 3
D2	24	data output; bit 2

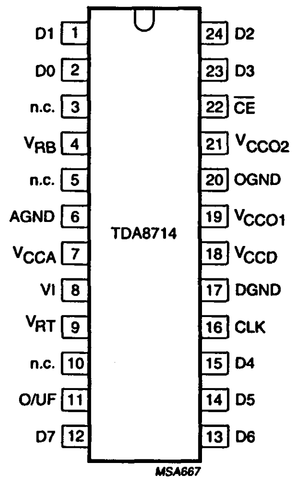


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	−0.3	7.0	V
V_{CCD}	digital supply voltage	note 1	−0.3	7.0	V
V_{CCO}	output stages supply voltage	note 1	−0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage difference		−1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage difference		−1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage difference		−1.0	1.0	V
V_{VI}	input voltage	referenced to AGND	−0.3	7.0	V
$V_{CLK(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	−	V_{CCD}	V
I_O	output current		−	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

Note

1. The supply voltages V_{CCA} and V_{CCD} may have any value between −0.3 and +7 V as long as the difference $V_{CCA} - V_{CCD}$ lies between −1 and +1 V.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	
	SOT101	55 K/W
	SOT137A	75 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_7 - V_6$ = 4.75 to 5.25 V; $V_{CCD} = V_{18} - V_{20}$ = 4.75 to 5.25 V; $V_{CCO} = V_{19} - V_{20}$ = 4.75 to 5.25 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD}$ = −0.25 to +0.25 V; $V_{CCO} - V_{CCD}$ = −0.25 to +0.25 V; $V_{CCA} - V_{CCO}$ = −0.25 to +0.25 V; T_{amb} = 0 to 75 °C; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	25	tbf	mA
I_{CCD}	digital supply current		–	20	tbf	mA
I_{CCO}	output stages supply current		–	20	tbf	mA
Inputs						
CLK (referenced to DGND); note 1						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	−400	–	–	μA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	300	μA
Z_I	input impedance	f_{CLK} = 75 MHz	–	2	–	kΩ
C_I	input capacitance	f_{CLK} = 75 MHz	–	4.5	–	pF
$\overline{CE}$ (referenced to DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{IL} = 0.4 V	−400	–	–	μA
I_{IH}	HIGH level input current	V_{IH} = 2.7 V	–	–	20	μA
VI (referenced to AGND)						
I_{IL}	LOW level input current	V_{VI} = 1.2 V	–	0	–	μA
I_{IH}	HIGH level input current	V_{VI} = 3.5 V	60	120	180	μA
Z_I	input impedance	f_i = 4.43 MHz	–	10	–	kΩ
C_I	input capacitance	f_i = 4.43 MHz	–	14	–	pF
Reference voltages for the resistor ladder						
V_{RB}	reference voltage BOTTOM		1.2	1.3	1.6	V
V_{RT}	reference voltage TOP		3.5	3.6	3.9	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		1.9	2.3	–	V
I_{REF}	reference current		–	10	–	mA
R_{LAD}	resistor ladder		–	220	–	Ω
TC_{RL}	temperature coefficient of the resistor ladder		–	0.24	–	Ω/°C
V_{OB}	voltage offset BOTTOM	note 2	–	275	–	mV
V_{OT}	voltage offset TOP	note 2	–	150	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
Digital outputs D7 to D0 (referenced to DGND)						
V_{OL}	LOW level output voltage	$I_O = 1$ mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	$I_O = -0.4$ mA	2.7	–	V_{CCD}	V
$\|I_O\|$	output current in 3-state mode	$0.4\ V < V_O < V_{CCD}$	–20	–	+20	μA
Switching characteristics; notes 1 and 2; see Fig. 3						
f_{CLK}	maximum clock frequency	TDA8714/7	75	–	–	MHz
		TDA8714/6	60	–	–	MHz
		TDA8714/4	40	–	–	MHz
t_{CPH}	clock pulse width HIGH		6	–	–	ns
t_{CPL}	clock pulse width LOW		6	–	–	ns
Analog signal processing (f_{CLK} = 40 MHz)						
G_{diff}	differential gain	note 3	–	0.3	–	%
Φ_{diff}	differential phase	note 3	–	0.4	–	deg
Harmonics (full-scale)						
f_1	fundamental	f_i = 4.43 MHz	–	–	0	dB
f_2	even	f_i = 4.43 MHz	–	70	–	dB
f_3	odd	f_i = 4.43 MHz	–	60	–	dB
Transfer function						
ILE	DC integral linearity error		–	–	±0.75	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ALE	AC integral linearity error	note 4	–	–	±2	LSB
Effective bits; note 5						
EB	TDA8714/4 (f_{CLK} = 40 MHz)	f_i = 4.43 MHz	–	7.7	–	bits
		f_i = 7.5 MHz	–	7.4	–	bits
	TDA8714/6 (f_{CLK} = 60 MHz)	f_i = 4.43 MHz	–	7.65	–	bits
		f_i = 7.5 MHz	–	7.35	–	bits
	TDA8714/7 (f_{CLK} = 75 MHz)	f_i = 4.43 MHz	–	7.6	–	bits
		f_i = 7.5 MHz	–	7.3	–	bits
		f_i = 10 MHz	–	7.0	–	bits
BER	bit error rate	f_{CLK} = 75 MHz; f_i = 4.43 MHz; V_i = ±8 LSB at code 128; 50% clock duty cycle	–	10^{-11}	–	times/ samples

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (f_{CLK} = 75 MHz; note 6; see Figs 3 to 5)						
t_{ds}	sampling delay		–	–	2	ns
t_{HD}	output hold time		5	–	–	ns
t_d	output delay time		–	10	13	ns
t_{dZ}	3-state output delay times	enable-to-HIGH	–	19	tbf	ns
		enable-to-LOW	–	16	tbf	ns
		disable-to-HIGH	–	14	tbf	ns
		disable-to-LOW	–	9	tbf	ns
t_{aj}	aperture jitter		–	50	–	ps

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Analog input voltages producing code 00 up to and including FF
   - V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C.
   - V_{OBTC} (voltage offset bottom temperature coefficient) is the dependence of V_{OB} with temperature.
   - V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
   - V_{OTTC} (voltage offset top temperature coefficient) is the dependence of V_{OT} with temperature.
3. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
4. Full-scale sinewave (f_i = 4.43 MHz; f_{CLK} = 75 MHz).
5. Effective bits are obtained via a Fast Fourier Transformer (FFT) treatment taking 4K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST) frequency).
   Conversion to SNR: SNR (dB) = EB x 6.02 + 1.76.
6. Output data acquisition;
   - Output data is available after the maximum delay t_d.
   - In the event of 75 MHz clock operation, the hardware design must take into account the t_d and t_{HD} limits with respect to the input characteristics of the acquisition circuit.

Table 1 Output coding and input voltage (typical values; referenced to AGND, V_{RB} = 1.3 V, V_{RT} = 3.6 V).

			BINARY OUTPUT BITS							
STEP	$V_{VI(P-P)}$	O/UF	D7	D6	D5	D4	D3	D2	D1	D0
underflow	< 1.575	1	0	0	0	0	0	0	0	0
0	1.575	0	0	0	0	0	0	0	0	0
1	.	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0
255	3.450	0	1	1	1	1	1	1	1	1
overflow	> 3.450	1	1	1	1	1	1	1	1	1

Table 2 Mode selection.

$\overline{CE}$	D7 to D0	O/UF
1	high impedance	high impedance
0	active; binary	active

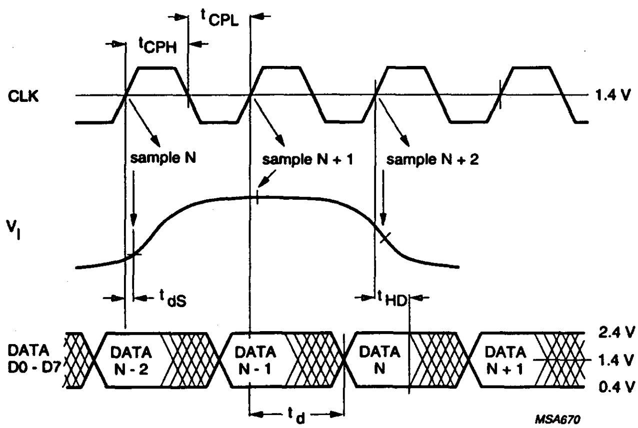


Fig.3 Timing diagram.

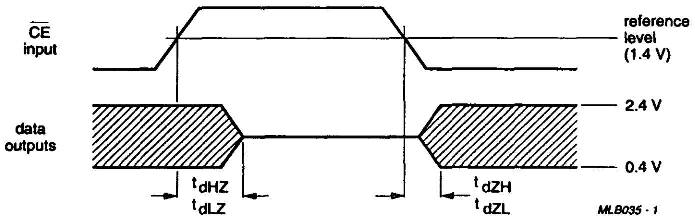


Fig.4 3-state delay timing diagram.

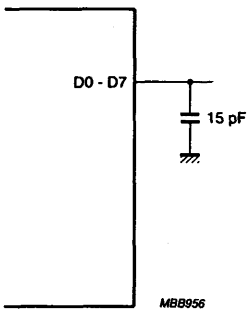


Fig.5 Load circuit for timing measurement.

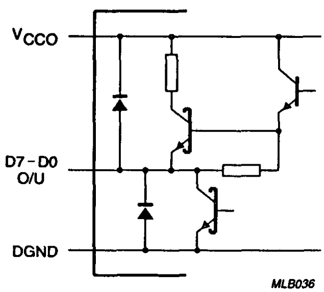


Fig.6 TTL data and overflow/underflow outputs.

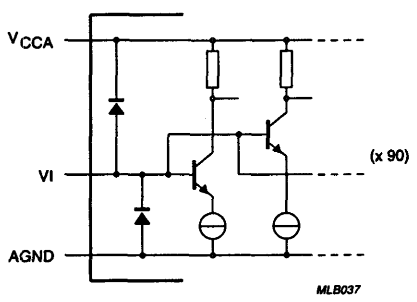


Fig.7 Analog inputs.

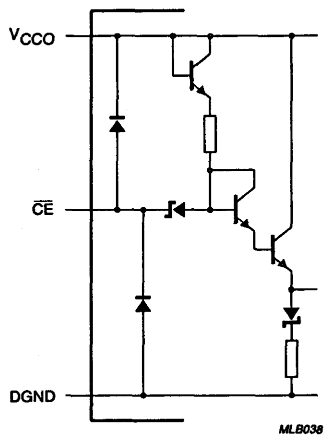


Fig.8 $\overline{CE}$ (3-state) input.

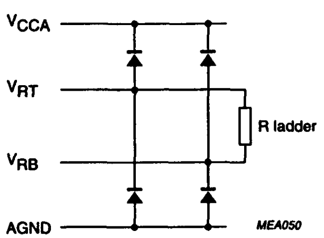


Fig.9 V_{RB}, V_{RT}.

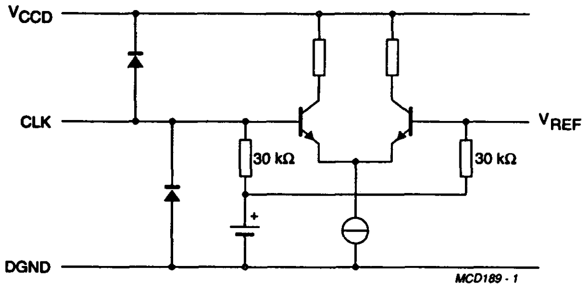
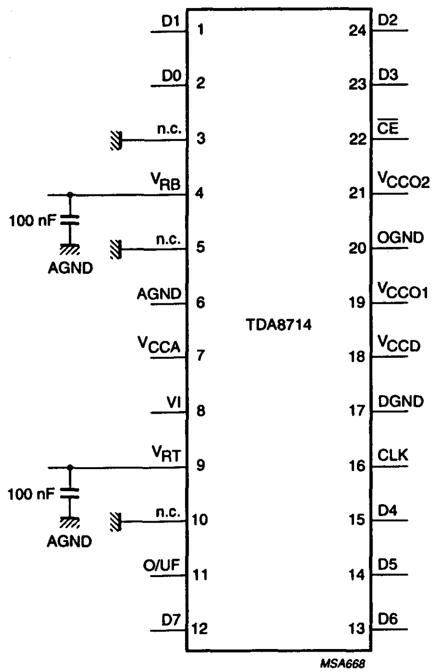


Fig.10 CLK input.

APPLICATION INFORMATION



(1) V_{RB} and V_{RT} are decoupled to AGND.
(2) Analog and digital supplies should be separated and decoupled.
(3) Pins 5 should be connected to AGND and pins 3 and 10 to DGND in order to prevent noise influence.
(4) The external voltage regulator must be build in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.

Fig.11 Application diagram.

8-bit high-speed analog-to-digital converter

TDA8715

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.5 effective bits at 4.43 MHz full-scale input at a 40 MHz clock frequency)
- ECL (10KH family) compatible digital inputs and outputs
- Overflow/underflow ECL output
- Low-level AC clock input signal allowed
- Power dissipation only 325 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - video data digitizing
  - radar pulse analysis
  - transient signal analysis
  - high energy physics research
  - ΣΔ modulators
  - medical imaging.

GENERAL DESCRIPTION

The TDA8715 is a bipolar 8-bit high-speed analog-to-digital converter (ADC) for profesional video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are 10KH ECL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		−4.7	−5.2	−5.7	V
V_{EED}	digital supply voltage		−4.7	−5.2	−5.7	V
I_{EEA}	analog supply current		−	20	25	mA
I_{EED}	digital supply current	see note 1	−	52	60	mA
ILE	DC integral linearity error		−	±0.4	±0.75	LSB
DLE	DC differential linearity error		−	±0.25	±0.5	LSB
EB	effective bits	f_i = 4.43 MHz; f_{CLK} = 50 MHz	−	7.2	−	bits
f_{CLK}; $f_{\overline{CLK}}$	maximum clock frequency		50	−	−	MHz
T_{amb}	operating ambient temperature		0	−	+125	°C
P_{tot}	total power dissipation	see note 1	−	325	425	mW

Note

1. All digital outputs are connected to V_{EED} via 2.2 kΩ resistors.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8715	18	DIL	plastic	SOT102
TDA8715T	20	SO20	plastic	SOT163A

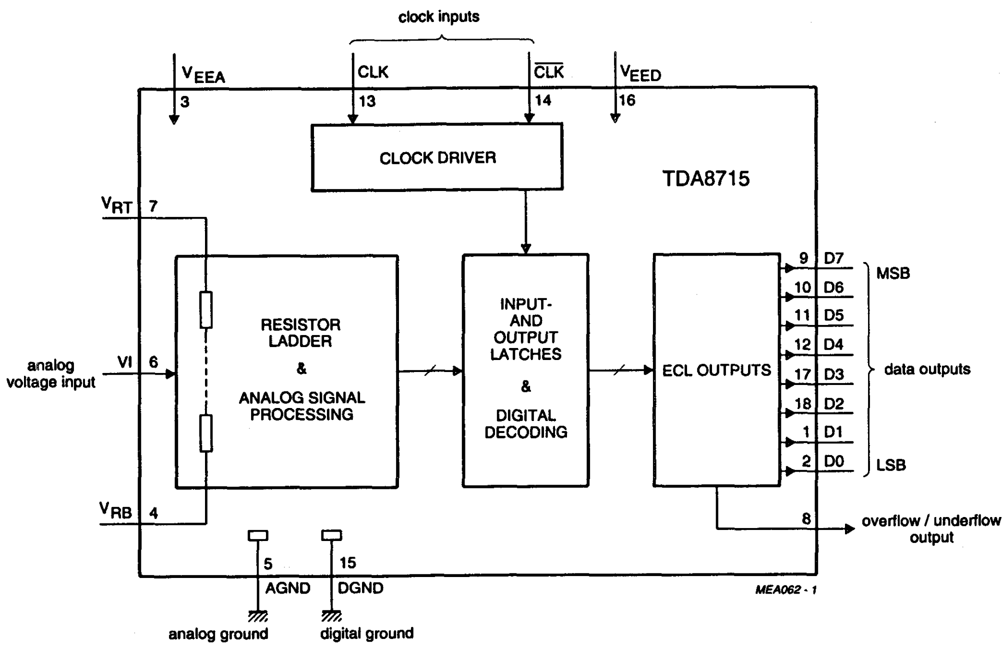


Fig.1 Block diagram.

PINNING

SYMBOL	DIL18	SO20	DESCRIPTION
D1	1	1	data output; bit 1
D0	2	2	data output; bit 0 (LSB)
n.c.	–	3	not connected
V_{EEA}	3	4	analog negative supply voltage (–5.2 V)
V_{RB}	4	5	reference voltage bottom input
AGND	5	6	analog ground
VI	6	7	analog voltage input
V_{RT}	7	8	reference voltage top input
O/UF	8	9	overflow/underflow data output
D7	9	10	data output; bit 7(MSB)
D6	10	11	data output; bit 6
D5	11	12	data output; bit 5
D4	12	13	data output; bit 4
CLK	13	14	clock input
$\overline{CLK}$	14	15	complementary clock input
DGND	15	16	digital ground
V_{EED}	16	17	digital negative supply voltage (–5.2 V)
n.c.	–	18	not connected
D3	17	19	data output; bit 3
D2	18	20	data output; bit 2

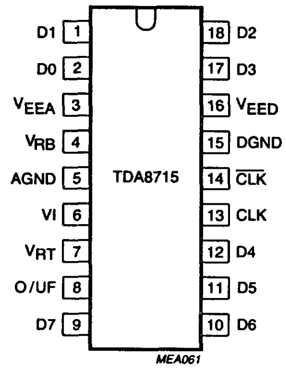


Fig.2 Pin configuration; TDA8715.

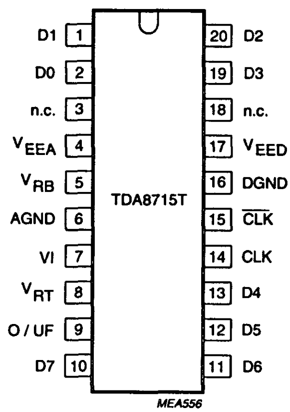


Fig.3 Pin configuration; TDA8715T.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage		−7	0.3	V
V_{EED}	digital supply voltage		−7	0.3	V
VI	analog input voltage		−7	0.3	V
V_{CLK}; $V_{\overline{CLK}}$	AC input voltage for switching (peak-to-peak value)	see note 1	−	2.0	V
I_O	output current		−15	+10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

Note

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

   Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals or with two complementary sinewave signals, imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal

   Asymmetrical drive modes; When driving the CLK input directly with an ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal

   When driving the CLK input with an ECL signal only (Asymmetrical drive modes), it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT102	65 K/W
	SOT163A	80 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{EEA} = V_3 - V_5 = -4.7$ V to -5.7 V; $V_{EED} = V_{16} - V_{15} = -4.7$ V to -5.7 V; AGND and DGND shorted together; $T_{amb} = 0$ °C to +70 °C; unless otherwise specified (typical values measured at $V_{EEA} = -5.2$V; $V_{EED} = -5.2$ V and $T_{amb} = 25$ °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EEA}	analog supply voltage		−4.7	−5.2	−5.7	V
V_{EED}	digital supply voltage		−4.7	−5.2	−5.7	V
I_{EEA}	analog supply current		–	20	25	mA
I_{EED}	digital supply current	note 1	–	52	60	mA
$V_{EEA}-V_{EED}$	supply voltage difference		−0.5	0	+0.5	V
Reference voltages for the resistor ladder						
V_{RB}	LOW level reference voltage		−3.2	−3.0	−2.7	V
V_{RT}	HIGH level reference voltage		−0.9	−0.6	−0.4	V
V_{REF}	differential reference voltage $V_{RT}-V_{RB}$		2.3	2.4	–	V
I_{REF}	reference current		–	12.6	–	mA
R_{LAD}	resistor ladder		–	200	–	Ω
TC_{RL}	temperature coefficient of the ladder		–	0.24	–	Ω/K
V_{OB}	voltage offset bottom	note 2	–	280	–	mV
TC_{VOB}	temperature coefficient voltage offset bottom	note 2	–	0.1	–	mV/K
V_{OT}	voltage offset top	note 2	–	245	–	mV
TC_{VOT}	temperature coefficient voltage offset top	note 2	–	0.1	–	mV/K
Inputs						
CLK INPUT (NOTE 3)						
V_{IL}	LOW level input voltage		−1.85	−1.77	−1.65	V
V_{IH}	HIGH level input voltage		−0.96	−0.88	−0.81	V
I_{IL}	LOW level input current	$V_{CLK} = -1.77$ V	–	−240	–	µA
I_{IH}	HIGH level input current	$V_{CLK} = -0.88$ V	–	−14	–	µA
R_I	input resistance					
		$f_{CLK} = 10$ MHz	–	7	–	kΩ
		$f_{CLK} = 50$ MHz	–	3.5	–	kΩ
C_I	input capacitance					
		$f_{CLK} = 10$ MHz	–	1.8	–	pF
		$f_{CLK} = 50$ MHz	–	1.55	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\overline{CLK}$ INPUT (NOTE 3)						
V_{IL}	LOW level input voltage		−1.85	−1.77	−1.65	V
V_{IH}	HIGH level input voltage		−0.96	−0.88	−0.81	V
I_{IL}	LOW level input current	$V_{\overline{CLK}}$ = −1.77 V	−	−140	−	μA
I_{IH}	HIGH level input current	$V_{\overline{CLK}}$ = −0.88 V	−	75	−	μA
R_I	input resistance					
		$f_{\overline{CLK}}$ = 10 MHz	−	9.3	−	kΩ
		$f_{\overline{CLK}}$ = 50 MHz	−	4.5	−	kΩ
C_I	input capacitance					
		$f_{\overline{CLK}}$ = 10 MHz	−	2.6	−	pF
		$f_{\overline{CLK}}$ = 50 MHz	−	2.4	−	pF
$V_{CLK} - V_{\overline{CLK}}$	AC input voltage for switching (peak-to-peak value)		0.5	0.9	1.1	V
V_I (ANALOG INPUT; V_{RB} = −3.1 V AND V_{RT} = −0.6 V)						
I_{IL}	LOW level input current	data output 00	−	0	−	μA
I_{IH}	HIGH level input current	data output FF	−	120	−	μA
R_I	input resistance	f_i = 1 MHz	−	9.4	−	kΩ
C_I	input capacitance	f_i = 1 MHz	−	13.7	20	pF
Outputs						
DIGITAL OUTPUTS (D7 TO D0 AND O/UF; DIGITAL 10KH ECL OUTPUTS)						
V_{OL}	LOW level output voltage	T_{amb} = 25 °C	−1.95	−1.77	−1.65	V
V_{OH}	HIGH level output voltage	T_{amb} = 25 °C	−0.96	−0.88	−0.81	V
I_{OL}	LOW level output current		−	1.8	4	mA
I_{OH}	HIGH level output current		−	1.8	4	mA
Switching characteristics						
f_{CLK}; $f_{\overline{CLK}}$	maximum clock frequency		50	−	−	MHz
Analog signal processing (f_{CLK} = 50 MHz)						
B	−3 dB bandwidth	note 4	−	20.5	−	MHz
G_{diff}	differential gain	note 5	−	0.3	2.0	%
Φ_{diff}	differential phase	note 5	−	0.4	1.5	deg
	harmonics (full-scale)	f_i = 4.43 MHz				
	fundamental		0	0	0	dB
	even		−	−60	−	dB
	odd		−	−50	−	dB
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		−	−	±0.75	LSB
DLE	DC differential linearity error		−	−	±0.5	LSB
AILE	AC integral linearity error	note 6	−	±0.75	−	LSB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EB	effective bits					
	f_i = 600 kHz	f_{CLK} = 20 MHZ	–	7.8	–	bits
	f_i = 4.43 MHz	f_{CLK} = 50 MHZ	–	7.2	–	bits
	f_i = 7 MHz	f_{CLK} = 50 MHZ	–	6.9	–	bits
Timing (note 7; see Fig.4; R_L 2.2 kΩ, C_L = 7.5 pF)						
t_{ds}	sampling delay		–	1	3	ns
t_{HD}	output hold time		3	4	–	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	–	7	10	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	–	10	13	ns

Notes

1. All digital outputs connected to V_{EED} via 2.2 kΩ resistors.
2. Analog input voltages producing code 00 up to and including FF

   V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C

   TC_{VOB} (voltage offset bottom temperature coefficient) is dependent on V_{OB} with temperature

   V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C

   TC_{VOT} (voltage offset top temperature coefficient) is dependent on V_{OT} with temperature.
3. The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

   Differential drive modes; when driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals or with two complementary sinewave signals, imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal

   Asymmetrical drive modes; when driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal

   When driving the CLK input with a ECL signal only (asymmetrical drive modes), it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connect to V_{EED} by a 150 kΩ resistor.
4. The −3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
5. Low frequency ramp signal ($V_{I(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{I(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
6. Full-scale sinewave (f_i = 4.43 MHz; f_{CLK}; $f_{\overline{CLK}}$ = 50 MHz).
7. Output data acquisition

   Output data is available after the maximum delay of t_{dHL} and t_{dLH}

   TDA8715 can withstand only one or two 10K ECL loads in order to work out timing at maximum sampling frequency. It is recommended to minimize the PCB load by implementing the load device as close as possible to the TDA8715.

Table 1 Output coding.

STEP	VI (TYP. VALUE)	BINARY OUTPUTS D7 to D0	$\overline{O}$/UFL
Underflow	< −2.789 V	00000000	1
0	−2.783 V	00000000	0
1	−2.775 V	00000001	0
.	.	....	.
.	.	....	.
.	.	....	.
254	.	11111110	0
255	−0.774 V	11111111	0
Overflow	> −0.770 V	11111111	1

Note to Table 1

Typical values: V_{RB} = −3 V, V_{RT} = −0.6 V and VI referenced to AGND.

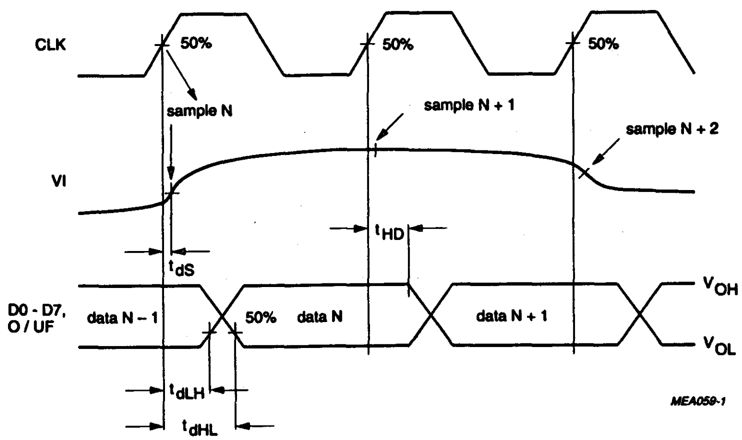


Fig.4 Timing diagram.

INTERNAL PIN CIRCUITRY

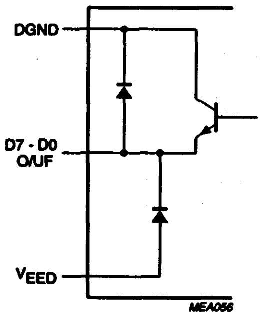


Fig.5 ECL data outputs.

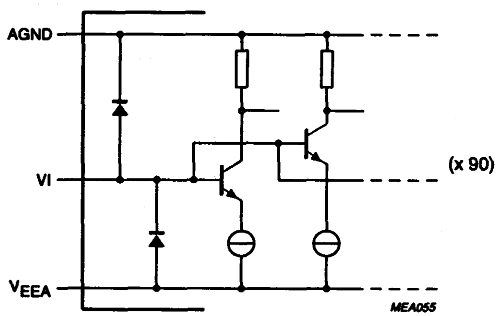


Fig.6 Analog input.

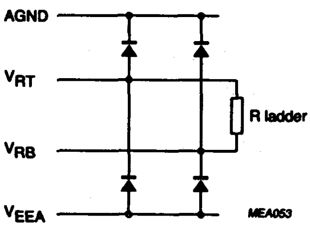


Fig.7 V_{RT} and V_{RB} inputs.

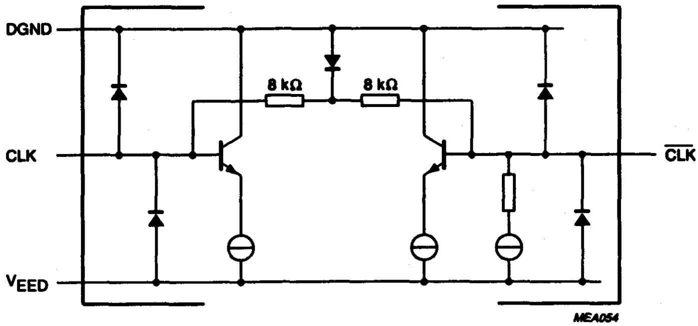
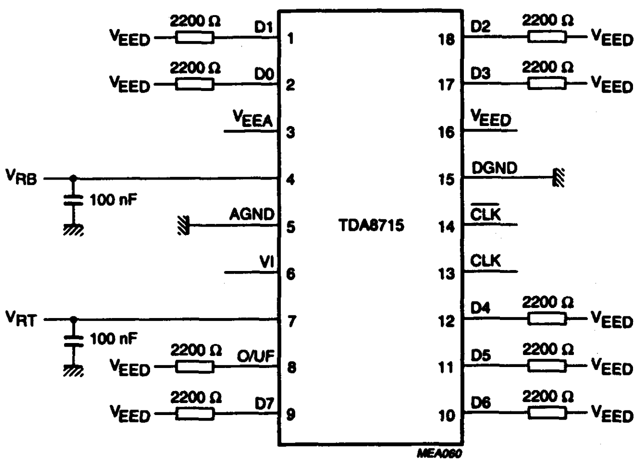


Fig.8 CLK and $\overline{CLK}$ input.

APPLICATION INFORMATION



1. Analog and digital supplies should be separated and decoupled.
2. The external voltage regulator should be configured in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.
3. In the event of a capacitive output load, it is recommended to implement a 22 Ω resistor in series with V_{EED} (pin 16).

Fig.9 Application diagram.

8-bit high-speed analog-to-digital converter

TDA8716

FEATURES

- 8-bit resolution
- Sampling rate up to 120 MHz
- ECL (10 K family) compatible digital inputs and outputs
- Overflow/Underflow output
- Low power dissipation
- Low input capacitance (13 pF typ.).

APPLICATIONS

- High speed analog-to-digital convertion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research
- Medical systems
- Industrial instrumentation.

GENERAL DESCRIPTION

The TDA8716 is an 8-bit high-speed analog-to-digital converter (ADC) designed for HDTV and professional applications. The device converts the analog input signal into 8-bit binary coded digital words at a sampling rate of 120 MHz. All digital outputs are ECL compatible.

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		−5.45	−5.2	−4.95	V
V_{EED}	digital supply voltage		−5.45	−5.2	−4.95	V
I_{EEA}	analog supply current		−	50	55	mA
I_{EED}	digital supply current		−	100	110	mA
I_{EEO}	output supply current	R_L = 2.2 kΩ	−	20	25	mA
V_{RB}	reference voltage BOTTOM		−	−3.130	−	V
V_{RT}	reference voltage TOP		−	−1.870	−	V
ILE	DC integral linearity error	see Fig.8	−	±0.5	±1	LSB
DLE	DC differential linearity error	see Fig.9	−	±0.25	±0.45	LSB
EB	effective bit	f_i = 20 MHz; f_{CLK} = 100 MHz	−	7	−	bits
f_{CLK}	maximum clock frequency		120	−	−	MHz
P_{tot}	total power dissipation	excluding load	−	780	900	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8716	24	DIL	plastic	SOT101
TDA8716T	32	SO32L	plastic	SOT287

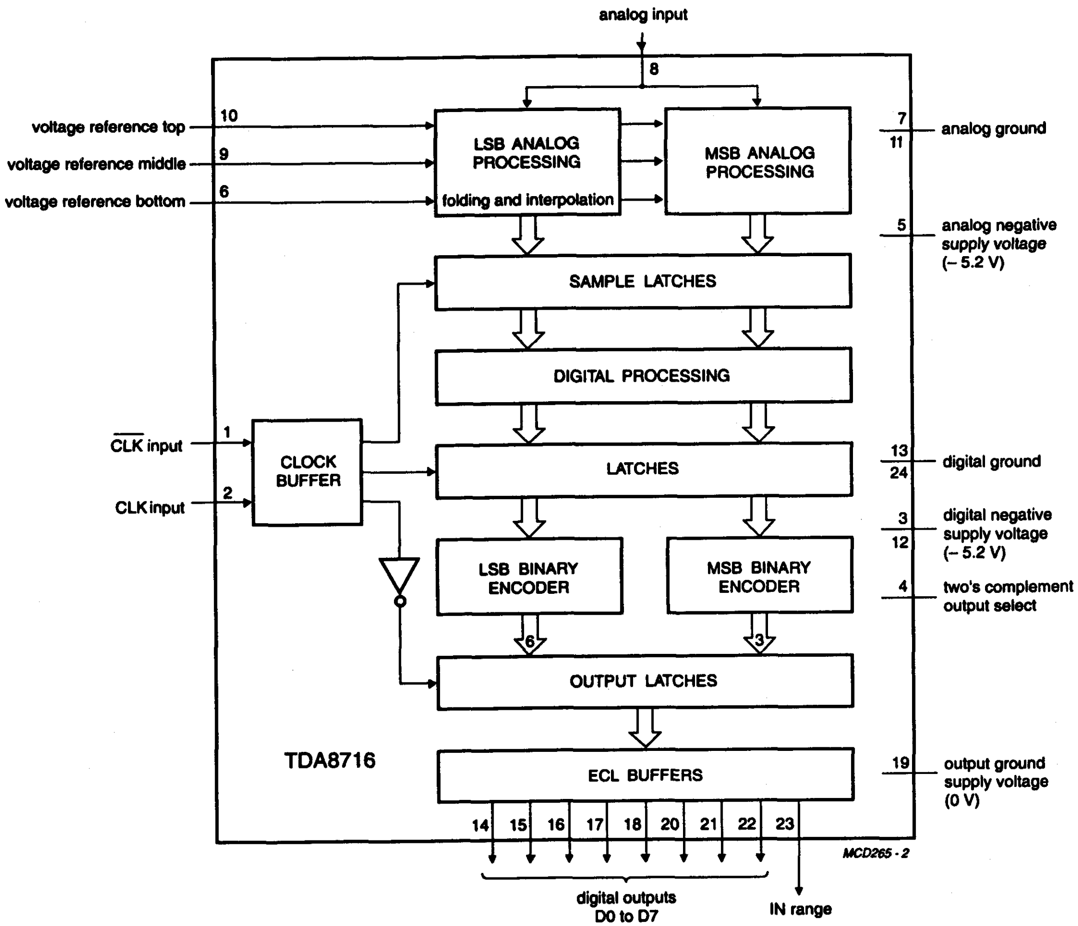


Fig.1 Block diagram; TDA8716.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{CLK}$	1	complementary clock input
CLK	2	clock input
V_{EED1}	3	digital negative supply voltage (−5.2 V)
C_{PLT2}	4	two's complement output select (active HIGH)
V_{EEA}	5	analog negative supply voltage (−5.2 V)
V_{RB}	6	reference voltage BOTTOM
AGND1	7	analog ground 1
V_I	8	analog input
V_{RM}	9	reference voltage MIDDLE decoupling
V_{RT}	10	reference voltage TOP
AGND2	11	analog ground 2
V_{EED2}	12	digital negative supply voltage (−5.2 V)
DGND1	13	digital ground 1
D0	14	digital output (LSB)
D1	15	digital output
D2	16	digital output
D3	17	digital output
D4	18	digital output
OGND	19	output ground supply voltage (0 V)
D5	20	digital output
D6	21	digital output
D7	22	digital output (MSB)
IR	23	IN range
DGND2	24	digital ground 2

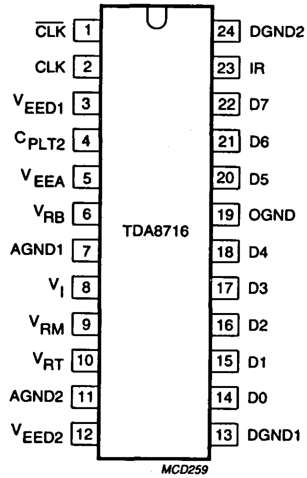


Fig.2 Pin configuration; TDA8716.

8-bit high-speed analog-to-digital converter

TDA8716

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{CLK}$	1	complementary clock input
CLK	2	clock input
V_{EED1}	3	digital negative supply voltage (−5.2 V)
n.c.	4	not connected
n.c.	5	not connected
C_{PLT2}	6	two's complement output select (active HIGH)
V_{EEA}	7	analog negative supply voltage (−5.2 V)
V_{RB}	8	reference voltage BOTTOM
AGND1	9	analog ground 1
V_I	10	analog input
V_{RM}	11	reference voltage MIDDLE decoupling
n.c.	12	not connected
n.c.	13	not connected
V_{RT}	14	reference voltage TOP
AGND2	15	analog ground 2
V_{EED2}	16	digital negative supply voltage (−5.2 V)
DGND1	17	digital ground 1
D0	18	digital output (LSB)
D1	19	digital output
n.c.	20	not connected
n.c.	21	not connected
D2	22	digital output
D3	23	digital output
D4	24	digital output
OGND	25	output ground supply voltage (0 V)
D5	26	digital output
D6	27	digital output
n.c.	28	not connected
n.c.	29	not connected
D7	30	digital output (MSB)
IR	31	IN range
DGND2	32	digital ground 2

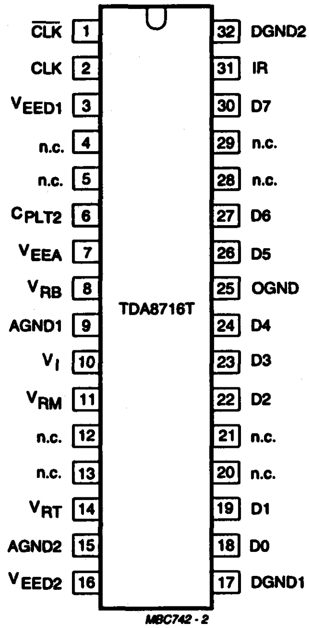


Fig.3 Pin configuration; TDA8716T.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage		−7.0	+0.3	V
V_{EED1}, V_{EED2}	digital supply voltage		−7.0	+0.3	V
$V_{EEA}-V_{EED1}$; $V_{EEA}-V_{EED2}$	supply voltage differences		−1	+1	V
V_I	input voltage	referenced to AGND	V_{EEA}	0	V
$V_{CLK;\ \overline{CLK}(p-p)}$	input voltage for differential clock drive (peak-to-peak value)	note 1	−	2.0	V
I_O	output current (each output stage)		−	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

Note

1. The circuit has two clock inputs: CLK and $\overline{CLK}$. Sampling takes place on the rising edge of the clock input signal: CLK and $\overline{CLK}$ are two's complementary ECL signals.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT101	35 K/W
	SOT287 (see Fig.4)	65 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

V_{EEA} = –4.95 V to –5.45 V; V_{EED1}, V_{EED2} = –4.95 V to –5.45 V; AGND, DGND and OGND shorted together; T_{amb} = 0 °C to +70°C; unless otherwise specified. (Typical values taken at V_{EEA} = –5.2 V; V_{EED1}, V_{EED2} = –5.2 V; T_{amb} = 25 °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EEA}	analog supply voltage		–5.45	–5.2	–4.95	V
V_{EED1}, V_{EED2}	digital supply voltage		–5.45	–5.2	–4.95	V
I_{EEA}	analog supply current		–	50	55	mA
I_{EED1}, I_{EED2}	digital supply current		–	100	110	mA
I_{EE}	output supply current	R_L = 2.2 kΩ	–	20	25	mA
V_{diff}	supply voltage differential	$V_{EEA} - V_{EED1}$; $V_{EEA} - V_{EED2}$	–0.5	0	+0.5	V
Reference voltages for the resistor ladder						
V_{RB}	reference voltage BOTTOM		–3.5	–3.13	–	V
V_{RT}	reference voltage TOP		–	–1.87	–1.5	V
V_{ref}	reference voltage differential	$V_{RT} - V_{RB}$	–	1.26	–	V
V_{OB}	voltage offset BOTTOM	note 1	–	130	–	mV
V_{OT}	voltage offset TOP	note 1	–	130	–	mV
$V_{I(p-p)}$	input voltage amplitude (peak-to-peak value)		0.95	1.0	1.5	V
I_{ref}	reference current		–	15	–	mA
R_{LAD}	resistor ladder		–	85	–	Ω
TC_{RL}	temperature coefficient of the resistor ladder		–	0.18	–	Ω/K
Inputs						
CLK and $\overline{CLK}$ input						
V_{IL}	LOW level input voltage		–1850	–1770	–1650	mV
V_{IH}	HIGH level input voltage		–960	–880	–810	mV
I_{IL}	LOW level input current	V_{CLK} = –1.77 V	–	1	–	μA
I_{IH}	HIGH level input current	V_{CLK} = –0.88 V	–	10	–	μA
R_I	input resistance		–	20	–	kΩ
C_I	input capacitance		–	2	–	pF
$V_{CLK(p-p)}$	differential clock input $V_{CLK} - V_{\overline{CLK}}$ (peak-to-peak value)		–	900	–	mV
Analog input; note 2						
I_{IB}	input current BOTTOM	V_{RB} = –3.13 V	–	0	–	μA
I_{IT}	input current TOP	V_{RT} = –1.87 V	–	170	–	μA
R_I	input resistance		–	7	–	kΩ
C_I	input capacitance		–	13	20	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs (R_L = 2.2 kΩ)						
Digital 10K ECL outputs (D0 to D7; IR)						
V_{OL}	LOW level output voltage		−1850	−1770	−1600	mV
V_{OH}	HIGH level output voltage		−960	−880	−810	mV
I_{OL}	LOW level output current		−	1.8	4.0	mA
I_{OH}	HIGH level output current		−	2.0	4.0	mA
Timing (f_{CLK} = 100 MHz; R_L = 2.2 kΩ; see Fig.5)						
t_{ds}	sampling delay		−	1	3	ns
t_{HD}	output hold time		4	−	−	ns
t_d	output delay time	note 3				
		C_L = 3.3 pF	−	−	7.5	ns
		C_L = 7.5 pF	−	−	9	ns
t_{aj}	aperture jitter		−	15	−	ps
Switching characteristics						
f_{CLK}; $f_{\overline{CLK}}$	maximum clock frequency		120	−	−	MHz
Analog signal processing (f_{CLK} = 100 MHz)						
G_{diff}	differential gain	note 4	−	0.3	−	%
ϕ_{diff}	differential phase	note 4	−	0.4	−	°C
Harmonics (full scale); f_i = 10 MHz; f_{CLK} = 100 MHz						
f1	fundamental		−	0	−	dB
f2	even harmonics		−	−60	−	dB
f3	odd harmonics		−	−50	−	dB
Transfer function						
ILE	DC integral linearity error		−	±0.5	±1	LSB
DLE	DC differential linearity error		−	±0.25	±0.45	LSB
AILE	AC integral linearity error	note 4	−	±1	±1.5	LSB
EB	effective bits	Figs 13 and 14; note 5; f_{CLK} = 100 MHz				
	f_i = 4.43 MHz	Fig.10	-	7.7	−	bits
	f_i = 10 MHz	Fig.11	-	7.5	−	bits
	f_i = 20 MHz	Fig.12	-	7.0	−	bits
	f_i = 30 MHz		-	6.5	−	bits
BER	bit error rate	f_{CLK} = 100 MHz; f_i = 10 MHz; V_i = ±8 LSB at code 128; 50% clock duty cycle	−	10^{-11}	−	times/samples

Notes

1. Voltage offset BOTTOM (V_{OB}) is the difference between the analog input which produces data outputs equal to 00 and the reference voltage BOTTOM (V_{RB}), at T_{amb} = 25 °C. Voltage offset TOP (V_{OT}) is the difference between reference voltage TOP (V_{RT}) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
2. The analog input is not internally biased. It should be externally biased between V_{RB} and V_{RT} levels.
3. The TDA8716 can only withstand one or two 10K or 100K ECL loads in order to work-out timings at the maximum sampling frequency. It is therefore recommended to minimize the printed-circuit board load by implementing the load device as close as possible to the TDA8716.
4. Full-scale sinewave; f_i = 4.43 MHz; f_{CLK}, $f_{\overline{CLK}}$ = 100 MHz.
5. Effective bits are obtained via a Fast Fourier Transformer (FFT) treatment taking 4 K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to SNR: SNR = EB (dB) x 6.02 + 1.76.

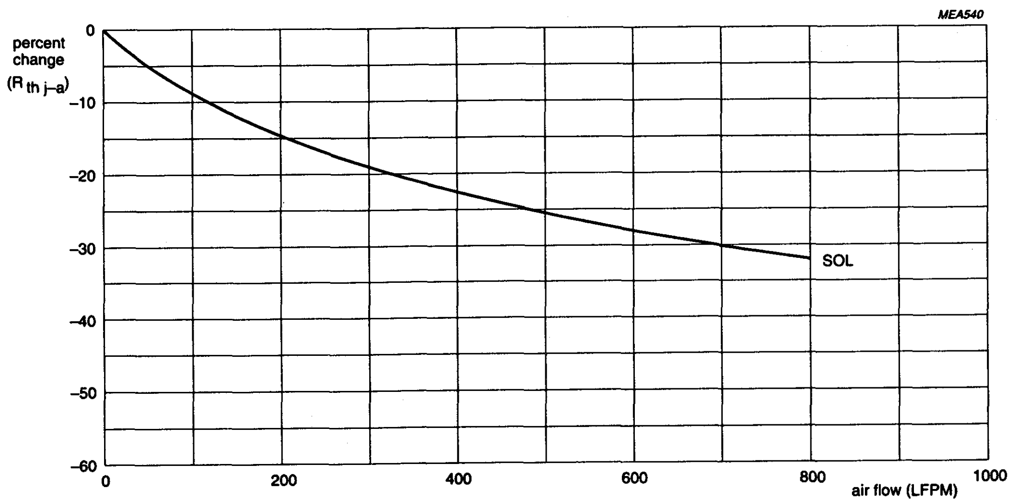


Fig.4 Average effect of air flow on thermal resistance.

Table 1 Output coding (CPLT2 HIGH).

STEP	V_I (TYP.)	BINARY OUTPUTS D7 to D0	IR
Underflow	< −3 V	00000000	0
0	−3 V	00000000	1
1	.	00000001	1
.	.	......	.
.	.	......	.
.	.	......	.
254	.	11111110	1
255	−2 V	11111111	1
Overflow	> −2 V	11111111	0

Table 2 Two's complement coding.

C_{PLT2}	D7 (MSB)
1 (V_{IH})	non inverted
0 (V_{IL})	inverted

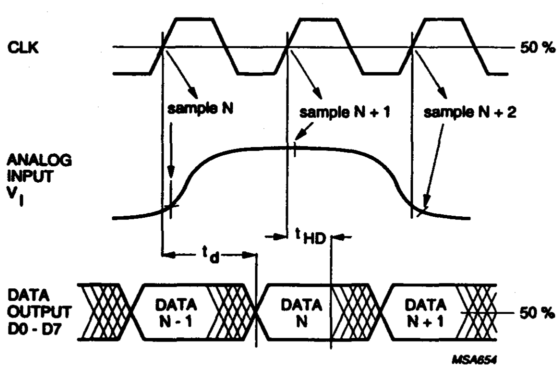


Fig.5 Timing diagram.

APPLICATION INFORMATION

Additional application information will be supplied upon request, please quote reference number FTV/AN 9109.

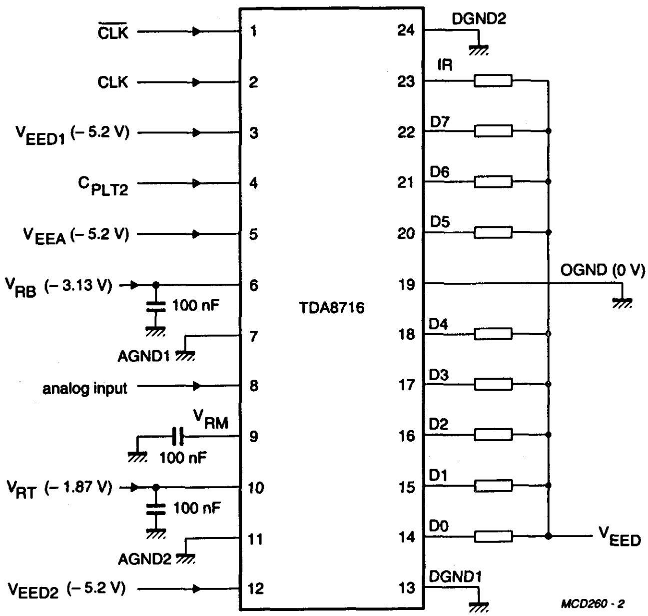


Fig.6 Application diagram; TDA8716.

Notes to Fig.6

1. Typical value for resistors = 2.2 kΩ.
2. Lower resistor values can be used down to 500 Ω to obtain higher sampling frequencies in the 150 MSPS range (limited by t_d and t_{HD} timings). In this configuration a DC shift of the ECL output levels V_{OL} and V_{OH} will occur.
3. V_{RB}, V_{RT} and V_M are decoupled to AGND.
4. Analog, digital and output supplies should be separated and decoupled.
5. The external voltage regulator must be constructed in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.

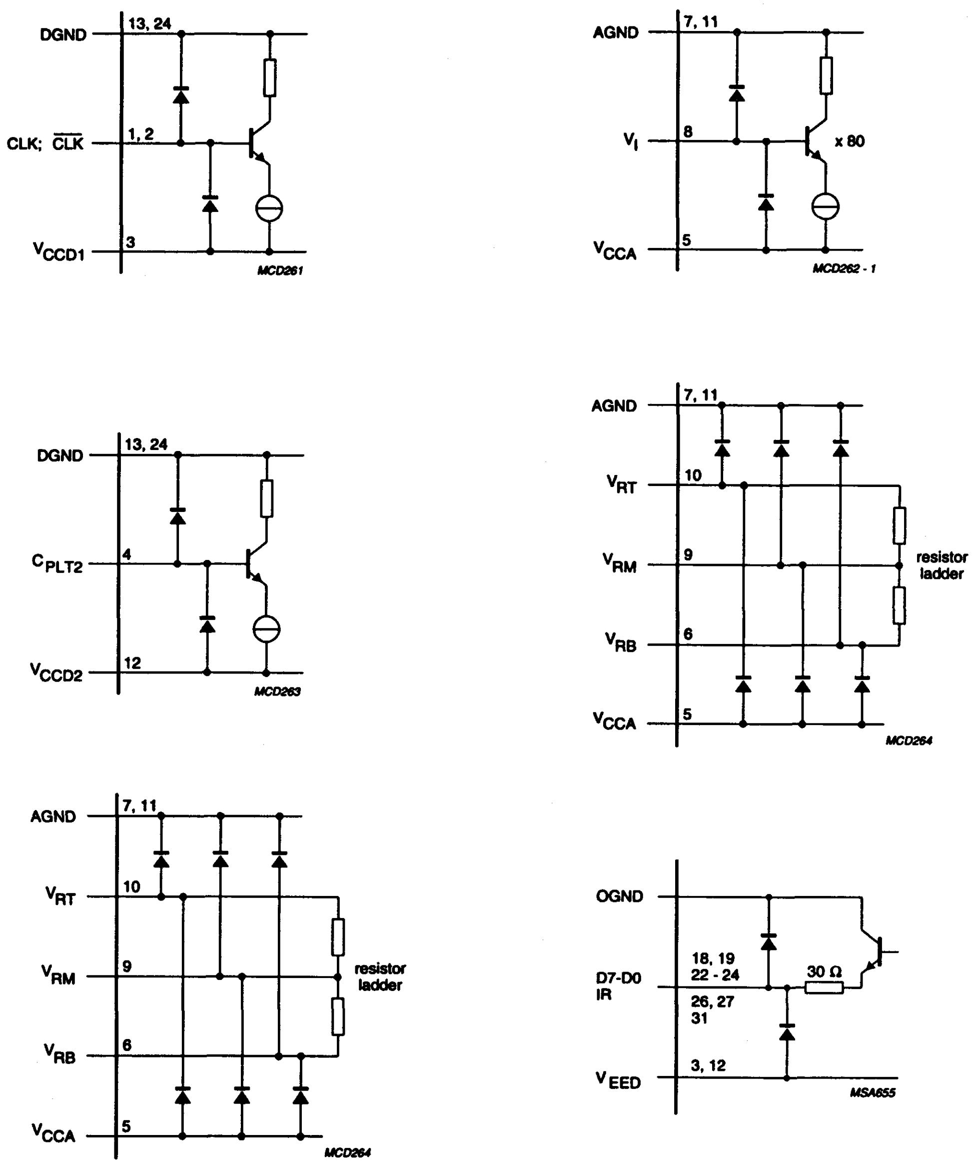


Fig.7 Internal pin configuration diagram.

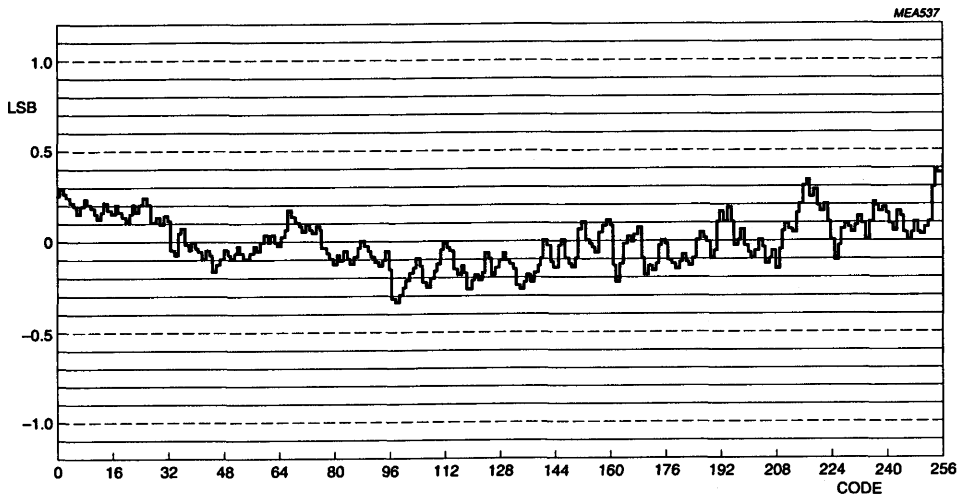


Fig.8 DC Integral linearity error (ILE).

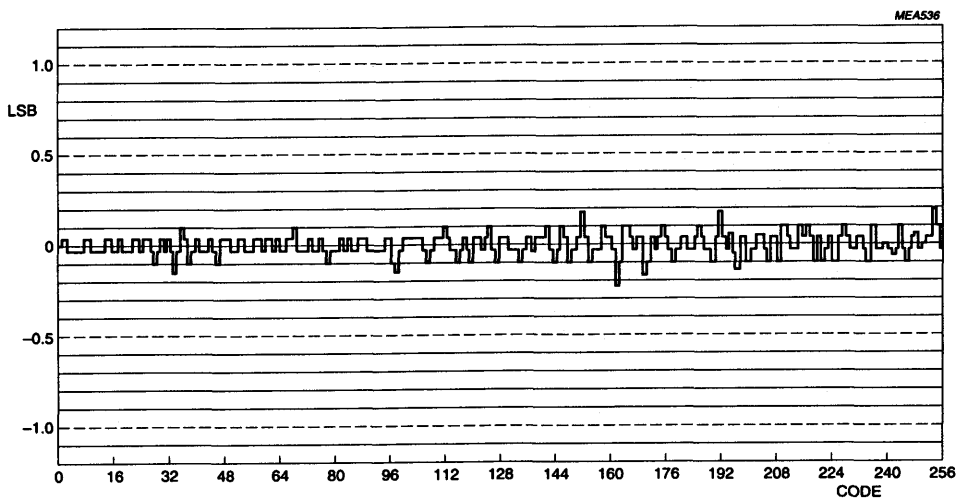
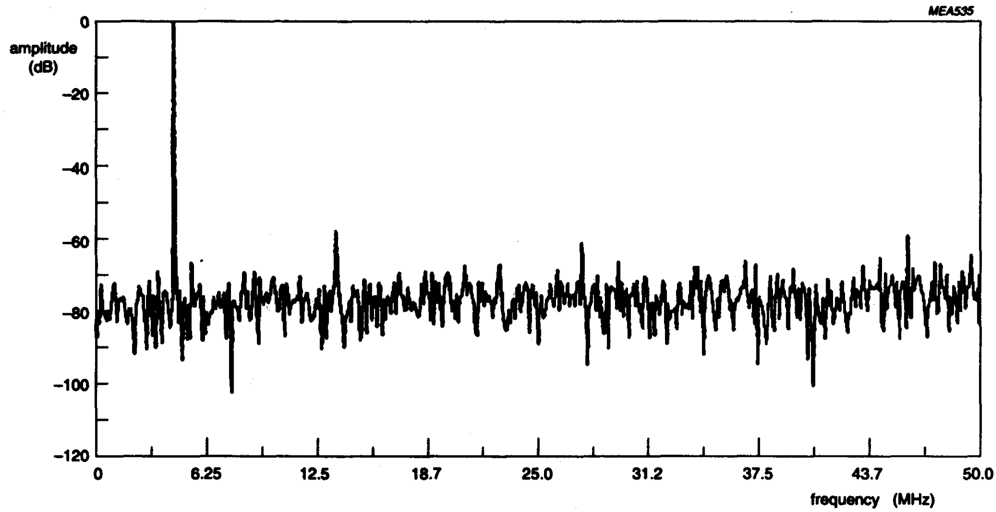


Fig.9 DC differential linearity error (DLE).

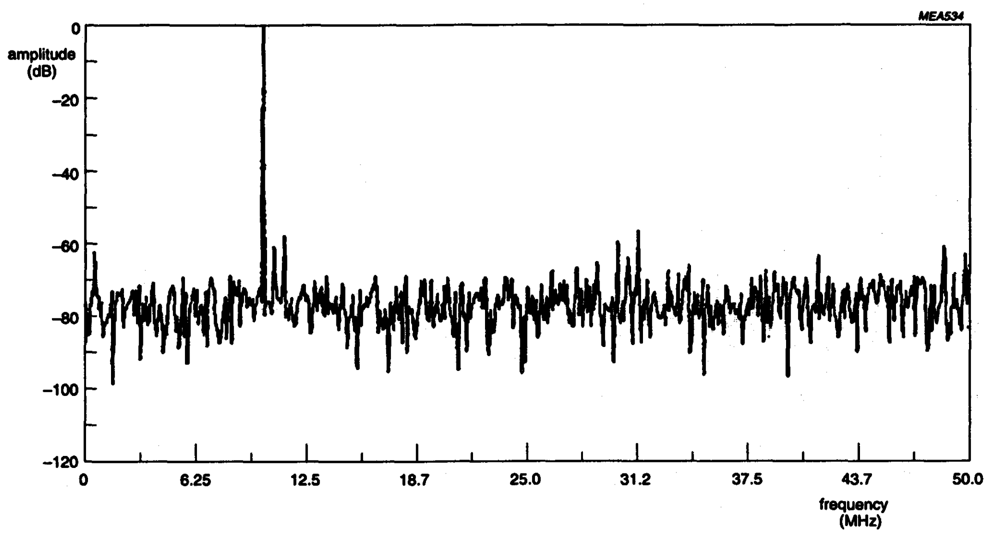
8-bit high-speed analog-to-digital converter

TDA8716



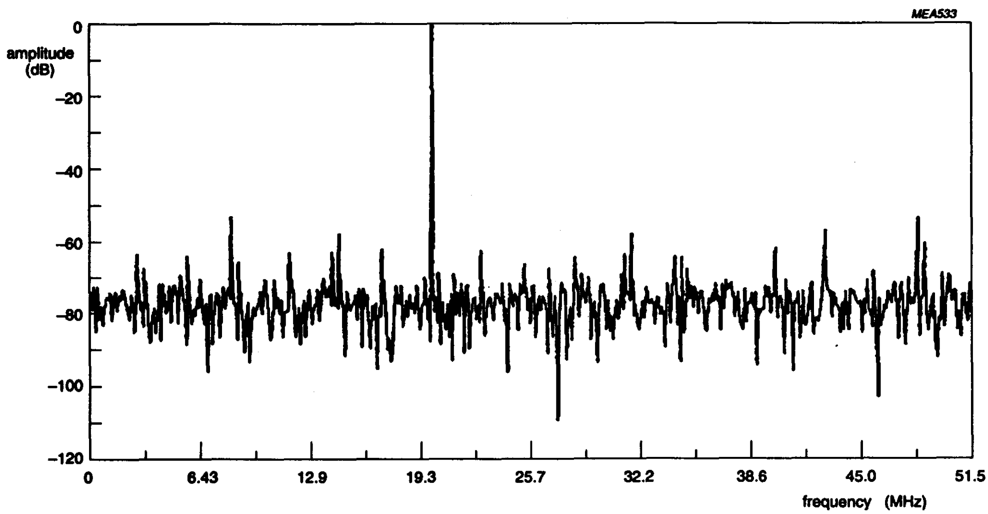
Effective bits: 7.74; Harmonic levels (in dB): 2nd = −69.34; 3rd = −58.85; 4th = −82.55; 5th = −68.16 and 6th = −63.01

Fig.10 Fast fourier transformer (f_{CLK} = 100 MHz; f_i = 4.43 MHz).



Effective bits: 7.57; Harmonic levels (in dB): 2nd = −82.07; 3rd = −61.90; 4th = −75.70; 5th = −65.61 and 6th = −72.50

Fig.11 Fast fourier transformer (f_{CLK} = 100 MHz; f_i = 10 MHz).



Effective bits: 7.04; Harmonic levels (in dB): 2nd = −61.36; 3rd = −56.66; 4th = −61.97; 5th = −62.79 and 6th = −61.52

Fig.12 Fast fourier transformer (f_{CLK} = 100 MHz; f_i = 20 MHz).

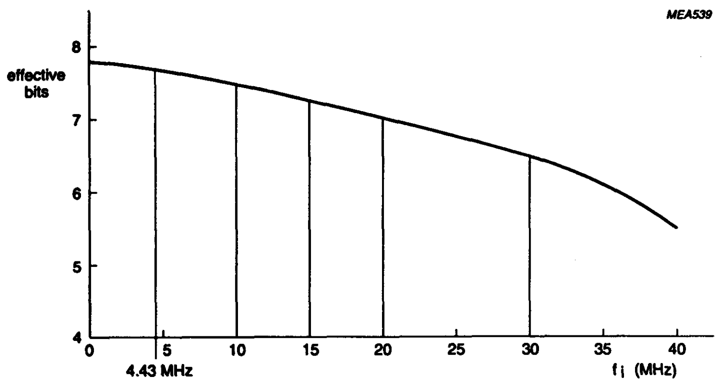


Fig.13 Typical effective bit as a function of input signal at f_{CLK} = 100 MHz.

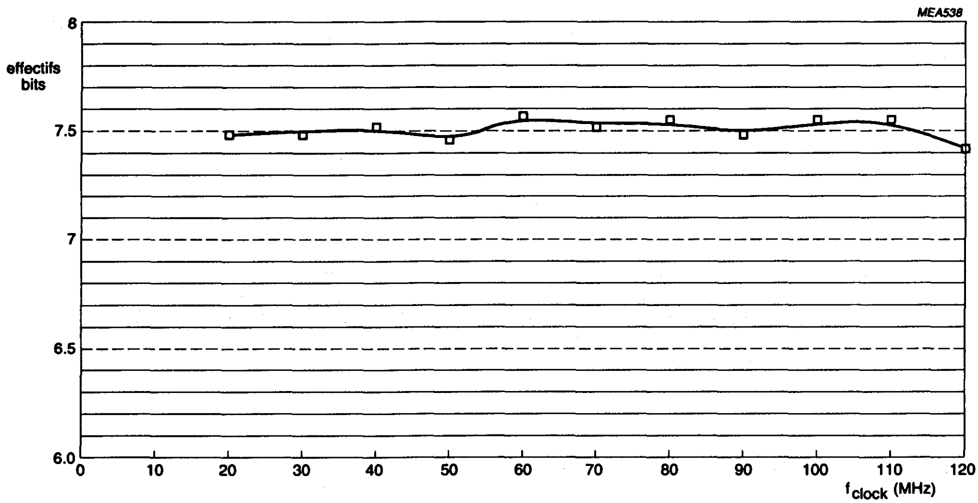


Fig.14 Typical effective bits as a function of clock frequency at f_i = 10 MHz.

8-bit high-speed analog-to-digital converter

FEATURES

- 8-bit resolution
- Sampling rate up to 600 MHz
- ECL (100 k family) compatible for digital inputs and outputs
- Overflow/Underflow output
- 50 Ω load drive capability
- Low input capacitance (5 pF typ.).

APPLICATIONS

- High speed analog-to-digital conversion
- Industrial instrumentation
- Data communication
- RF communication.

GENERAL DESCRIPTION

The TDA8718 is a bipolar 8-bit analog-to-digital converter (ADC) designed for professional applications. The device converts the analog input signal into 8-bit binary coded digital words at a sampling rate of 600 MHz. It has an effective 8-bit bandwidth of 100 MHz. All digital outputs are ECL compatible.

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		−4.2	−4.5	−4.8	V
V_{EED}	digital supply voltage		−4.2	−4.5	−4.8	V
I_{REF}	resistive ladder current	R = 48 Ω	20	45	60	mA
I_{EEA}	analog supply current		−	50	tbf	mA
I_{EED}	digital supply current		−	150	tbf	mA
I_{EEO}	output supply current	R_L = 50 Ω	−	160	−	mA
ILE	DC integral linearity error		−	±0.5	tbf	LSB
DLE	DC differential linearity error		−	±0.5	tbf	LSB
EB	effective bits	f_i = 100 MHz; I_{REF} = 45 mA; f_{CLK} = 500 MHz	−	7.2	−	bits
f_{CLK}	maximum clock frequency		600	−	−	MHz
P_{tot}	total power dissipation (excluding load)		−	1140	tbf	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8718WP	28	PLCC	plastic	SOT261

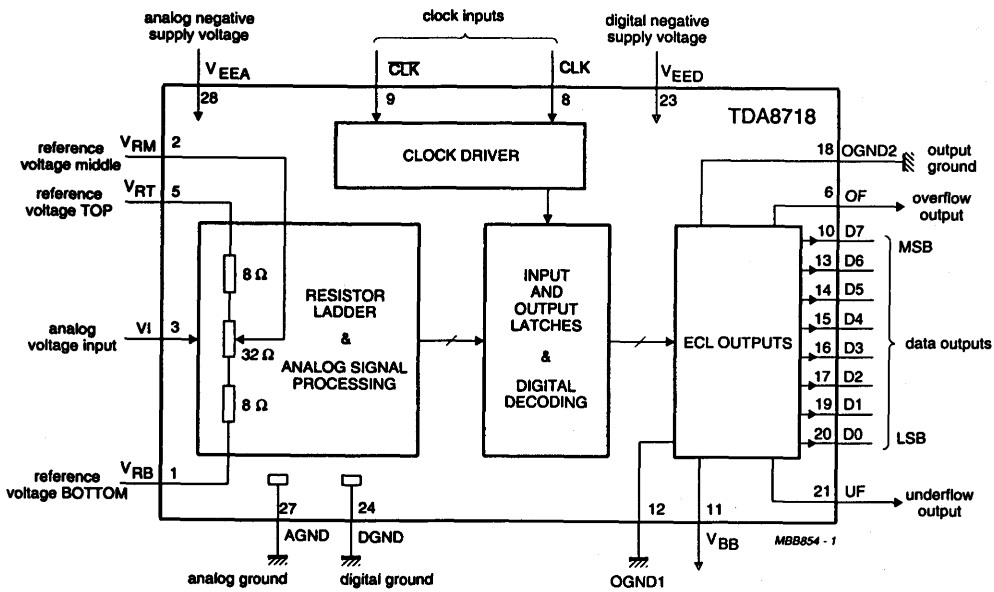


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{RB}	1	reference voltage BOTTOM
V_{RM}	2	reference voltage middle decoupling
VI	3	analog input
n.c.	4	not connected
V_{RT}	5	reference voltage TOP
OF	6	overflow digital output
n.c.	7	not connected
CLK	8	clock input
$\overline{CLK}$	9	complementary clock input
D7	10	digital output (MSB)
V_{BB}	11	ECL reference voltage
OGND1	12	output ground 1 (0 V)
D6	13	digital output
D5	14	digital output
D4	15	digital output
D3	16	digital output
D2	17	digital output
OGND2	18	output ground 2 (0 V)
D1	19	digital output
D0	20	digital output (LSB)
UF	21	underflow digital output
n.c.	22	not connected
V_{EED}	23	digital negative supply voltage (−4.5 V)
DGND	24	digital ground
n.c.	25	not connected
n.c.	26	not connected
AGND	27	analog ground
V_{EEA}	28	analog negative supply voltage (−4.5 V)

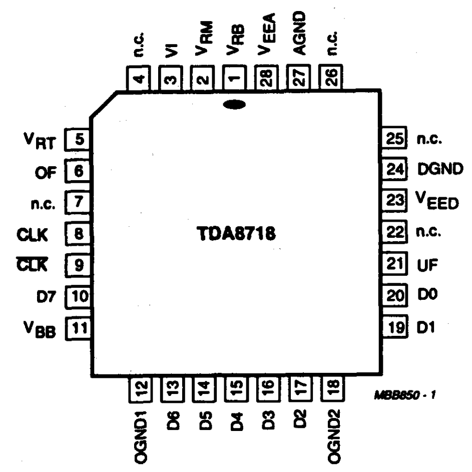


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

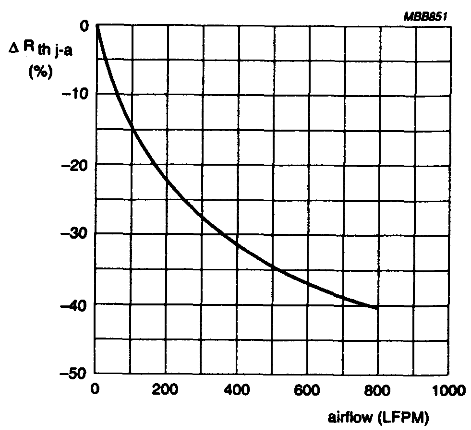
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage (pin 28)		−7.0	+0.3	V
V_{EED}	digital supply voltage (pin 23)		−7.0	+0.3	V
V_{EEA}-V_{EED}	supply voltage difference		−1.00	+1.0	V
VI	input voltage	referenced to AGND	V_{EEA}	0	V
CLK; $\overline{CLK}$(p-p)	input voltage for differential clock drive (peak-to-peak value)	referenced to V_{EED}; note 1	−	2.0	V
I_O	output current		−	tbf	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

Note

1. The circuit has two clock inputs: CLK and $\overline{CLK}$. Sampling takes place on the falling edge of the clock input signal: CLK and $\overline{CLK}$ are two complementary signals.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	45 K/W



Test conditions: PCB (2.24 x 2.24 x 0.062 inches)

Fig.3 Average effect of air flow on $R_{th\ j\text{-}a}$.

CHARACTERISTICS

V_{EEA} = −4.2 V to −4.8 V; V_{EED} = −4.2 V to −4.8 V; $V_{EEA} - V_{EED}$ = −0.1 to +0.1 V; AGND and DGND shorted together; T_{amb} = 0 to +70 °C; unless otherwise specified. (Typical readings taken at V_{EEA} = −4.5 V; V_{EED} = −4.5 V; T_{amb} = 25 °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EEA}	analog supply voltage (pin 28)		−4.2	−4.5	−4.8	V
V_{EED}	digital supply voltage (pin 23)		−4.2	−4.5	−4.8	V
I_{EEA}	analog supply current (pin 28)		−	50	tbf	mA
I_{EED}	digital supply current (pin 23)		−	150	tbf	mA
I_{EEO}	output supply current	R_L = 50 Ω	−	160	−	mA
Reference voltages for the resistor ladder (see Table 1)						
I_{REF}	reference current (pin 5)	R = 48 Ω	20	45	60	mA
V_{RB}	reference voltage BOTTOM (pin 1)		−	48 Ω x I_{REF}	−	V
V_{RT}	reference voltage TOP (pin 5)		−	0	−	V
R_{LAD}	resistor ladder		−	48	−	Ω
R_{LTC}	temperature coefficient of the resistor ladder		−	tbf	−	Ω/°C
V_{OB}	voltage offset BOTTOM	note 1	−	8 Ω x I_{ref}	−	mV
V_{OT}	voltage offset TOP	note 1	−	8 Ω x I_{ref}	−	mV
Inputs						
CLK input (pin 8); $\overline{CLK}$ input (pin 9)						
V_{IL}	LOW level input voltage	T_{amb} = 25 °C	−	−1.8	−	V
V_{IH}	HIGH level input voltage	T_{amb} = 25 °C	−	−0.8	−	V
I_{IL}	LOW level input current	V_{CLK} = −1.8 V	−	tbf	−	µA
I_{IH}	HIGH level input current	V_{CLK} = −0.8 V	−	tbf	−	µA
R_I	input resistance	f_{CLK} = 100 MHz	−	1.5	−	kΩ
C_I	input capacitance	f_{CLK} = 100 MHz	−	3.5	−	pF
$\Delta V_{CLK(p-p)}$	clock input differential V_{CLK} - $V_{\overline{CLK}}$ (peak-to-peak value)		tbf	900	tbf	mV
Analog input (pin 3); note 2						
I_{IL}	LOW level input current	data output = 00	20	40	80	µA
I_{IH}	HIGH level input current	data output = FF	100	200	400	µA
R_I	input resistance		−	10	−	kΩ
C_I	input capacitance		−	5	−	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs (R_L = 50 Ω)						
Gigital 100 K ECL outputs (D0 to D7; OF; UF)						
V_{OL}	LOW level output voltage	T_{amb} = 25 °C	−1810	−1705	−1630	mV
V_{OH}	HIGH level output voltage	T_{amb} = 25 °C	−1025	−955	−880	mV
V_{ECL}	ECL reference voltage		–	−1.4	–	V
I_{OL}	LOW level output current		4	6	8	mA
I_{OH}	HIGH level output current		10	20	25	mA
Switching characteristics						
f_{CLK}; $\overline{f_{CLK}}$	maximum clock frequency		600	–	–	MHz
$t_{r,f}$	rise and fall time	f_i = 100 MHz	–	–	750	ps
Analog signal processing (f_{CLK} = 500 MHz)						
Harmonics (full scale)						
f_1	fundamental	f_i = 100 MHz	–	0	–	dB
f_2	even	f_i = 100 MHz	–	−54	–	dB
f_3	odd	f_i = 100 MHz	–	−50	–	dB
Transfer function						
ILE	DC integral linearity error		–	±0.5	tbf	LSB
DLE	DC differential linearity error		–	±0.5	tbf	LSB
AILE	AC integral linearity error	note 3	–	tbf	tbf	LSB
EB	effective bits	note 4; I_{REF} = 45 mA; f_{CLK} = 100 MHz; f_i = 4.43 MHz	–	7.7	–	bits
		note 5; I_{REF} = 45 mA; f_{CLK} = 500 MHz; f_i = 100 MHz	–	7.2	–	bits
BER	bit error rate	f_{CLK} = 500 MHz; f_i = 100 MHz; V_i = ±8 LSB at code 128; 50% clock duty cycle	–	10^{-11}	–	times/ sample s
Timing (f_{CLK} = 500 MHz; R_L = 50 Ω; C_L = 3 pF) note 5						
t_{ds}	sampling delay		–	–	300	ps
t_{HD}	output hold time		tbf	250	–	ps
t_d	output delay time		–	500	tbf	ps
t_{aj}	aperture jitter		–	4	–	ps

Notes

1. Voltage offset BOTTOM (V_{OB}) is the difference between the analog input which produces data outputs equal to 00 and the reference voltage BOTTOM (V_{RB}), at T_{amb} = 25 °C. Voltage offset TOP (V_{OT}) is the difference between reference voltage TOP (V_{RT}) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
2. The analog input is not internally biased. It should be externally biased between V_{RT} and V_{RB} levels.

3. Full-scale sinewave; f_i = 4.43 MHz; f_{CLK}, $\bar{f}_{CLK}$ = 100 MHz.
4. Effective bits are obtained via a Fast Fourier Transformer (FFT) treatment taking 4 K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to SNR: SNR (dB) = EB x 6.02 + 1.76.
5. TDA8718 can only withstand one or two 100 k ECL loads in order to work out timings at the maximum sampling frequency. It is recommended to minimize the printed circuit-board load by implementing the load device as close as possible to the TDA8718.

Table 1 Output coding (typical value).

STEP	V_I	BINARY OUTPUTS	O/UFL
	(TYP. value)	D5 to D0	
Underflow	< −40 Ω x I_{ref}	000000	1
0	−40 Ω x I_{ref}	000000	0
1	.	000001	0
.	.	......	.
.	.	......	.
.	.	......	.
254	.	111110	0
255	−8 Ω x I_{ref}	111111	0
Overflow	> −8 Ω x I_{ref}	111111	1

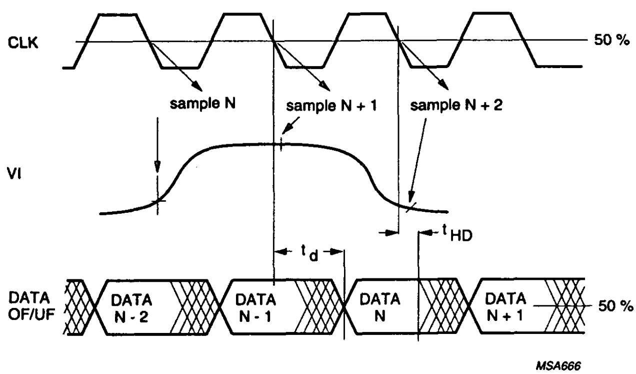


Fig.4 Timing diagram.

APPLICATION INFORMATION

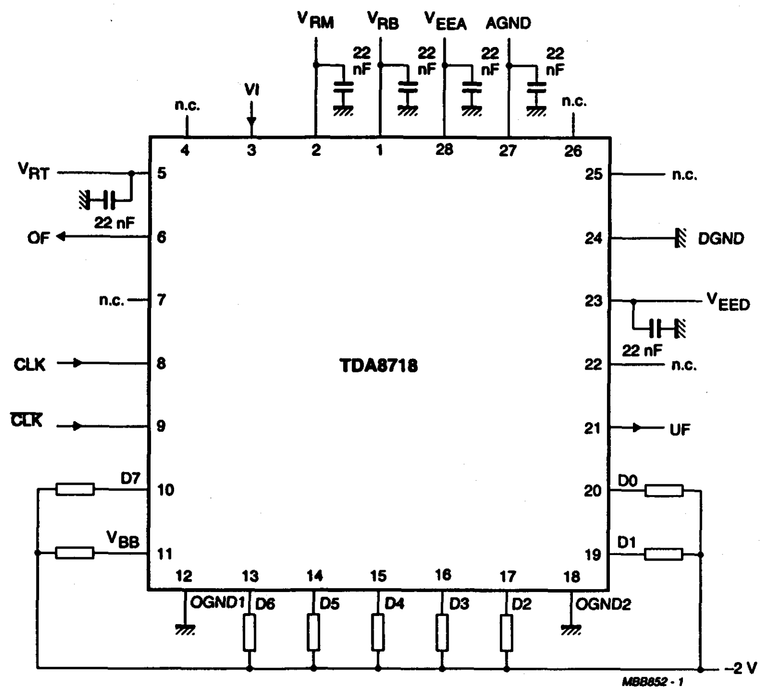


Fig.5 Application diagram.

YUV 8-bit video low-power analog-to-digital interface

TDA8755

FEATURES

- 8-bit resolution
- Sampling rate up to 20 MHz
- TTL compatible digital inputs
- 3-state TTL outputs
- U, V two's complement outputs
- Y binary output
- Power dissipation of 565 mW (typ.)
- Low analog input capacitance, no buffer amplifier required
- High signal-to-noise ratio over a large analog input frequency range
- Track-and-hold included
- Clamp functions included
- UV multiplexed ADC
- 4:1:1 output data encoder
- Stable voltage regulator included.

APPLICATIONS

- High speed analog-to-digital convertion for video signal digitizing
- 100 Hz improved definition TV (IDTV)

GENERAL DESCRIPTION

The TDA8755 is a monolithic bipolar 8-bit video low-power analog-to-digital convertion (ADC) interface for YUV signals. The device converts the YUV analog input signal into 8-bit binary coded digital words in a 4:1:1 format at a sampling rate of 20 MHz. The U/V signals are converted in a multiplexed manner. All analog signal inputs are digitally clamped and a fast precharge is provided for start-up. All digital inputs and outputs are TTL compatible. Frame synchronization is supported.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	48	tbf	mA
I_{CCD}	digital supply current		–	57	tbf	mA
I_{EEO}	output stages supply current		–	8	tbf	mA
ILE	DC integral linearity error	f_{CLK} = 0.8 MHz	–	–	±1	LSB
DLE	DC differential linearity error	f_{CLK} = 0.8 MHz	–	–	±0.5	LSB
EB	effective bit	note 1	–	7.0	–	bits
f_{CLK}	maximum conversion rate		20	–	-	MHz
P_{tot}	total power dissipation		–	565	620	mW

Note

1. The number of effective bits is measured with a 20 MHz clock frequency. This value is given for a 4.43 MHz input frequency on the Y channel (1.5 MHz on the U and V channels). This value is obtained via a Fast Fourier Transformer (FFT) treatment taking 4K acquisition points per period. The valculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency).
   Conversion to SNR: SNR (dB) = EB x 6.02 + 1.76.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8755T	32	SO32L	plastic	SOT287

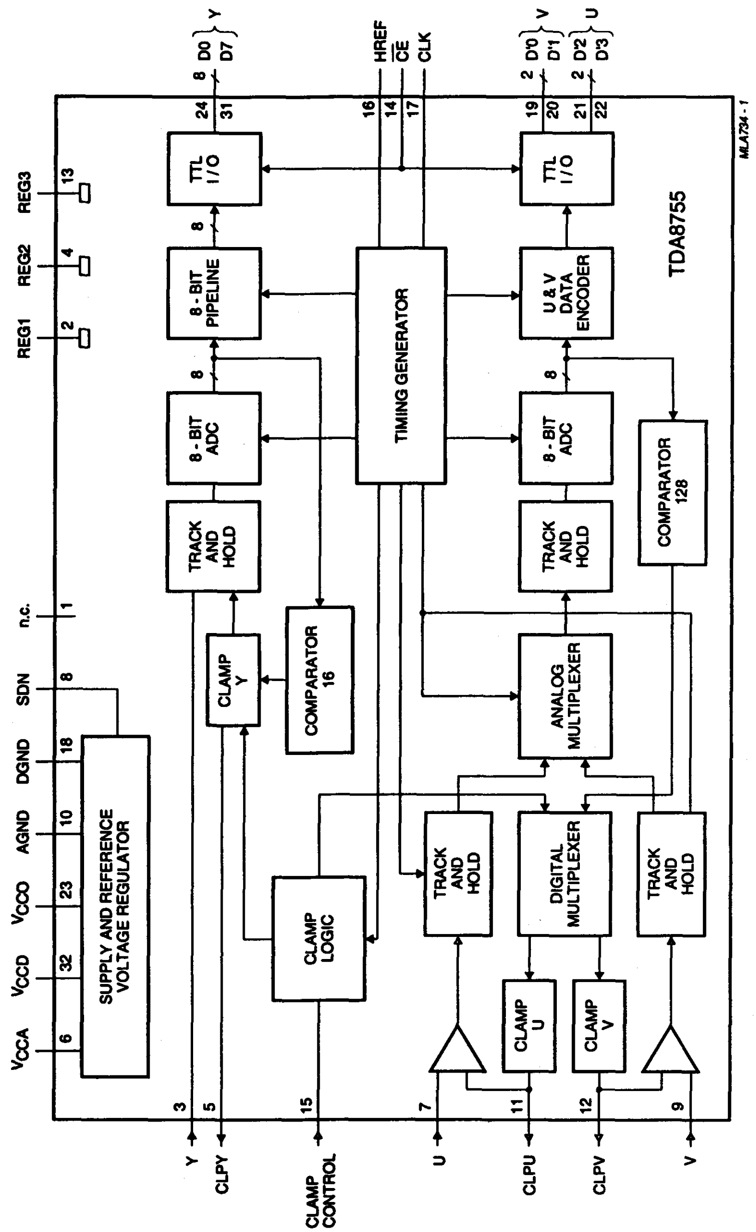


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
REG1	2	decoupling input (internal stabilization loop decoupling)
INY	3	Y analog voltage input
REG2	4	decoupling input (internal stabilization loop decoupling)
CLPY	5	Y clamp capacitor connection
V_{CCA}	6	analog positive supply voltage (+5 V)
INU	7	U analog voltage input
SDN	8	stabilizer decoupling node and analog reference voltage (+3.35 V)
INV	9	V analog voltage input
AGND	10	analog ground
CLPU	11	U clamp capacitor connection
CLPV	12	V clamp capacitor connection
REG3	13	decoupling input (internal stabilization loop decoupling)
$\overline{CE}$	14	chip enable input (TTL level input active LOW)
CLP	15	clamp control input
HREF	16	horizontal reference signal
CLK	17	clock input
DGND	18	digital ground
D'0	19	V data output; bit 0 (n−1)
D'1	20	V data output; bit 1 (n)
D'2	21	U data output; bit 0 (n−1)
D'3	22	U data output; bit 1 (n)
V_{CCO}	23	positive supply voltage for output stages (+5 V)
D0	24	Y data output; bit 0 (LSB)
D1	25	Y data output; bit 1
D2	26	Y data output; bit 2
D3	27	Y data output; bit 3
D4	28	Y data output; bit 4
D5	29	Y data output; bit 5
D6	30	Y data output; bit 6
D7	31	Y data output; bit 7 (MSB)
V_{CCD}	32	digital positive supply voltage (+5 V)

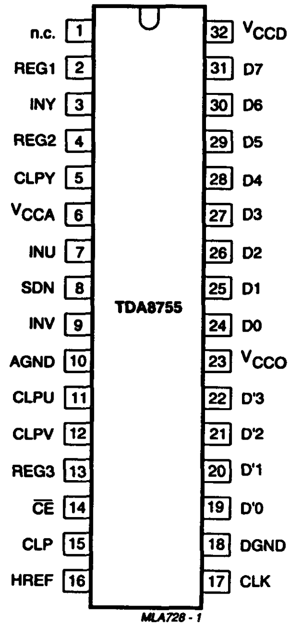


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		−0.3	7.0	V
V_{CCD}	digital supply voltage		−0.3	7.0	V
V_{CCO}	output stages supply voltage		−0.3	7.0	V
V_{CCA} - V_{CCD}	supply voltage difference		−1	+1	V
V_{CCO} - V_{CCD}	supply voltage difference		−1	+1	V
V_{CCA} - V_{CCO}	supply voltage difference		−1	+1	V
V_I	input voltage	referenced to AGND	−	+5.0	V
$V_{CLK(p-p)}$	AC input switching voltage (peak-to-peak value)	referenced to DGND	−	V_{CCD}	V
I_O	output current		−	+6	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	70 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_8 - V_{10}$ = 4.75 V to 5.25 V; $V_{CCD} = V_{32} - V_{18}$ = 4.75 V to 5.25 V; $V_{CCO} = V_{23} - V_{18}$ = 4.75 V to 5.25 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD}$ = −0.25 V to +0.25 V; $V_{CCO} - V_{CCD}$ = −0.25 V to +0.25 V; $V_{CCA} - V_{CCO}$ = −0.25 V to +0.25 V; T_{amb} = 0 °C to +70 °C; unless otherwise specified. (Typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V; T_{amb} = 25 °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		−	48	tbf	mA
I_{CCD}	digital supply current		−	57	tbf	mA
I_{CCO}	output stage supply current		−	8	tbf	mA
Inputs						
CLK input (pin 7)						
V_{IL}	LOW level input voltage		0	−	0.8	V
V_{IH}	HIGH level input voltage		2.0	−	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	−400	−	−	μA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	−	−	100	μA
Z_I	input impedance	f_{CLK} = 20 MHz	−	4	−	kΩ
C_I	input capacitance	f_{CLK} = 20 MHz	−	4.5	−	pF
$\overline{CE}$, CLP and HREF (pins 14 to 16)						
V_{IL}	LOW level input voltage		0	−	0.8	V
V_{IH}	HIGH level input voltage		2.0	−	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	−400	−	−	μA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	−	−	20	μA
Clamp input CLPY (pin 5)						
V_7	clamp voltage for 16 output code		−	3.5	−	V
I_7	clamp output current		−	±50	−	μA
Clamp inputs CLPU and CLPV (pins 11 and 12)						
$V_{9,\,10}$	clamp voltage for 128 output code		−	3.325	−	V
$I_{9,\,10}$	clamp output current		−	±50	−	μA
Analog input INY (pin 3)						
$V_{I(p-p)}$	input voltage, full range (peak-to-peak value)	f_i = 4.43 MHz	tbf	1.0	tbf	V
Z_I	input impedance	f_i = 6 MHz	−	30	−	kΩ
C_I	input capacitance	f_i = 6 MHz	−	1	−	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs INU and INV (pins 7 and 9)						
$V_{I(p-p)}$	input voltage, full range (peak-to-peak value)	f_i = 1.5 MHz	tbf	1.0	tbf	V
Z_I	input impedance	f_i = 2 MHz	–	30	–	kΩ
C_I	input capacitance	f_i = 2 MHz	–	1	–	pF
Inputs isolation						
α	crosstalk between Y, U and V		–	−55	−50	dB
Outputs						
SDN (pin 8)						
V_{REF}	reference voltage		–	3.35	–	V
V_{REG}	line regulation	4.75 V ≤ V_{CCA} ≤ 5.25 V	–	2.0	–	mV
I_{LOAD}	load current		−2	–	–	mA
Digital outputs D0 to D7 and D'0 to D'3 (pins 24 to 31 and 19 to 22)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = −0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	–	+20	μA
Switching characteristics						
f_{CLKmax}	maximum input clock frequency		20	–	–	MHz
f_{CLKmin}	minimum input clock frequency		–	–	0.8	MHz
t_{CPH}	clock pulse width HIGH		20	–	–	ns
t_{CPL}	clock pulse width LOW		20	–	–	ns
Analog signal processing (f_{CLK} = 20 MHz; 50% clock duty factor)						
G_{diff}	differential gain	note 1; see Fig.7	–	2	–	%
Φ_{diff}	differential phase	note 1; see Fig.7	–	3	–	deg
f_1	fundamental harmonics (full-scale)	note 2	–	–	0	dB
f_{all}	harmonics (full-scale), all components	note 2	–	−54	–	dB
SVRR1	supply voltage ripple rejection	note 3	–	−32	–	dB
SVRR2	supply voltage ripple rejection	note 3	–	tbf	–	%/V
Transfer function (50% clock duty factor)						
ILE	DC integral linearity error	f_{CLK} = 0.8 MHz	–	–	±1	LSB
DLE	DC differential linearity error	f_{CLK} = 0.8 MHz	–	–	±0.5	LSB
AILE	AC integral linearity error	note 4	–	–	±2	LSB
EB	effective bit	note 5	–	7.0	–	bits

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (note 6; see Figs 3 to 7; f_{CLK} = 20 MHz)						
t_{ds}	sampling delay		–	tbf	–	ns
t_{HD}	output hold time		7	–	–	ns
t_d	output delay time		–	40	42	ns
t_{dZH}	3-state output delay time	enable-to-HIGH	–	tbf	tbf	ns
t_{dZL}	3-state output dedlay time	enable-to-LOW	–	tbf	tbf	ns
t_{dHZ}	3-state output delay time	disable-to-HIGH	–	tbf	tbf	ns
t_{dLZ}	3-state output dedlay time	disable-to-LOW	–	tbf	tbf	ns
t_{CLKr}	clock rise time		3	5	–	ns
t_{CLKf}	clock fall time		3	5	–	ns
t_{SU}	HREF set-up time		7	–	–	ns
t_{IH}	HREF hold time		3	–	–	ns
t_r	data output rise time		–	10	–	ns
t_f	data output fall time		–	10	–	ns
t_{CLP}	minimum time for active clamp	note 7; see Fig.9	3	–	–	µs

Notes

1. Low frequency ramp signal ($V_{I(p-p)}$ = full-scale and 64 µs period) combined with a sinewave input voltage ($V_{I(p-p)}$ = 0.25 full-scale, f_i = maximum permitted frequency) at the input.
2. The input conditions are related as follows:

   Y - $V_{I(p-p)}$ = 1.0 V; f_i = 4.43 MHz

   U/V - $V_{I(p-p)}$ = 1.0 V; f_i = 1.5 MHz.
3. Supply voltage ripple rejection:

   SVRR1: variation of the input voltage producing output code 127 (code 15) for supply voltage variation of 1 V:

   $SVRR1 = 20 \log (\Delta V_{I(127)} / \Delta V_{CCA})$

   SVRR2: relative variation of the full-scale range of analog input for a supply voltage variation of 1 V:

   $SVRR2 = \{\Delta(V_{I(0)} - \Delta V_{(255)}) / (V_{I(0)} - V_{I(255)}\} / \Delta V_{CCA}$.
4. Full-scale sinewave (f_i = 4.43 MHz for Y and f_i = 1.5 MHz for U and V; f_{CLK} = 20 MHz).
5. The number of effective bits is measured using a 20 MHz clock frequency. This value is given for a 4.43 MHz input frequency on the Y channel (1.5 MHz on the U and V channels). This value is obtained via a fast fourier transformer (FFT) treatment taking 4K acquisition points per period. The valculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency).
   Conversion to SNR: SNR (dB) = EB x 6.02 + 1.76.
6. Output data acquisition: is available after the maximum delay of t_d.
7. U and V output data is not valid during t_{CLP}.

Table 1 Mode selection.

$\overline{CE}$	D7 to D0; D'3 to D'0
1	high impedance
0	active; binary

Table 2 Output data coding.

OUTPUT PORT	BIT	OUTPUT DATA			
Y	D7	Y_07	Y_17	Y_27	Y_37
	D6	Y_06	Y_16	Y_26	Y_36
	D5	Y_05	Y_15	Y_25	Y_35
	D4	Y_04	Y_14	Y_24	Y_34
	D3	Y_03	Y_13	Y_23	Y_33
	D2	Y_02	Y_12	Y_22	Y_32
	D1	Y_01	Y_11	Y_21	Y_31
	D0	Y_00	Y_10	Y_20	Y_30
U	D'3	$\overline{U_0}7$	U_05	U_03	U_01
	D'2	U_06	U_04	U_02	U_00
V	D'1	$\overline{V_0}7$	V_05	V_03	V_01
	D'0	V_06	V_04	V_02	V_00

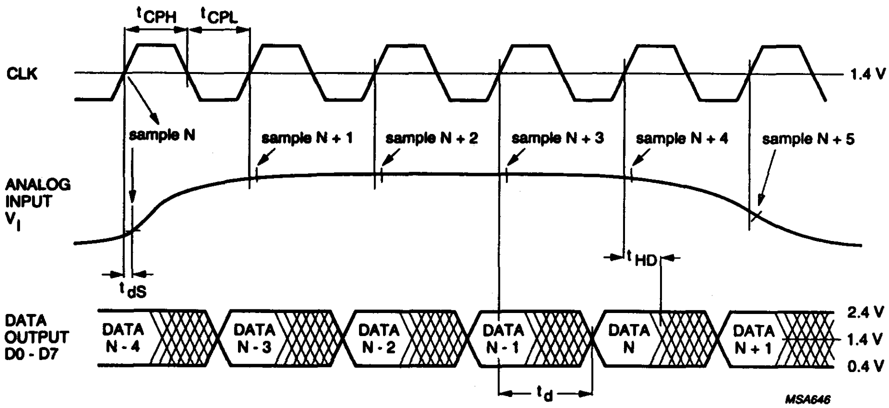


Fig.3 Timing diagram (INY signal).

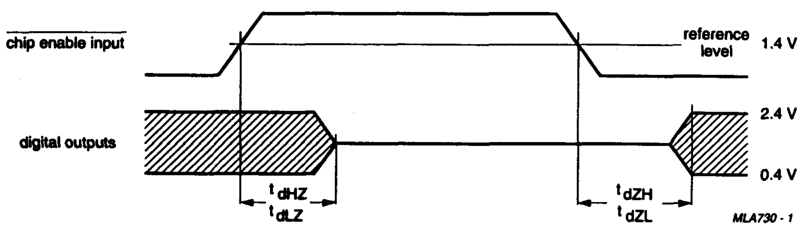
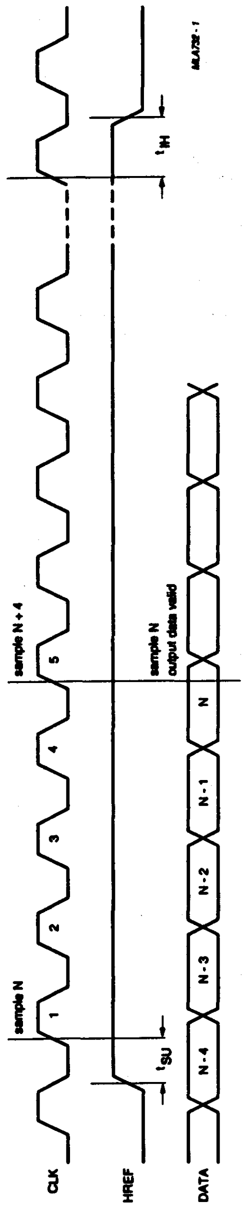
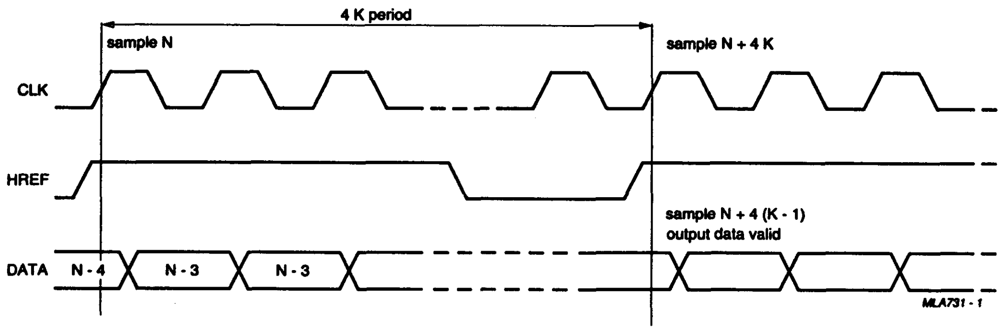


Fig.4 Timing diagram (3-state delay).



The output data is valid 4 clock periods after HREF goes HIGH.

Fig.5 Timing definition for set-up and hold (HREF signal).



When the HREF period is a whole multiple of 4 clock periods, the output data is valid without any clock delay. The internal circuit always gives an internal delay of 4 clock periods as illustrated in Fig.5.

Fig.6 Timing diagram (HREF signal).

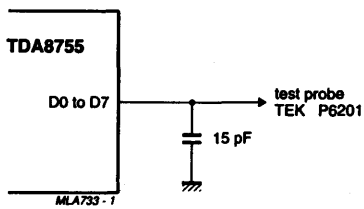


Fig.7 Load circuit for the 3-state output timing measurement.

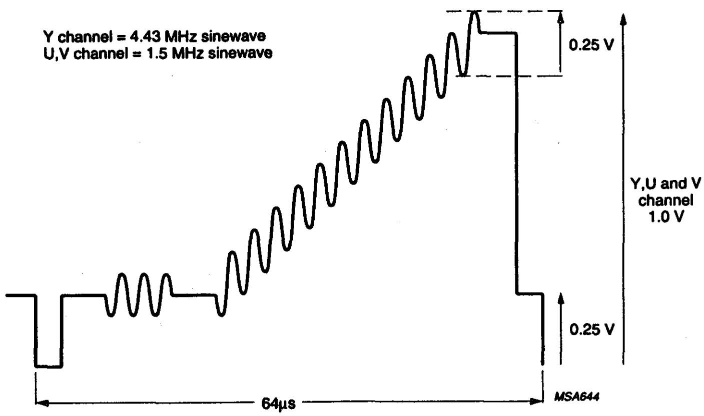


Fig.8 Input test signal for differential gain anf phase measurements.

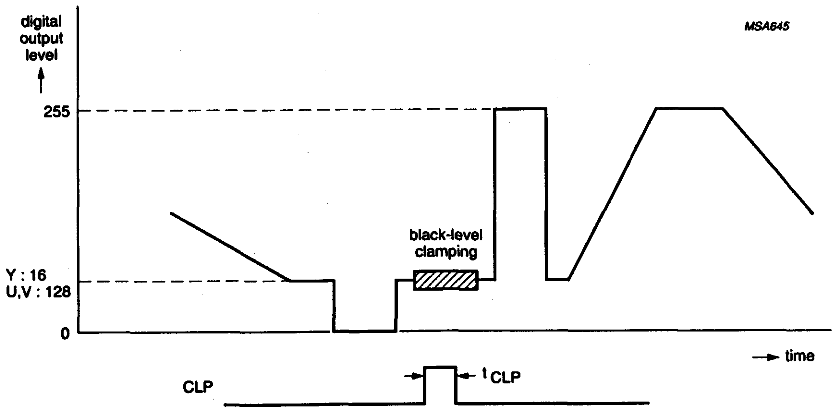
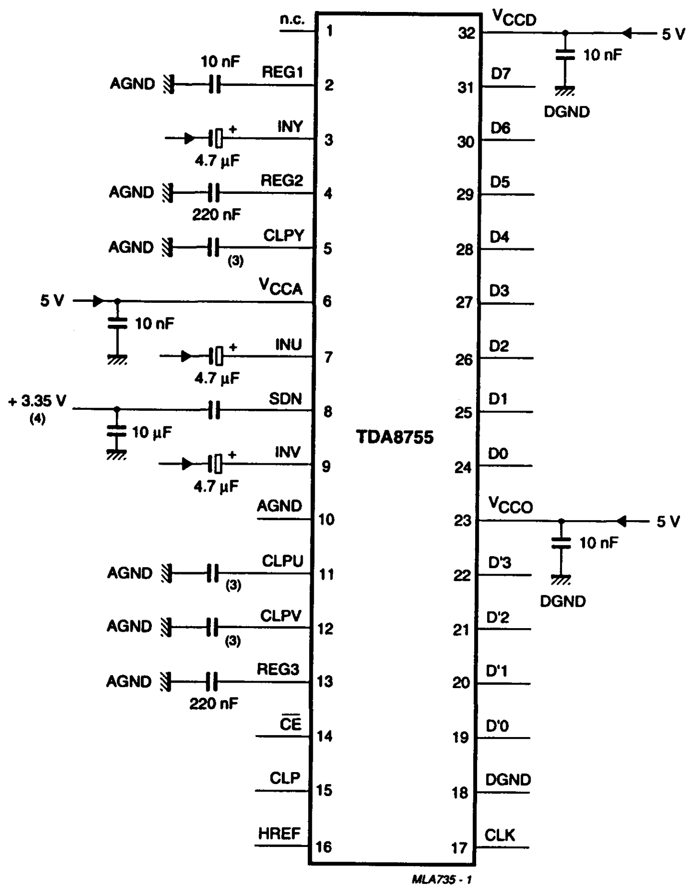


Fig.9 Clamping control timing.



(1) CLK should be decoupled to DGND with a 100 nF capacitor if a TTL signal is used on CLK.
(2) Analog and digital supplies should be separated and decoupled.
(3) Clamp capacitors must be determined according to the application; recommended values are CLPY = 18 nF, CLPU and CLPV = 33 nF.
(4) It is possible to use the reference output voltage pin SDN to drive other analog circuits under the limits indicated (see Characteristics).

Fig.10 Application diagram.

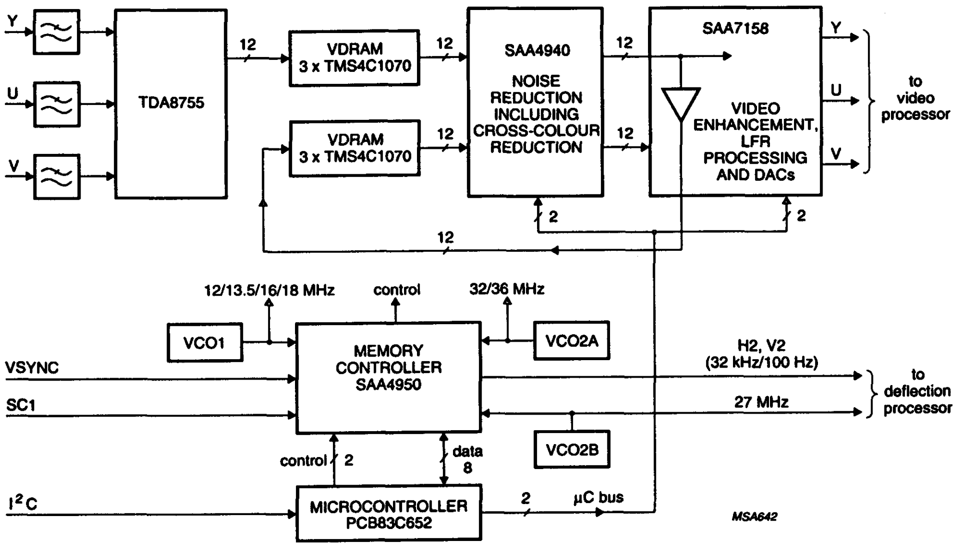


Fig.11 Block diagram of a full-options IPQ module.

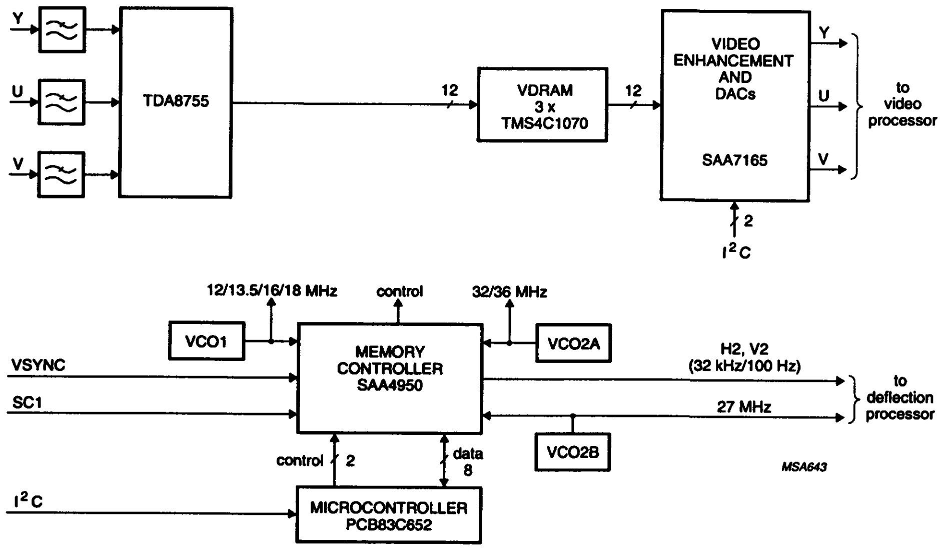


Fig.12 Block diagram of an economic IPQ module.

Triple 8-bit video digital-to-analog converter TDA8771

FEATURES

- 8-bit resolution
- Sampling rate up to 35 MHz
- Internal reference voltage regulator
- No deglitching circuit required
- Large output voltage range
- 1 kΩ output load
- Single 5 V power supply
- Power dissipation only 175 mW (typical)
- 44-pin QFP package.

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing.

GENERAL DESCRIPTION

The TDA8771 is a triple 8-bit video digital-to-analog converter (DAC). It converts the digital input signals into analog voltage outputs at a maximum conversion rate of 35 MHz. The DACs are based on resistor-string architecture with integrated output buffers. The output voltage range is determined by a built-in reference source.
The device is fabricated in a 5 V, 1 µm CMOS process that ensures high functionality with low power dissipation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	30	tbf	mA
I_{DDD}	digital supply current	–	5	tbf	mA
ILE	DC integral linearity error	–	–	±1/2	LSB
DLE	DC differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum conversion rate	35	–	–	MHz
P_{tot}	total power dissipation (without load)	–	175	tbf	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8771H	44	QFP	plastic	SOT307B

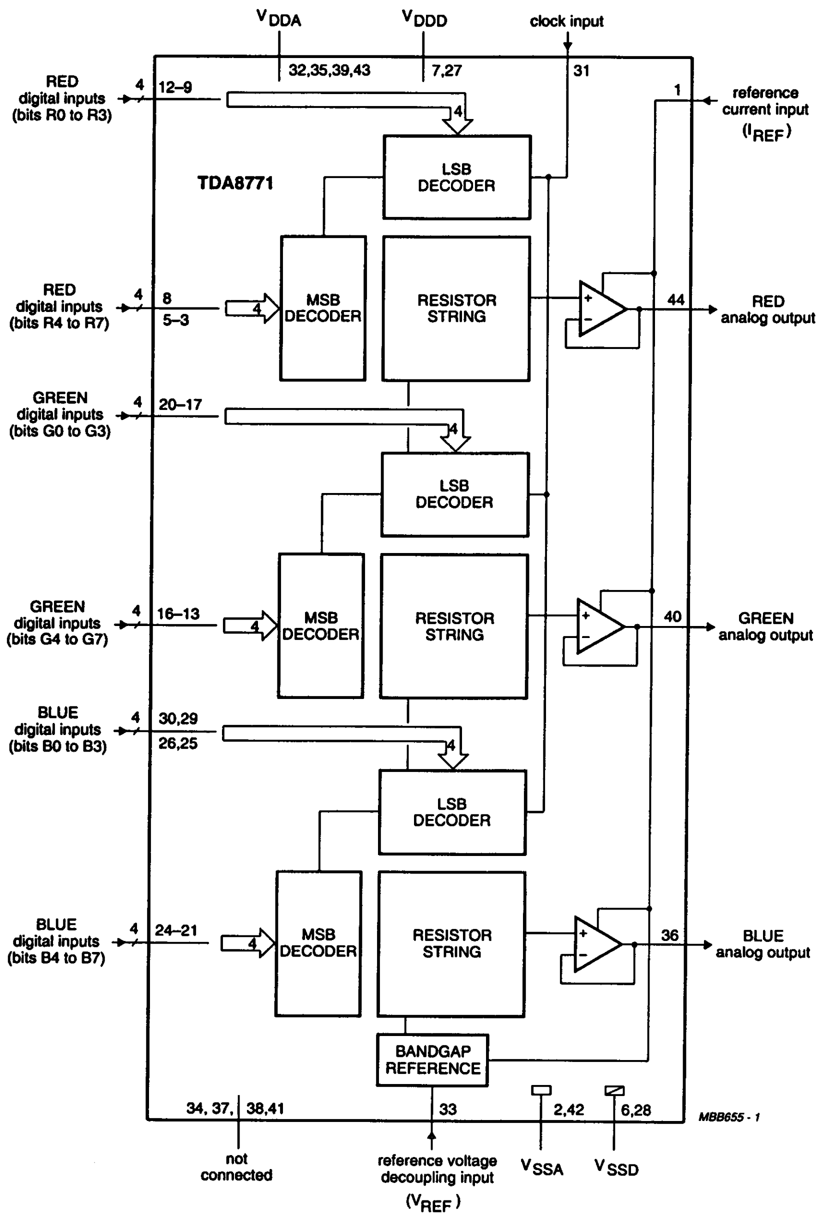


Fig.1 Block diagram.

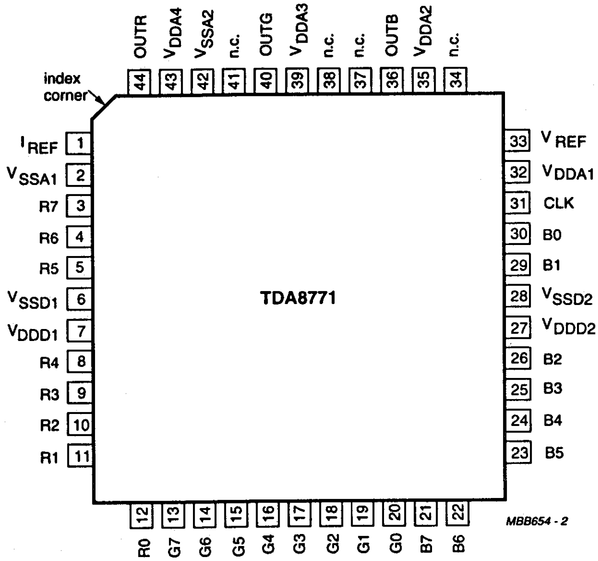


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
I_{REF}	1	reference current input for output buffers
V_{SSA1}	2	analog supply ground 1
R7	3	RED digital input data; bit 7 (MSB)
R6	4	RED digital input data; bit 6
R5	5	RED digital input data; bit 5
V_{SSD1}	6	digital supply ground 1
V_{DDD1}	7	digital supply voltage 1
R4	8	RED digital input data; bit 4
R3	9	RED digital input data; bit 3
R2	10	RED digital input data; bit 2
R1	11	RED digital input data; bit 1
R0	12	RED digital input data; bit 0 (LSB)
G7	13	GREEN digital input data; bit 7 (MSB)
G6	14	GREEN digital input data; bit 6

SYMBOL	PIN	DESCRIPTION
G5	15	GREEN digital input data; bit 5
G4	16	GREEN digital input data; bit 4
G3	17	GREEN digital input data; bit 3
G2	18	GREEN digital input data; bit 2
G1	19	GREEN digital input data; bit 1
G0	20	GREEN digital input data; bit 0 (LSB)
B7	21	BLUE digital input data; bit 7 (MSB)
B6	22	BLUE digital input data; bit 6
B5	23	BLUE digital input data; bit 5
B4	24	BLUE digital input data; bit 4
B3	25	BLUE digital input data; bit 3
B2	26	BLUE digital input data; bit 2
V_{DDD2}	27	digital supply voltage 2
V_{SSD2}	28	digital supply ground 2
B1	29	BLUE digital input data; bit 1
B0	30	BLUE digital input data; bit 0 (LSB)
CLK	31	clock input
V_{DDA1}	32	analog supply voltage 1
V_{REF}	33	decoupling input for reference voltage
n.c.	34	not connected
V_{DDA2}	35	analog supply voltage 2
OUTB	36	BLUE analog output
n.c.	37	not connected
n.c.	38	not connected
V_{DDA3}	39	analog supply voltage 3
OUTG	40	GREEN analog output
n.c.	41	not connected
V_{SSA2}	42	analog supply ground 2
V_{DDA4}	43	analog supply voltage 4
OUTR	44	RED analog output

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	−0.5	+6.5	V
V_{DDD}	digital supply voltage	−0.5	+6.5	V
V_{DDA} - V_{DDD}	supply voltage differences	−1.0	+1.0	V
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	−	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT307B)	75 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{DDA} = V_{DDD}$ = 4.5 V to 5.5 V; V_{SSA} and V_{SSD} shorted together; $V_{DDA} - V_{DDD}$ = −0.5 V to +0.5 V; T_{amb} = 0 °C to +70 °C; unless otherwise specified (typical values measured at $V_{DDA} = V_{DDD}$ = 5 V and T_{amb} = 25 °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	R7-R0, G7-G0, B7-B0 = logic 0	–	30	tbf	mA
I_{DDD}	digital supply current	f_{CLK} = 35 MHz	–	5	tbf	mA
Inputs						
Clock input (pin 31)						
V_{IL}	LOW level input voltage		0	–	1.2	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
R, G, B digital inputs (pins 12-8, 5-3; 20-13; 30, 29, 26-21)						
V_{IL}	LOW level input voltage		0	–	1.2	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
I_{REF} buffer supply current						
I_I	input current		–	0.6	0.7	mA
Timing (see Fig.3)						
f_{CLK}	maximum clock frequency		35	–	–	MHz
k_{CLK}	clock duty factor		40	–	60	%
t_r	clock rise time		–	–	5	ns
t_f	clock fall time		–	–	6	ns
$t_{SU;DAT}$	input data set-up time		4	–	–	ns
$t_{HD;DAT}$	input data hold time		4	–	–	ns
Voltage reference (pin 33, referenced to V_{SSA})						
V_{REF}	output voltage reference		1.180	1.242	1.305	V
Outputs						
OUTB, OUTR, OUTG analog outputs (pins 36, 44 and 40, referenced to V_{SSA}) for 1 kΩ load; see Table 1						
FSR	full-scale output voltage range		tbf	2.9	tbf	V
V_{os}	offset of analog voltage output		tbf	0.3	tbf	V
$V_{OUT(max)}$	maximum output voltage	data inputs = logic 1; note 1	tbf	3.20	tbf	V
$V_{OUT(min)}$	minimum output voltage	data inputs = logic 0; note 1	tbf	0.3	tbf	V
EB	effective bits	f_i = 4.43 MHz; f_{CLK} = 35 MHz	–	tbf	–	bits
Z_L	output load impedance		0.9	1.0	1.1	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transfer function (f_{CLK} = 35 MHz)						
ILE	DC integral linearity error		–	–	±1/2	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
CT	crosstalk DAC to DAC		–	−50	–	dB
	DAC to DAC matching		–	–	2	%
Switching characteristics (for 1 kΩ output load; C_L = 25 pF; f_{CLK} = 35 MHz; see Fig.4)						
t_{pd}	propagation delay time	1 LSB input to output	–	10	tbf	ns
t_{s1}	settling time	10% to 90% full-scale change	–	20	tbf	ns
t_{s2}	settling time	to ±1 LSB	–	50	tbf	ns
Output transients (glitches)						
V_g	area for 1 LSB change		–	tbf	–	LSB.ns

Note

1. V_{OUT} is directly proportional to V_{REF}.

Table 1 Input coding and DAC output voltages (typical values).

BINARY INPUT DATA	CODE	DAC OUTPUT VOLTAGES (V) OUTB, OUTR, OUTG Z_L = 1 kΩ
0000 0000	0	0.312
0000 0001	1	0.323
....	.	..
1000 0000	128	1.756
....	.	..
1111 1110	254	3.189
1111 1111	255	3.200

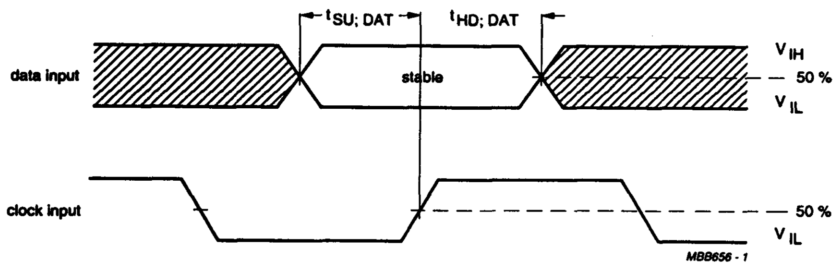


Fig.3 Input timing.

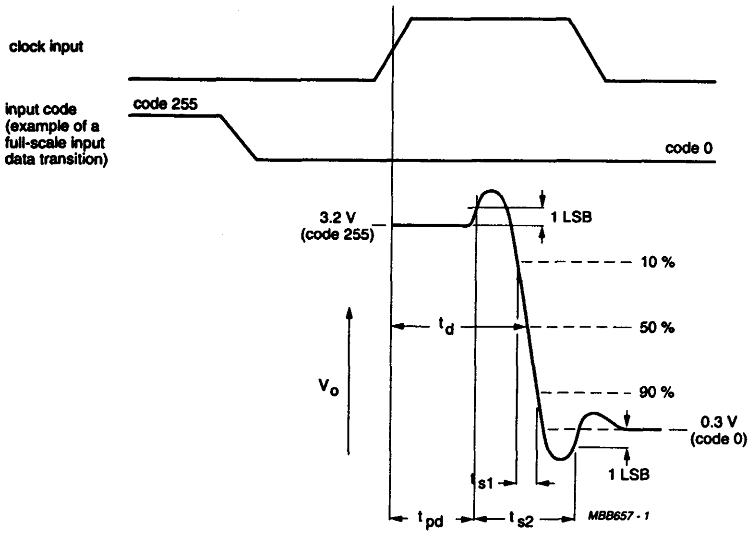


Fig.4 Switching timing.

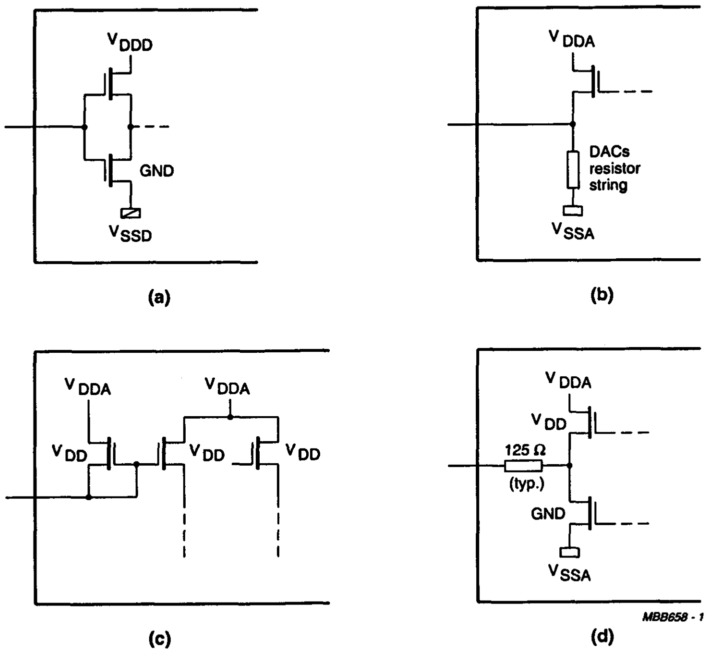
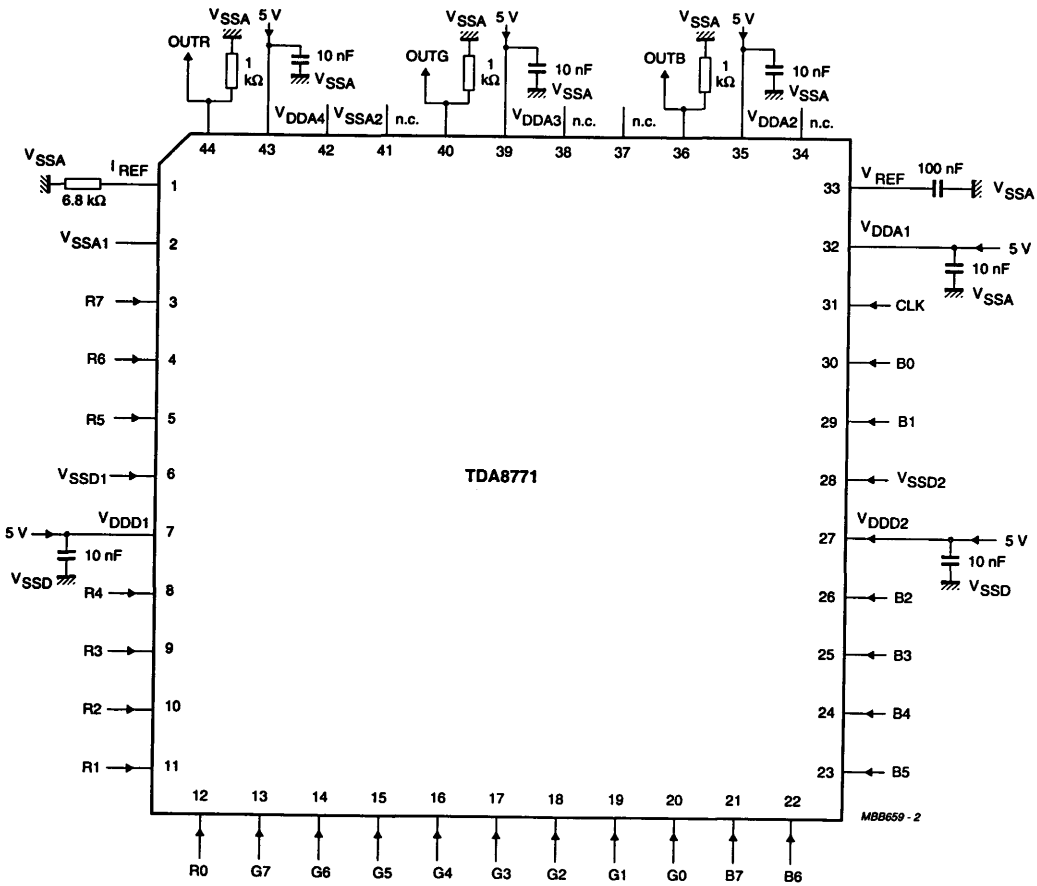


Fig.5 Internal circuitry (a) digital inputs; pins 3-5, 8-26, 29-31 (b) V_{REF}; pin 33 (c) I_{REF}; pin 1 (d) OUTR, G, B; pins 44, 40, 36.

APPLICATION INFORMATION



1. Analog and digital supplies should be separated and decoupled.
2. Supplies are not connected internally; also applicable to grounds.
3. See Fig.7 and Fig.9 examples of anti-aliasing filters.

Fig.6 Application diagram.

Filters

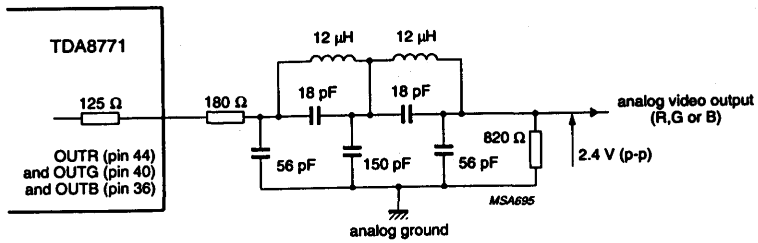
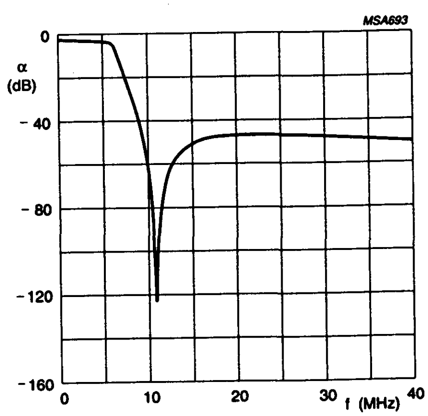


Fig.7 Example of anti-aliasing filter for 2.4 V typical output swing.



Characteristics

- Order 5; adapted CHEBYSHEV
- Ripple ρ ≥ 0.7 dB
- $f_{(-3\ dB)}$ = 6.2 MHz
- $f_{(NOTCH)}$ = 10.8 MHz

Fig.8 Frequency response for filter shown in Fig.7.

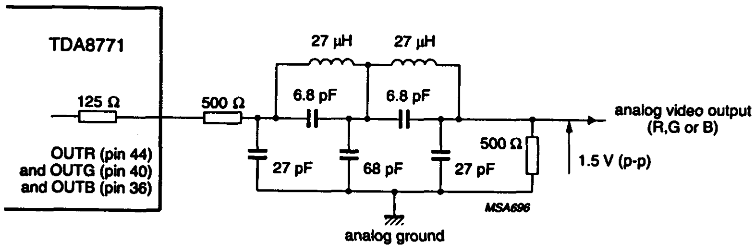
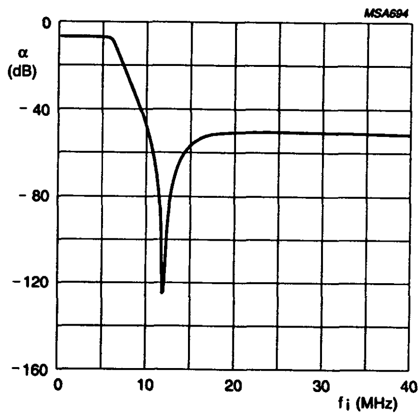


Fig.9 Example of anti-aliasing filter for 1.5 V typical output swing.



Characteristics

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \geq 0.25$ dB
- $f_{(-3\ dB)} = 5.6$ MHz
- $f_{(NOTCH)} = 11.7$ MHz

Fig.10 Frequency response for filter shown in Fig.9.

Triple 8-bit video digital-to-analog converter

TDA8772

FEATURES

- 8-bit resolution
- Sampling rate up to
  35 MHz for TDA8772H/3
  85 MHz for TDA8772H/8
- Internal reference voltage regulator
- No deglitching circuit required
- $\overline{SYNC}$, $\overline{BLANK}$ control inputs
- Drive capability with 3 different clocks
- 1 V output voltage range
- 75 Ω output load
- Single 5 V power supply
- 44-pin QFP package.

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing.

GENERAL DESCRIPTION

The TDA8772 is a triple 8-bit video digital-to-analog converter (DAC). It converts the digital input signals into analog voltage outputs at a maximum conversion rate of 35 MHz (TDA8772H/3) and 85 MHz (TDA8772H/8).

The DACs are based on resistor-string architecture with integrated output buffers. The output voltage range is determined by a built-in reference source.

The device is fabricated in a 5 V, 1 µm CMOS process that ensures high functionality with low power dissipation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	45	–	mA
I_{DDD}	digital supply current				
	TDA8772H/3	–	7	–	mA
	TDA8772H/8	–	16	–	mA
ILE	integral linearity error	–	–	±1/2	LSB
DLE	differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum conversion rate				
	TDA8772H/3	35	–	–	MHz
	TDA8772H/8	85	–	–	MHz
P_{tot}	total power dissipation (without load)				
	TDA8772H/3	–	260	–	mW
	TDA8772H/8	–	310	–	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				SAMPLING FREQUENCY
	PINS	PIN POSITION	MATERIAL	CODE	
TDA8772H/3	44	QFP	plastic	SOT307B	35 MHz
TDA8772H/8	44	QFP	plastic	SOT307B	85 MHz

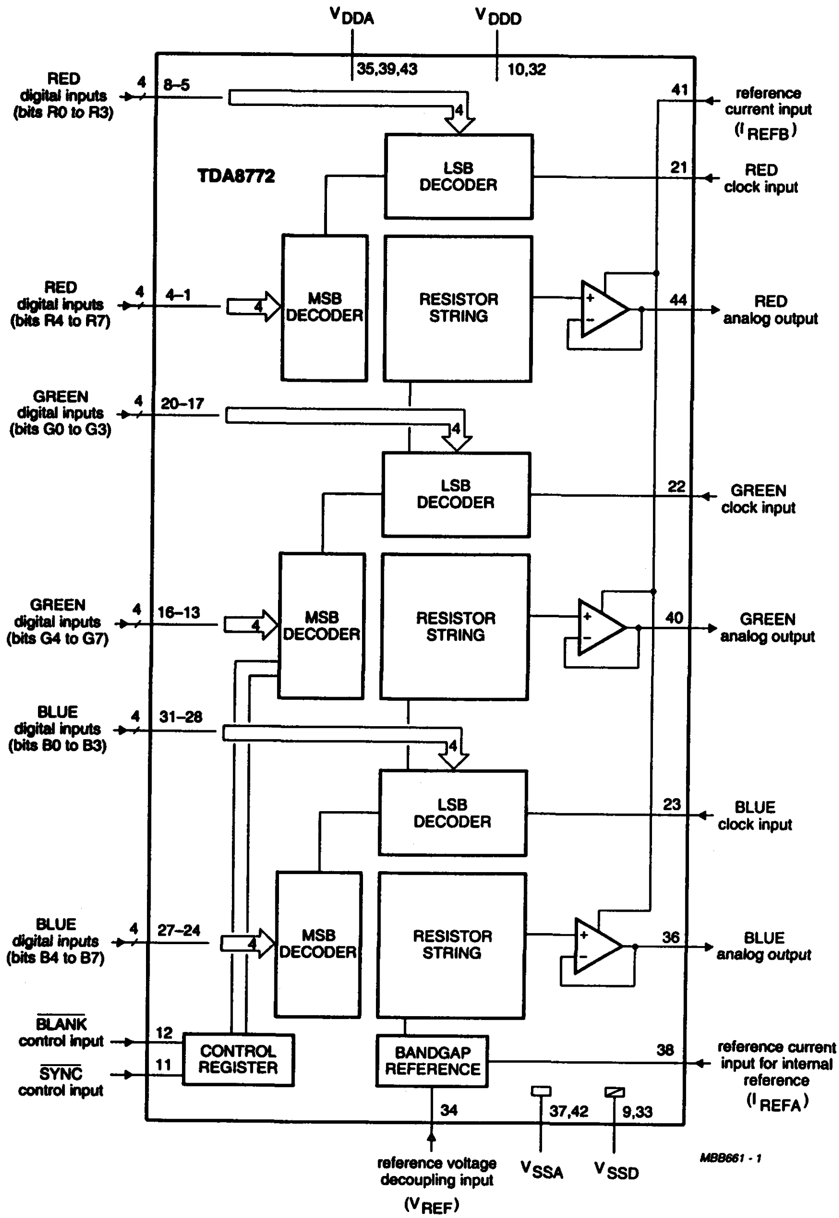


Fig.1 Block diagram.

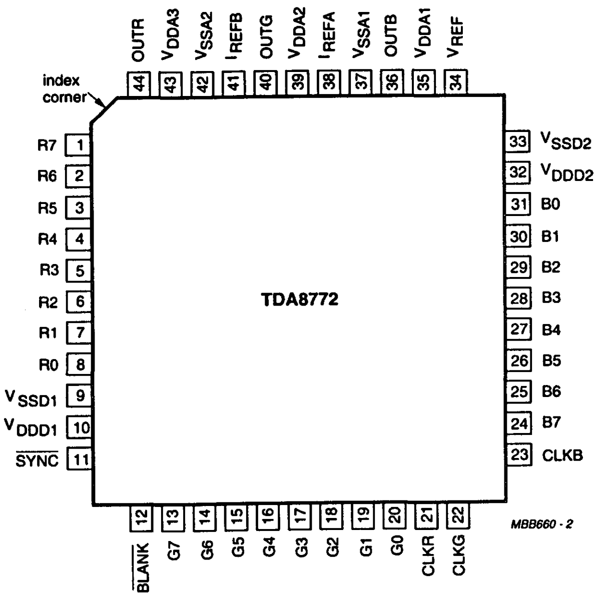


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
R7	1	RED digital input data; bit 7 (MSB)
R6	2	RED digital input data; bit 6
R5	3	RED digital input data; bit 5
R4	4	RED digital input data; bit 4
R3	5	RED digital input data; bit 3
R2	6	RED digital input data; bit 2
R1	7	RED digital input data; bit 1
R0	8	RED digital input data; bit 0 (LSB)
V_{SSD1}	9	digital supply ground 1
V_{DDD1}	10	digital supply voltage 1
$\overline{SYNC}$	11	composite sync control input; for GREEN channel only (active LOW)
$\overline{BLANK}$	12	composite blank control input (active LOW)
G7	13	GREEN digital input data; bit 7 (MSB)
G6	14	GREEN digital input data; bit 6

SYMBOL	PIN	DESCRIPTION
G5	15	GREEN digital input data; bit 5
G4	16	GREEN digital input data; bit 4
G3	17	GREEN digital input data; bit 3
G2	18	GREEN digital input data; bit 2
G1	19	GREEN digital input data; bit 1
G0	20	GREEN digital input data; bit 0 (LSB)
CLKR	21	RED clock input
CLKG	22	GREEN clock input
CLKB	23	BLUE clock input
B7	24	BLUE digital input data; bit 7 (MSB)
B6	25	BLUE digital input data; bit 6
B5	26	BLUE digital input data; bit 5
B4	27	BLUE digital input data; bit 4
B3	28	BLUE digital input data; bit 3
B2	29	BLUE digital input data; bit 2
B1	30	BLUE digital input data; bit 1
B0	31	BLUE digital input data; bit 0 (LSB)
V_{DDD2}	32	digital supply voltage 2
V_{SSD2}	33	digital supply ground 2
V_{REF}	34	decoupling input for reference voltage
V_{DDA1}	35	analog supply voltage 1
OUTB	36	BLUE analog output
V_{SSA1}	37	analog supply ground 1
I_{REFA}	38	reference current input for internal reference
V_{DDA2}	39	analog supply voltage 2
OUTG	40	GREEN analog output
I_{REFB}	41	reference current input for output buffers
V_{SSA2}	42	analog supply ground 2
V_{DDA3}	43	analog supply voltage 3
OUTR	44	RED analog output

LIMITING VALUES (TDA8772H/3 and TDA8772H/8)

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	−0.5	+6.5	V
V_{DDD}	digital supply voltage	−0.5	+6.5	V
V_{DDA} - V_{DDD}	supply voltage differences	−1.0	+1.0	V
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	−	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT307B)	75 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

TDA8772H/3 and TDA8772H/8 operating at 35 and 85 MHz respectively unless otherwise specified.
$V_{DDA} = V_{DDD}$ =4.5 V to 5.5 V; V_{SSA} and V_{SSD} shorted together; V_{DDA} - V_{DDD} = −0.5 V to +0.5 V; T_{amb} = 0 °C to +70 °C; unless otherwise specified (typical values measured at $V_{DDA} = V_{DDD}$ = 5 V and T_{amb} = 25 °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	R7-R0, G7-G0, B7-B0 = logic 0	–	45	tbf	mA
I_{DDD}	digital supply current					
	TDA8772H/3		–	7	tbf	mA
	TDA8772H/8		–	16	tbf	mA
Inputs						
Clock inputs (pins 21, 22 and 23)						
V_{IL}	LOW level input voltage		V_{SSD}−0.5	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}+0.5	V
$\overline{BLANK}$, $\overline{SYNC}$ inputs (pins 12 and 11; active LOW)						
V_{IL}	LOW level input voltage		V_{SSD}−0.5	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}+0.5	V
R, G, B digital inputs (pins 1-8; 13-20; 24-31)						
V_{IL}	LOW level input voltage		V_{SSD}−0.5	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}+0.5	V
I_{REFA} internal reference supply current (pin 38)						
I_I	input current		–	0.17	0.25	mA
I_{REFB} output buffer supply current (pin 41)						
I_I	input current		–	0.5	0.7	mA
Timing (C_L = 25 pF; R_L 75 Ω; see Fig.3)						
f_{CLK}	maximum clock frequency					
	TDA8772H/3		35	–	–	MHz
	TDA8772H/8		85	–	–	MHz
k_{CLK}	clock duty factor		40	–	60	%
t_r	clock rise time					
	TDA8772H/3		–	–	5	ns
	TDA8772H/8		–	–	3	ns
t_f	clock fall time					
	TDA8772H/3		–	–	5	ns
	TDA8772H/8		–	–	3	ns
$t_{SU;DAT}$	input data set-up time		4	–	–	ns
$t_{HD;DAT}$	input data hold time		2.5	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage reference (pin 34, referenced to V_{SSA})						
V_{REF}	output voltage reference		1.180	1.242	1.305	V
Outputs						
OUTB, OUTR, OUTG analog outputs (pins 36, 44 and 40, referenced to V_{SSA}) for 75 Ω load; see Tables 1 and 2						
FSR	full-scale output voltage range		tbf	1.0	tbf	V
V_{os}	offset of analog voltage output		tbf	0.83	tbf	V
$V_{OUT(max)}$	maximum output voltage	data inputs = logic 1; note 1	tbf	1.83	tbf	V
$V_{OUT(min)}$	minimum output voltage	data inputs = logic 0; note 1	tbf	0.83	tbf	V
EB	effective bits	f_i = 4.43 MHz				
		f_{CLK} = 35 MHz	–	tbf	–	bits
		f_{CLK} = 85 MHz	–	tbf	–	bits
Z_L	output load impedance		tbf	75	tbf	Ω
Transfer function (f_{CLK} = 85 MHz)						
ILE	integral linearity error		–	–	±1/2	LSB
DLE	differential linearity error		–	–	±1/2	LSB
CT	crosstalk DAC to DAC		–	−45	–	dB
	DAC to DAC matching		–	–	2	%
Switching characteristics (for 75 Ω output load; see Fig.4)						
t_{pd}	propagation delay time	1 LSB input to output	–	tbf	–	ns
t_{s1}	settling time	10% to 90% full-scale change	–	tbf	–	ns
t_{s2}	settling time	to ±1 LSB	–	tbf	–	ns
Output transients (glitches)						
V_g	area for 1 LSB change		–	tbf	–	LSB.ns

Note

1. V_{OUT} is directly proportional to V_{REF}.

Table 1 Input coding and DAC output voltages (typical values).

BINARY INPUT DATA (SYNC = BLANK = 0)	CODE	DAC OUTPUT VOLTAGES (V) OUTB, OUTR, OUTG $Z_L = 75\ \Omega$
0000 0000	0	0.830
0000 0001	1	0.834
....	.	..
1000 0000	128	1.330
....	.	..
1111 1110	254	1.826
1111 1111	255	1.830

Table 2 Input coding and DAC output voltages (typical values).

BINARY INPUT DATA	$\overline{\text{SYNC}}$ (pin 11)	$\overline{\text{BLANK}}$ (pin 12)	DAC OUTPUT VOLTAGES (V)	
			OUTG (pin 40)	OUTR/B (pin 44, 36)
....	x	1	see Table 1	see Table 1
....	1	0	0.830	0.830
....	0	0	0.440	

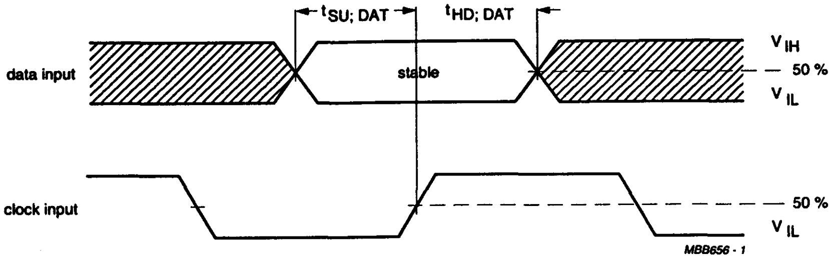


Fig.3 Input timing.

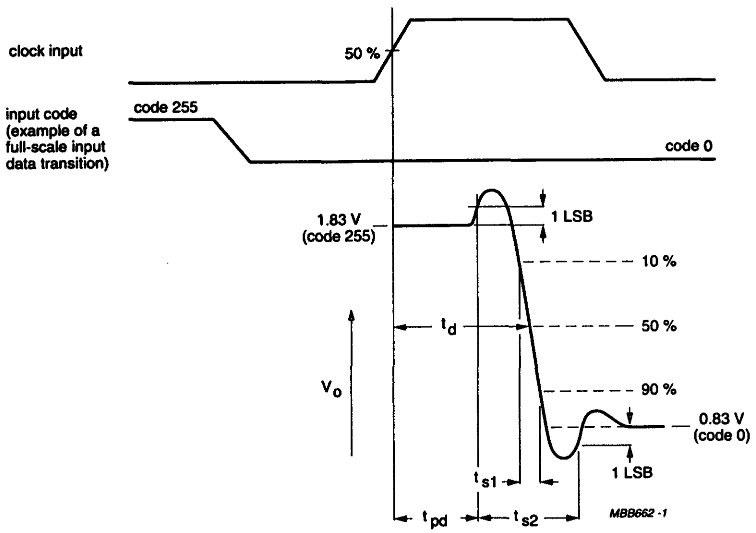


Fig.4 Switching timing.

Triple 8-bit video digital-to-analog converter TDA8772

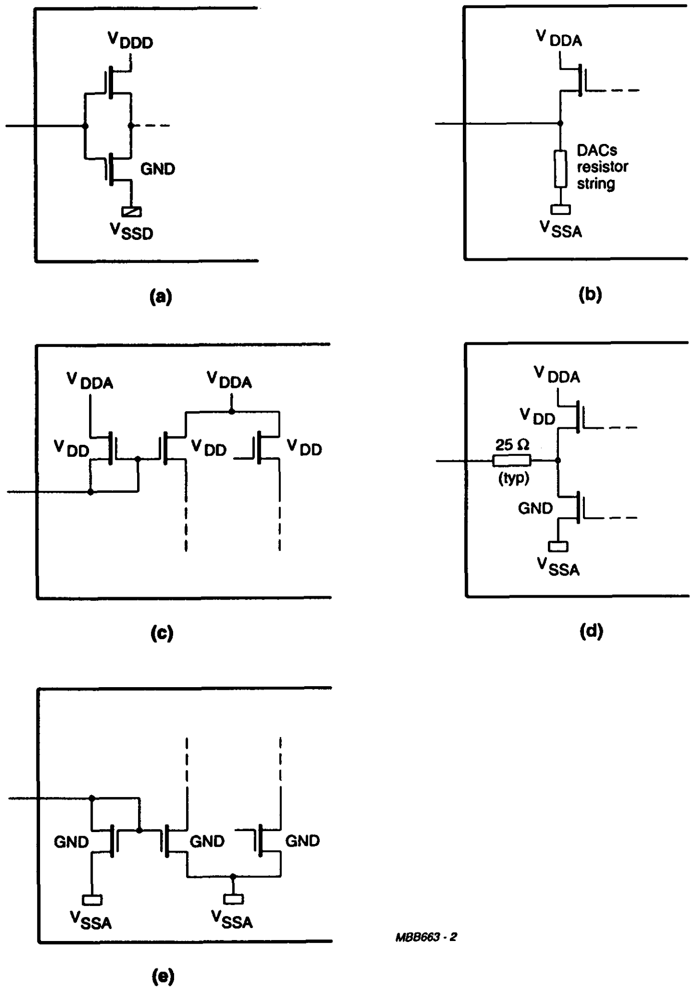
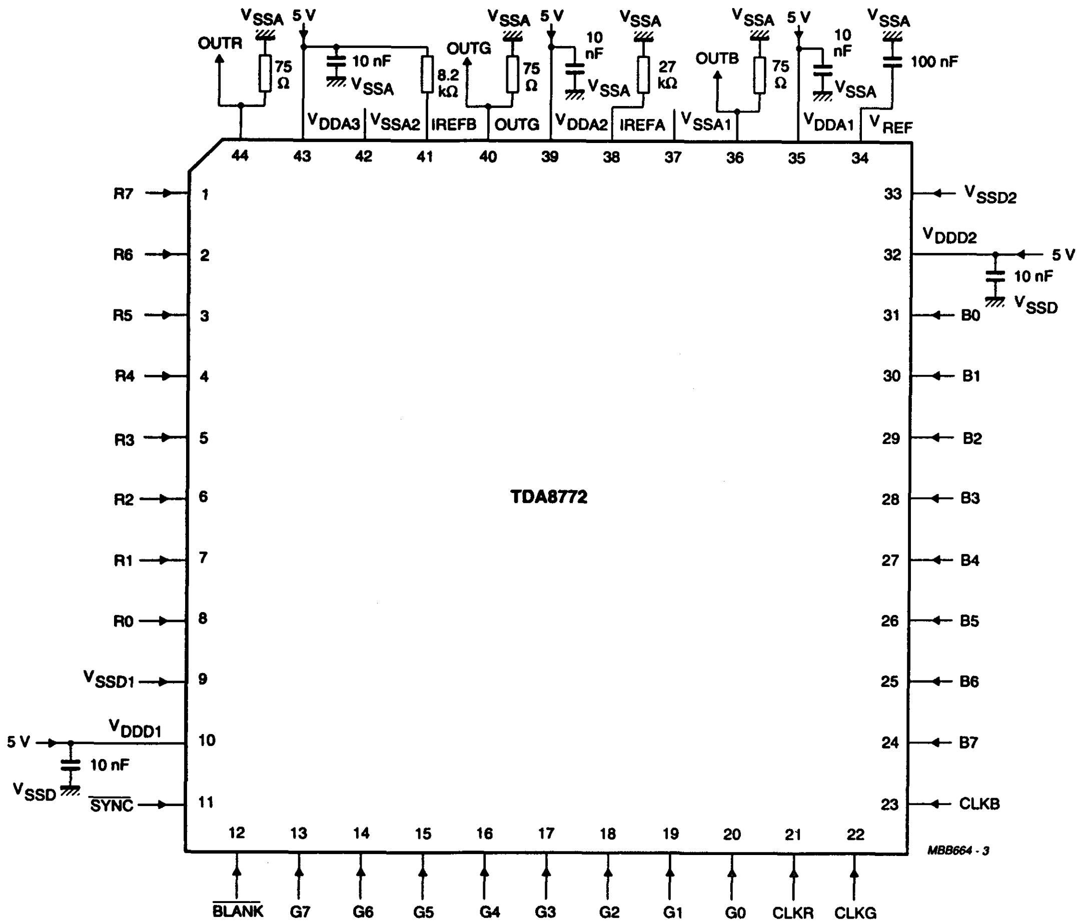


Fig.5 Internal circuitry (a) digital inputs; pins 1-8, 11-31 (b) V_{REF}; pin 34 (c) I_{REFA}; pin 38 (d) OUTR, G, B; pins 44, 40, 36 (e) I_{REFB}; pin 41.

APPLICATION INFORMATION



1. Analog and digital supplies should be separated and decoupled.
2. Supplies are not connected internally; also applicable to grounds.
3. See Fig.7 example of anti-aliasing filter.

Fig.6 Application diagram.

Filters

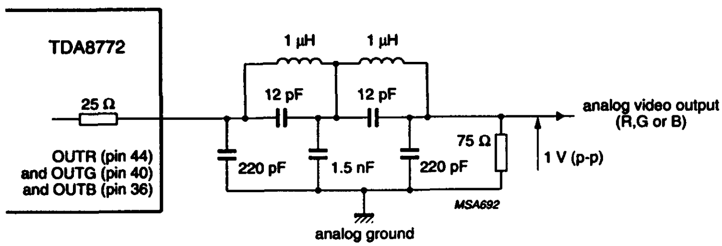
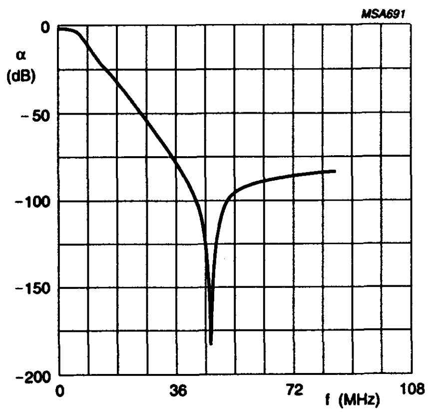


Fig.7 Example of anti-aliasing filter for 1 V typical output swing.



Characteristics

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \geq 0.6$ dB
- $f_{(-3\ dB)} = 6.5$ MHz
- $f_{(NOTCH)} = 46$ MHz

Fig.8 Frequency response for filter shown in Fig.7.

PAL/NTSC/SECAM decoder/sync processor

TDA9141

FEATURES

- Multistandard PAL, NTSC and SECAM
- I^2C-bus controlled
- I^2C-bus addresses can be selected by hardware
- Alignment free
- Few external components
- Designed for use with baseband delay lines
- Integrated video filters
- CVBS or YC input with automatic detection
- CVBS output
- Vertical divider system
- Two-level sandcastle signal
- V_A synchronization pulse (3-state)
- H_A synchronization pulse or clamping pulse CLP input/output
- Line-locked clock output or stand-alone I^2C-bus output port
- Stand-alone I^2C-bus input/output port
- Colour matrix and fast YUV switch
- Comb filter enable input/output with subcarrier frequency.

GENERAL DESCRIPTION

The TDA9141 is an I^2C-bus controlled, alignment-free PAL/NTSC/SECAM decoder/sync processor. The TDA9141 has been designed for use with baseband chrominance delay lines, and has a combined subcarrier frequency/comb filter enable signal for communication with a PAL comb filter.

The IC can process CVBS signals and Y/C input signals. The input signal is available on an output pin, in the event of a Y/C signal, it is added into a CVBS signal.

The sync processor provides a two-level sandcastle, a horizontal pulse (CLP or H_A pulse, bus selectable) and a vertical (V_A) pulse. When the H_A pulse is selected a line-locked clock (LLC) signal is available at the output port pin.

A fast switch can select either the internal Y signal with the UV input signals, or YUV signals made of the RGB input signals. The RGB input signals can be clamped with either the internal or an external clamping signal (search tuning mode).

Two pins with an input/output port and an output port of the I^2C-bus are available.

The I^2C-bus address of the TDA9141 is hardware programmable.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9141	32	SDIL	plastic	SOT232

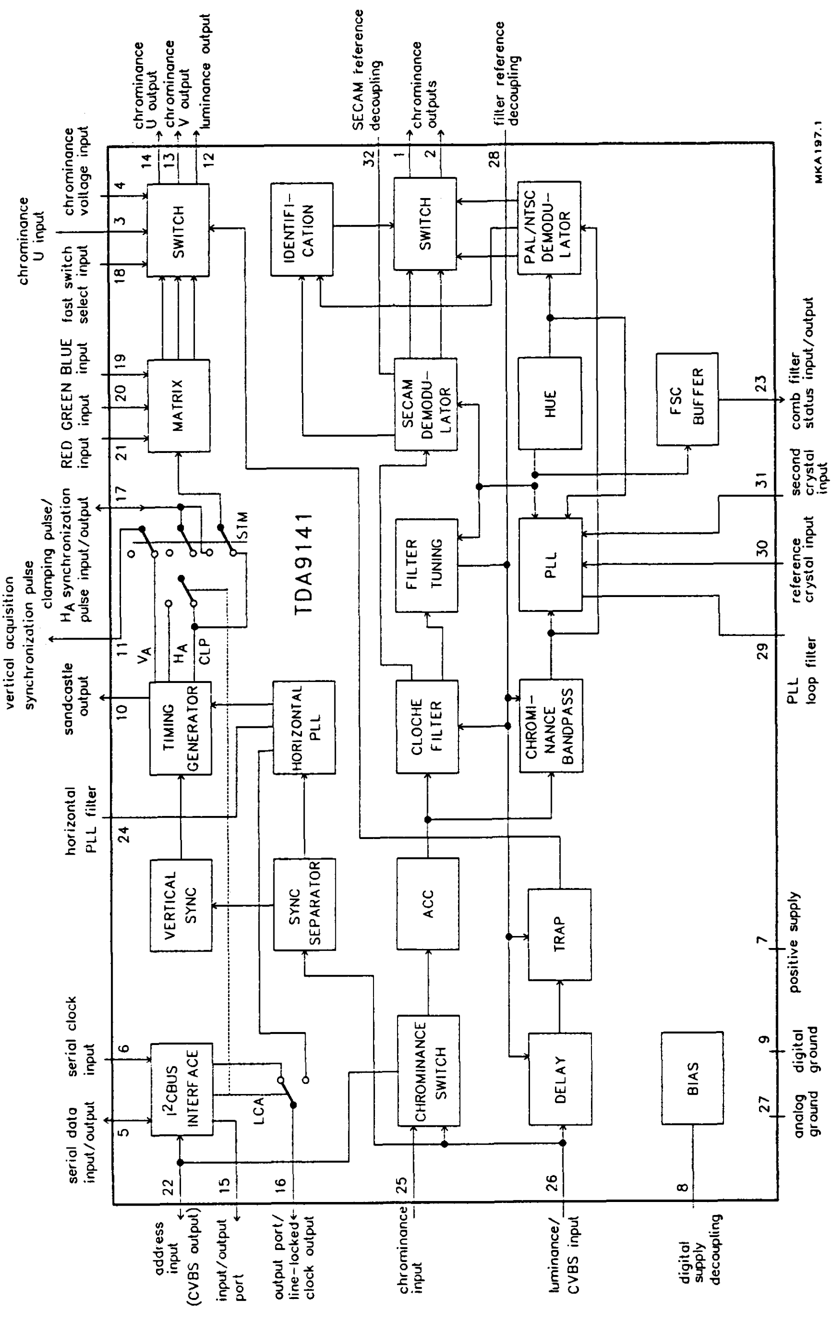


Fig.1 Block diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current		–	45	–	mA
$V_{26(p\text{-}p)}$	CVBS input voltage (peak-to-peak value)	top sync - white	–	1.0	–	V
$V_{26(p\text{-}p)}$	luminance input voltage (peak-to-peak value)	top sync - white	–	1.0	–	V
$V_{22(p\text{-}p)}$	chrominance burst input voltage (peak-to-peak value)		–	0.3	–	V
V_{12}	luminance black-white output voltage		–	1.0	–	V
$V_{14(p\text{-}p)}$	U output voltage (peak-to-peak value)	standard colour bar	–	1.33	–	V
$V_{13(p\text{-}p)}$	V output voltage (peak-to-peak value)	standard colour bar	–	1.05	–	V
V_{10}	sandcastle blanking voltage level		–	2.5	–	V
V_{10}	sandcastle clamping voltage level		–	4.5	–	V
V_{11}	V_A output voltage		–	5.0	–	V
V_{17}	H_A output voltage		–	5.0	–	V
$V_{16(p\text{-}p)}$	LLC output voltage amplitude (peak-to-peak value)		–	500	–	mV
$V_{21,20\ 19(p\text{-}p)}$	RGB input voltage (peak-to-peak value)	0 to 100% saturation	–	0.7	–	V
$V_{clamp\ I/O}$	clamping pulse input/output voltage		–	5.0	–	V
V_{sub}	subcarrier output voltage amplitude (peak-to-peak value)		–	200	–	mV
$V_{15,16}$	O port output voltage		–	5.0	–	V

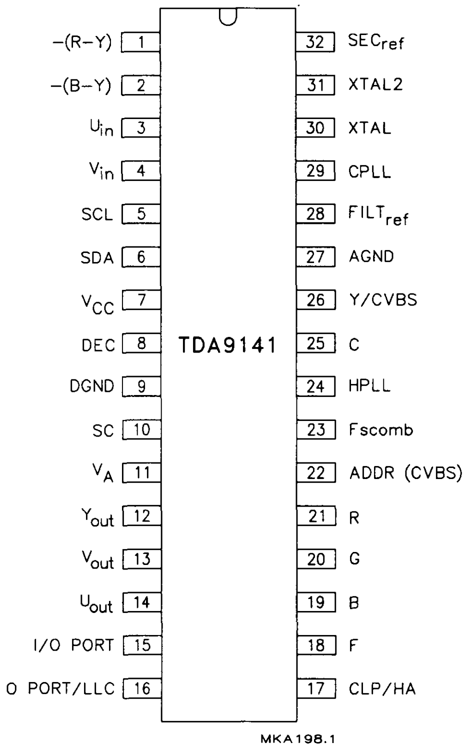


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
−(R−Y)	1	chrominance output
−(B−Y)	2	chrominance output
U_{in}	3	chrominance U input
V_{in}	4	chrominance voltage input
SCL	5	serial clock input
SDA	6	serial data input/output
V_{CC}	7	positive supply input
DEC	8	digital supply decoupling
DGND	9	digital ground
SC	10	sandcastle output
V_A	11	vertical acquisition synchronization pulse
Y_{out}	12	luminance output
V_{out}	13	chrominance V output
U_{out}	14	chrominance U output
I/O PORT	15	input/output port
O PORT/LLC	16	output port/line-locked clock output
CLP/HA	17	clamping pulse/H_A synchronization pulse input/output
F	18	fast switch select input
B	19	BLUE input
G	20	GREEN input
R	21	RED input
ADDR (CVBS)	22	I²C-bus address input (CVBS output)
Fscomb	23	comb filter status input/output
HPLL	24	horizontal PLL filter
C	25	chrominance input
Y/CVBS	26	luminance/CVBS input
AGND	27	analog ground
$FILT_{ref}$	28	filter reference decoupling
CPLL	29	colour PLL filter
XTAL	30	reference crystal input
XTAL2	31	second crystal input
SEC_{ref}	32	SECAM reference decoupling

FUNCTIONAL DESCRIPTION

General

The TDA9141 is an I²C-bus controlled, alignment-free PAL/NTSC/SECAM colour decoder/sync processor which has been designed for use with baseband chrominance delay lines. In the standard operating mode the I²C-bus address is 8A. If the address input is connected to the positive rail the address will change to 8E.

Input switch

WARNING: THE VOLTAGE ON THE CHROMINANCE PIN MUST NEVER EXCEED 5.5 V. IF IT DOES THE IC ENTERS A TEST MODE.

The TDA9141 has a two pin input for CVBS or YC signals which can be selected via the I²C-bus. The input selector also has a position in which it automatically detects whether a CVBS or YC signal is on the input. In this input selector position, standard identification first takes place on an added Y/CVBS and C input signal. After that, both chrominance signal input amplitudes are checked once and the input with the strongest chrominance burst signal is selected. The input switch status is read out by the I²C-bus via output bit YC.

CVBS output

In the standard operating mode with the I²C-bus address 8A, a CVBS output signal is available on the address pin, which represents either the CVBS input signal or the Y/C input signal, added into a CVBS signal

RGB colour matrix

WARNING: THE VOLTAGE ON THE UIN PIN MUST NEVER EXCEED 5.5 V. IF IT DOES THE IC ENTERS A TEST MODE.

The TDA9141 has a colour matrix to convert RGB input signals into YUV signals. A fast switch, controlled by the signal on pin F and enabled by the I²C-bus via EFS (enable fast switch), can select between these YUV signals and the YUV signals of the decoder. The Y signal is internally connected to the switch. The –(R–Y) and –(B–Y) output signals of the decoder have to first be delayed in external baseband chrominance delay lines. The outputs of the delay lines must be connected to the UV input pins. If the RGB signals are not synchronous with the selected decoder input signal, clamping of the RGB input signals is possible by I²C-bus selection of STM (search tuning mode), EFS and by feeding an external clamping signal to the CLP pin.
Also in search tuning mode the VA output will be in a high impedance OFF-state.

Standard identification

The standards which the TDA9141 can decode are dependent on the choice of external crystals. If a 4.4 MHz and a 3.6 MHz crystal are used then SECAM, PAL 4.4/3.6 and NTSC 4.4/3.6 can be decoded. If two 3.6 MHz crystals are used then only PAL 3.6 and NTSC 3.6 can be decoded. Which 3.6 MHz standards can be decoded is dependent on the exact frequencies of the 3.6 MHz crystals. In an application where not all standards are required only one crystal is sufficient (in this instance the crystal must be connected to the reference crystal input (pin 30)). If a 4.4 MHz crystal is used it must always be connected to pin 30. Both crystals are used to provide a reference for the filters and the horizontal PLL, however, only the reference crystal is used to provide a reference for the SECAM demodulator.
To enable the calibrating circuits to be adjusted exactly two bits from I²C-bus subaddress 00 are used to indicate which crystals are connected to the IC.

The standard identification circuit is a digital circuit without external components; the search loop is illustrated in Fig.3.

The decoder (via the I²C-bus) can be forced to decode either SECAM or PAL/NTSC (but not PAL or NTSC). Crystal selection can also be forced. Information concerning which standard and which crystal have been selected and whether the colour killer is ON or OFF is provided by the read out. Using the forced-mode does not affect the search loop, it does, however, prevent the decoder from reaching or staying in an unwanted state. The identification circuit skips impossible standards (e.g. SECAM when no 4.4 MHz crystal is fitted) and illegal standards (e.g. is forced mode). To reduce the risk of wrong identification PAL has priority over SECAM (only line identification is used for SECAM).

Integrated filters

All filters, including the luminance delay line, are an integral part of the IC. The filters are gyrator-capacitor type filters. The resonant frequency of the filters is controlled by a circuit that uses the active crystal to tune the SECAM Cloche filter during the vertical flyback time. The remaining filters and the luminance delay line are matched to this filter. The filters can be switched to either 4.43 MHz, 4.28 MHz or 3.58 MHz irrespective of the frequency of the active crystal. The switching is controlled by the identification circuit.
In YC mode the chrominance notch filter is bypassed, to preserve full

signal bandwidth.
For a CVBS signal the chrominance notch filter can be bypassed by I²C-bus selection of TB (trap bypass).
The luminance delay line delivers the Y signal to the output 60 ns after the –(R–Y) and –(B–Y) signals have arrived at their outputs. This compensates for the delay of the external chrominance delay lines.

Colour decoder

The PAL/NTSC demodulator employs an oscillator that can operate with either crystal (3.6 or 4.4 MHz). If the I²C-bus indicates that only one crystal is connected it will always connect to the crystal on the reference crystal input (pin 30).

The Hue signal, which is adjustable via the I²C-bus, is gated during the burst for NTSC signals.

The SECAM demodulator is an auto-calibrating PLL demodulator which has two references. The reference crystal, to force the PLL to the desired free-running frequency and the bandgap reference, to obtain the correct absolute value of the output signal. The VCO of the PLL is calibrated during each vertical blanking period, when the IC is in search mode or SECAM mode. If the reference crystal is not 4.4 MHz the decoder will not produce the correct SECAM signals.

The frequency of the active crystal is fed to the Fscomb output, which can be connected to an external comb filter IC. The DC value on this pin contains the comb enable information. Comb enable is true when bus bit ECMB is HIGH. If ECMB is LOW, the subcarrier frequency is suppressed. The external comb filter can force the DC value of Fscomb LOW, as pin Fscomb also acts as input pin. In this event the subcarrier frequency is still present. If the DC value of Fscomb is HIGH, the input switch is always forced in Y/C mode, indicated by bus bit YC.

Sync processor (φ1 loop)

The main part of the sync circuit is a 432 x f_H (6.75 MHz) oscillator the frequency of which is divided by 432 to lock the Phase 1 loop to the incoming signal. The time constant of the loop can be forced by the I²C-bus (fast or slow). If required the IC can select the time constant, depending on the noise content of the input signal and whether the loop is phase-locked or not (medium or slow). The free-running frequency of the oscillator is determined by a digital control circuit that is locked to the active crystal.

When a power-on-reset pulse is detected the frequency of the oscillator is switched to a frequency greater than 6.75 MHz to protect the horizontal output transistor. The oscillator frequency is reset to 6.75 MHz when the crystal indication bits have been loaded into the IC. To ensure that this procedure does not fail it is absolutely necessary to send subaddress 00 before subaddress 01. Subaddress 00 contains the crystal indication bits and when subaddress 01 is received the line oscillator calibration will be initiated (for the start-up procedure after power-on reset detection see the I²C-bus protocol. The calibration is terminated when the oscillator frequency reaches 6.75 MHz. The oscillator is again calibrated when an out-of-lock condition with the input signal is detected by the coincidence detector. Again the calibration will be terminated when the oscillator frequency reaches 6.75 MHz.
The Phase 1 loop can be opened using the I²C-bus. This is to facilitate On Screen Display (OSD) information. If there is no input signal or a very noisy input signal the phase 1 loop can be opened to provide a stable line frequency and thus a stable picture.

The sync part also delivers a two-level sandcastle signal, which provides a combined horizontal and vertical blanking signal and a clamping pulse for the display section of the TV.

Vertical divider system

The vertical divider system has a fully integrated vertical sync separator. The divider can accommodate both 50 and 60 Hz systems; it can either locate the field frequency automatically or it can be forced to the desired system via the I²C-bus. A block diagram of the vertical divider system is illustrated in Fig.4. The divider system operates at twice the horizontal line frequency. The line counter receives enable pulses at this line frequency, thereby counting two pulses per line. A state diagram of the controller is illustrated in Fig.5. Because it is symmetrical only the right hand part will be described.

Depending on the previously found field frequency, the controller will be in one of the COUNT states. When the line counter has counted 488 pulses (i.e. 244 lines of the video input signal) the controller will move to the next state depending on the output of the norm counter. This can be either NORM, NEAR_NORM or NO_NORM depending on the position of the vertical sync pulse in the previous fields. When the controller is in the NORM state it generates the vertical sync pulse (VSP) automatically and then, when the line counter is at LC = 626, moves to the WAIT state. In this condition it waits for the next pulse of the double line frequency signal and then moves to the COUNT state of the current field frequency. When the controller returns to the COUNT state the line counter will be reset half a line after the start of the vertical sync pulse of the video input signal.

When the controller is in the NEAR_NORM state it will move to the COUNT state if it detects the vertical sync pulse within the NEAR_NORM window (i.e. 622 < LC < 628). If no vertical sync pulse is detected, the controller will move back to the COUNT state when the line counter reaches LC = 628. The line counter will then be reset.

When the controller is in the NO_NORM state it will move to the COUNT state when it detects a vertical sync pulse and reset the line counter. If a vertical sync pulse is not detected before LC = 722 (if the Phase 1 loop is locked in forced mode) it will move to the COUNT state and reset the line counter. If the Phase 1 loop is not locked the controller will move back to the COUNT state when LC = 628.

The forced mode option keeps the controller in either the left-hand side (60 Hz) or the right-hand side (50 Hz) of the state diagram.

Figure 6 illustrates the state diagram of the norm counter which is an up/down counter that counts up if it finds a vertical sync pulse within the selected window. In the NEAR_NORM and NORM states the first correct vertical sync pulse after one or more incorrect vertical sync pulses is processed as an incorrect pulse. This procedure prevents the system from staying in the NEAR_NORM or NORM state if the vertical sync pulse is correct in the first field and incorrect in the second field. If no vertical sync pulse is found in the selected window this will always result in a down pulse for the norm counter.

Output port and input/output port

Two stand-alone ports are available for external use. These ports are I²C-bus controlled, the output port by bus bit OPB and the input/output port by bus bit OPA. Bus bit OPA is an open-drain output, to enable input port functioning. The pin status is read out by bus via output bit IP.

Sandcastle

Figure 7 illustrates the timing of the acquisition sandcastle (ASC) and the V_A pulse with respect to the input signal. The sandcastle signal is in accordance with the 2-level 5 V sandcastle format. An external vertical guard current can overrule the sink current to enable blanking purposes.

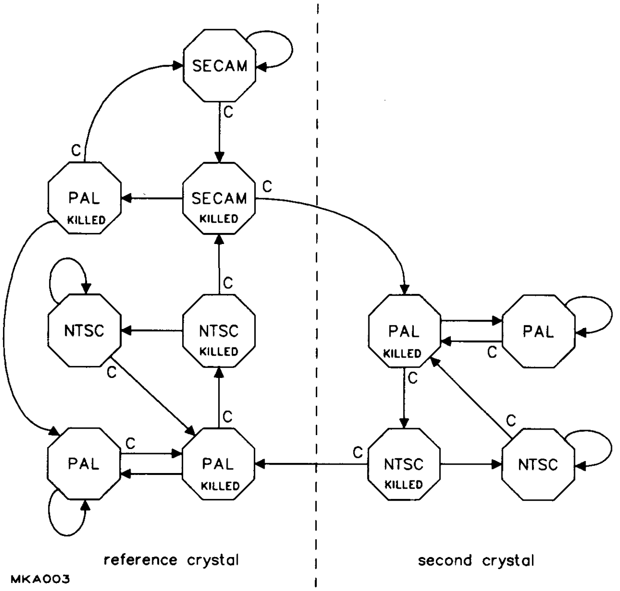


Fig.3 Search loop of the identification circuit.

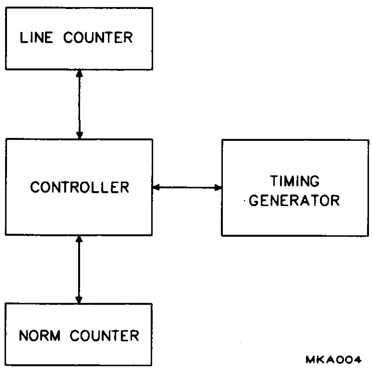


Fig.4 Block diagram of the vertical divider system.

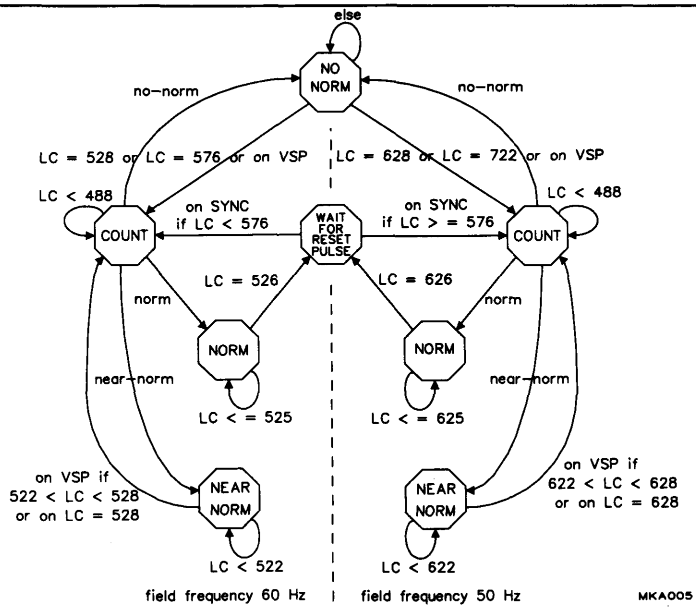


Fig.5 State diagram of the vertical divider system.

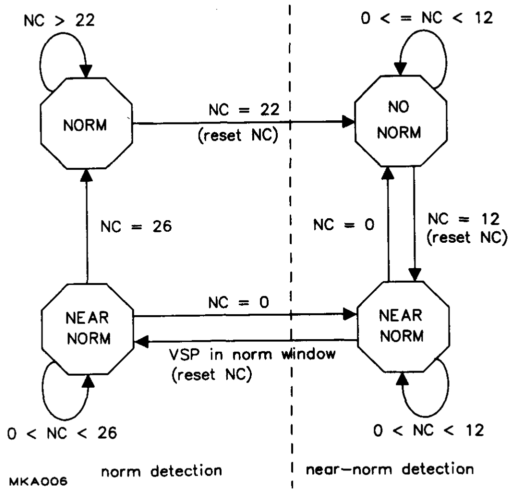


Fig.6 State diagram of the norm counter.

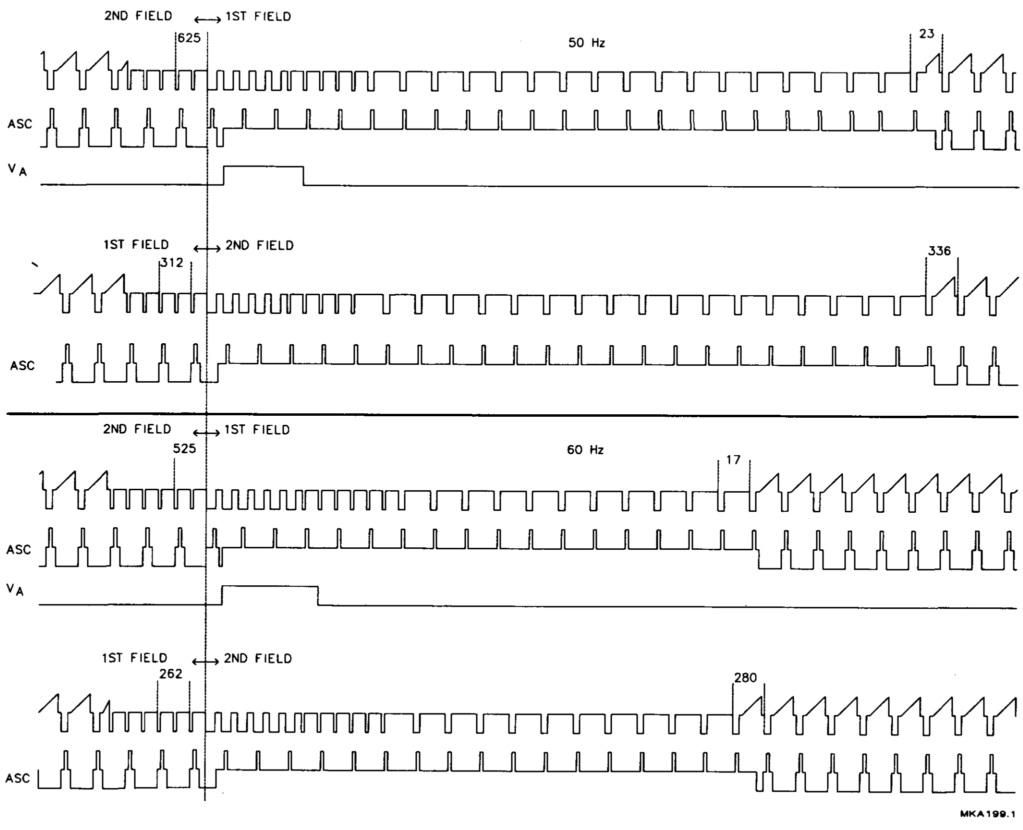


Fig.7 Acquisition sandcastle signal and V_A pulse timing diagram.

Table 1 Slave address (8A).

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	0	0	1	X	1	X

Table 2 Inputs.

SUBADDRESS	MSB						LSB
00	INA	INB	TB	ECMB	FOA	FOB	XA	XB
01	FORF	FORS	OPA	OPB	POC	FM	SAF	FRQF
02	EFS	STM	HU5	HU4	HU3	HU2	HU1	HU0
03	LCA	–	–	–	–	–	–	–

Table 3 Outputs.

ADDRESS	POR	FSI	YC	SL	IP	SAK	SBK	FRQ

I²C-bus protocol

If the address input is connected to the positive supply the address will change from 8A to 8E.

Valid subaddresses = 00 to 0F
Auto-increment mode available for subaddresses.

Start-up procedure: read the status byte until POR = 0; send subaddress 00 with the crystal indicator bits (XA and XB) indicating that only one crystal is connected to the IC; wait for 250 ms; send subaddress 01; wait for at least 100 ms; set XA, XB to the actual crystal configuration.
Each time before the data in the IC is refreshed , the staus byte must be read. If POR = 1, then the above procedure must be carried out to restart the IC.
Failure to stick to the above procedure may result in an incorrect line frequency after power-up or a power-dip.

INPUT SIGNALS

Table 4 Source select.

INA	INB	SOURCE
0	0	CVBS
0	1	YC
1	–	auto CVBS/YC

Table 5 Trap bypass.

TB	CONDITION
0	trap not bypassed
1	trap bypassed

Table 6 Comb filter enable.

ECMB	CONDITION
0	comb filter disabled
1	comb filter enabled

Table 7 Phase 1 time constant.

FOA	FOB	MODE
0	0	auto
0	1	slow
1	–	fast

Table 8 Crystal indication.

XA	XB	CRYSTAL
0	0	2 x 3.6 MHz
0	1	1 x 3.6 MHz
1	0	1 x 4.4 MHz
1	1	3.6 and 4.4 MHz

Table 9 Forced field frequency.

FORF	FORS	FIELD FREQUENCY
0	0	auto; 60 Hz if no lock
0	1	60 Hz
1	0	50 Hz
1	1	auto; 50 Hz if no lock

Table 10 Output value I/O port.

OPA	CONDITION
0	LOW
1	HIGH

Table 11 Output value O port.

OPB	CONDITION
0	LOW
1	HIGH

Table 12 Phase 1 loop control.

POC	CONDITION
0	phase one loop closed
1	phase one loop open

Table 13 Forced standard.

FM	SAF	FRQF	STANDARD
0	–	–	auto search
1	0	0	PAL/NTSC second crystal
1	0	1	PAL/NTSC reference crystal
1	1	0	illegal
1	1	1	SECAM reference crystal

Note to Table 13

If XA and XB indicate that only one crystal is connected to the IC and FM and FRQF force it to use the second crystal the colour will be switched off.

Table 14 Fast switch enable.

EFS	CONDITION
0	fast switch disabled
1	fast switch enabled

Table 15 Search tuning mode.

STM	CONDITION
0	search tuning mode off
1	search tuning mode on

Table 16 Hue.

FUNCTION	ADDRESS	DIGITAL NUMBER
hue	HU5 to HU0	000000 = −45 ° 111111 = +45 °

Table 17 Line-locked clock active.

LCA	CONDITION
0	OPB/CLP mode
1	LLC/HA mode

OUTPUT SIGNALS

Table 18 Power-on reset.

POR	CONDITION
0	normal mode
1	power-down mode

Table 19 Field frequency indication.

FSI	CONDITION
0	50 Hz
1	60 Hz

Table 20 Input switch mode.

YC	CONDITION
0	CVBS mode
1	YC mode

Table 21 Phase 1 lock indication.

SL	CONDITION
0	not locked
1	locked

Table 22 Input value I/O port.

IP	CONDITION
0	LOW
1	HIGH

Table 23 Standard read-out.

SAK	SBK	FRQ	STANDARD
0	0	0	PAL second crystal
0	0	1	PAL reference crystal
0	1	0	NTSC second crystal
0	1	1	NTSC reference crystal
1	0	0	illegal forced mode
1	0	1	SECAM reference crystal
1	1	–	colour off

LIMITING VALUES

In accordance with the Absolute Maximum Rating System. (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	positive supply voltage		–	8.8	V
I_{CC}	supply current		–	60	mA
P_{tot}	total power dissipation		–	530	mW
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−10	+65	°C
ESD	electrostatic discharge (on all pins)				
	Human body model	note 1	−2000	+2000	V
	Machine model	note 2	−200	+200	V

Notes to the limiting values

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
2. Equivalent to discharging a 200 pF capacitor via a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	48 K/W

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current		–	45	–	mA
P_{tot}	total power dissipation		–	360	–	mW
Input switch						
Y/CVBS INPUT (PIN 26)						
$V_{26(p-p)}$	input voltage (peak-to-peak value)	top sync - white	–	1.0	1.43	V
Z_I	input impedance		60	–	–	kΩ
C INPUT (PIN 25)						
$V_{25(p-p)}$	input burst voltage (peak-to-peak value)		–	0.3	0.43	V
Z_I	input impedance		60	–	–	kΩ
CVBS OUTPUT (PIN 22) ONLY ADDRESS 8A						
$V_{22(p-p)}$	output voltage (peak-to-peak value)	top sync - white	–	1.0	–	V
Z_O	output impedance		–	–	500	Ω
V_{tsl}	top sync voltage level		–	2.8	–	V
Bias generator (pin 8)						
V_8	digital supply voltage		–	5.0	–	V
Subcarrier regeneration						
GENERAL						
CR	catching range	note 1				
	reference crystal 4.4 MHz		±400	–	–	Hz
	reference crystal 3.6 MHz		tbf	–	–	Hz
	second crystal 3.6 MHz		±300	–	–	Hz
φ	phase shift					
	for 400 Hz deviation	4.4 MHz	–	–	5	deg
	for 300 Hz deviation	3.6 MHz	–	–	5	deg
TC	temperature coefficient of oscillator		–	tbf	–	Hz/K
Z_I	input impedance					
	reference crystal input		–	1.0	–	kΩ
	second crystal input		–	1.5	–	kΩ
V_{dep}	supply voltage dependency		–	tbf	–	V
FSCOMB OUTPUT (PIN 23)						
$V_{sub(p-p)}$	subcarrier output amplitude (peak-to-peak value)	C_L = 15 pF	150	200	300	mV
V_{cen}	comb enable voltage level		4.0	4.2	–	V
V_{cdis}	comb disable voltage level		–	0.8	1.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{sink}	minimum sink current to force output to comb disable level		0.4	–	2.0	mA
R_{GND}	value of grounded resistor to force output to comb disable level		0.4	–	2.0	kΩ
ACC						
	ACC control range		−20	–	+5	dB
	change of −(R−Y) and −(B−Y) signals over ACC range		–	–	1	dB
	colour killer threshold PAL/NTSC SECAM		 – –	 −25 −23	 – –	 dB dB
	kill - unkill hysteresis		–	3	–	dB
Demodulators −(R−Y) and −(B−Y) outputs (pins 1 and 2)						
	ratio of −(R−Y) and −(B−Y) signals	standard colour bar	1.20	1.27	1.34	
TC	temperature coefficient of −(R−Y) and −(B−Y) amplitude		–	tbf	–	Hz/K
	spread of −(R−Y) and −(B−Y) ratio between standards		−1	–	+1	dB
V_1	output level of −(R−Y) during blanking		–	2.0	–	V
V_2	output level of −(B−Y) during blanking		–	2.0	–	V
B	−3 dB bandwidth		–	1	–	MHz
Z_O	output impedance		–	–	500	Ω
V_{dep}	supply voltage dependency		–	tbf	–	V
PAL/NTSC DEMODULATOR						
$V_{1(p-p)}$	−(R−Y) output voltage (peak-to-peak value)	standard colour bar	470	525	585	mV
$V_{2(p-p)}$	−(B−Y) output voltage (peak-to-peak value)	standard colour bar	595	665	740	mV
α	crosstalk between −(R−Y) and −(B−Y)		–	tbf	–	dB
$V_{1,2(p-p)}$	8.8 MHz residue (peak-to-peak value)	both outputs	–	–	15	mV
$V_{1,2(p-p)}$	7.2 MHz residue (peak-to-peak value)	both outputs	–	–	20	mV
PAL DEMODULATOR						
$V_{R(p-p)}$	H/2 ripple (peak-to-peak value)		–	–	50	mV
S/N	signal-to-noise ratio		46	–	–	dB
NTSC DEMODULATOR						
φ	hue phase shift		–	±45	–	deg
SECAM DEMODULATOR						
$V_{1(p-p)}$	−(R−Y) output voltage (peak-to-peak value)	standard colour bar	0.94	1.05	1.17	V
$V_{2(p-p)}$	−(B−Y) output voltage (peak-to-peak value)	standard colour bar	1.19	1.33	1.48	V
f_{os}	black level offset		–	–	7	kHz
S/N	signal-to-noise ratio		–	43	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{res(p-p)}$	7.8 to 9.4 MHz residue (peak-to-peak value)		–	–	30	mV
f_{pole}	pole frequency of deemphasis		77	85	93	kHz
	ratio of pole and zero frequency		–	3	–	
V_{cal}	calibration voltage		3	4	5	V
NL	non linearity		–	–	3	%
Filters						
TUNING						
V_{tune}	tuning voltage		1.5	3.0	6.0	V
LUMINANCE DELAY						
t_d	delay time					
	PAL/NTSC		–	480	–	ns
	SECAM		–	480	–	ns
	B/W		–	220	–	ns
CHROMINANCE TRAP						
f_O	notch frequency					
		f_{SC} = 3.6 MHz	3.53	3.58	3.63	MHz
		f_{SC} = 4.4 MHz	4.37	4.43	4.49	MHz
		SECAM	4.23	4.29	4.35	MHz
		YC mode; not active				
B	bandwidth at −3 dB					
		f_{SC} = 3.6 MHz	–	2.5	–	MHz
		f_{SC} = 4.4 MHz	–	3.1	–	MHz
		SECAM	–	3.0	–	MHz
SUPP	subcarrier suppression		26	–	–	dB
CHROMINANCE BANDPASS						
f_{res}	resonant frequency					
		f_{SC} = 3.6 MHz	–	3.58	–	MHz
		f_{SC} = 4.4 MHz	–	4.43	–	MHz
B	bandwidth at −3 dB					
		f_{SC} = 3.6 MHz	–	1.4	–	MHz
		f_{SC} = 4.4 MHz	–	1.7	–	MHz
CLOCHE FILTER						
f_{res}	resonant frequency	SECAM	4.26	4.29	4.31	MHz
B	bandwidth at −3 dB	SECAM	241	268	295	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sync input						
VIDEO INPUT						
V_{26}	sync pulse amplitude	Y/CVBS input	50	300	600	mV
	slicing level		–	50	–	%
t_d	delay of sync pulse due to internal filter		0.2	0.3	0.4	µs
S/N	noise detector threshold level		–	20	–	dB
H	hysteresis		–	3	–	dB
t_d	delay between video signal and internally separated vertical sync pulse		12	18.5	27	µs
Horizontal section						
CLP OUTPUT (OPB/CLP MODE); H_A OUTPUT (LLC/HA MODE)						
V_{OH}	HIGH level output voltage		4.0	5.0	5.5	V
V_{OL}	LOW level output voltage	I_{sink} = 2 mA	–	0.2	0.4	V
I_{sink}	sink current		2	–	–	mA
I_{source}	source current		2	–	–	mA
t_W	H_A pulse width (32 LLC pulses)		–	4.7	–	µs
t_d	delay between middle of horizontal sync pulse and middle of H_A	note 2	0.3	0.45	0.6	µs
t_d	delay between negative edge LLC pulse and positive edge H_A pulse	C_L = 15 pF	10	20	40	ns
t_W	CLP pulse width	21 LLC pulses	–	3.1	–	µs
t_d	delay between middle of horizontal sync pulse and start of CLP pulse	note 2	3.5	3.7	3.9	µs
FIRST LOOP						
Δf	frequency deviation when not locked		–	–	1.5	%
SVRR	supply voltage ripple rejection		–	tbf	–	V
TC	temperature coefficient		–	tbf	–	Hz/°C
f_{CR}	catching range		±625	–	–	Hz
f_{HR}	holding range		–	–	±1.4	kHz
ϕ	static phase shift		–	–	0.1	µs/kHz
LLC OUTPUT (LLC/H_A MODE)						
f_O	output frequency					
	$432f_H$	50 Hz standard	–	6.75	–	MHz
	$432f_H$	60 Hz standard	–	6.80	–	MHz
$V_{O(p-p)}$	output amplitude (peak-to-peak value)	C_L = 15 pF	0.25	–	–	V
V_O	DC output voltage level		–	2.5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical section						
VERTICAL OSCILLATOR						
f_{fr}	free running frequency					
		FORF = 1; divider ratio 628	–	50	–	Hz
		FORF = 0; divider ratio 528	–	60	–	Hz
f_{LR}	frequency locking range		43	–	64	Hz
LR	divider locking range		488	625	722	
V_A output						
V_{OH}	HIGH level output voltage		4.0	5.0	5.5	V
V_{OL}	LOW level output voltage		–	0.2	0.4	V
I_{sink}	sink current		2	–	–	mA
I_{source}	source current		2	–	–	mA
t_W	V_A pulse width					
		50 Hz standard	–	160	–	µs
		60 Hz standard	–	192	–	µs
t_d	delay between start of vertical sync pulse and positive edge of V_A pulse		–	32	–	µs
Z_O	output impedance	STM = 1	3	–	–	MΩ
Sandcastle output (pin 10)						
V_{10}	zero level output voltage		0	0.5	1.0	V
I_{sink}	sink current		0.5	–	–	mA
HORIZONTAL AND VERTICAL BLANKING						
V_{bl}	blanking voltage level		2.0	2.5	3.0	V
I_{source}	source current		0.5	–	–	mA
I_{ext}	external current required to force the output to the blanking level		1.0	–	3.0	mA
t_W	horizontal blanking pulse width	69 LLC pulses	–	10.2	–	µs
t_d	delay between start of horizontal blanking and start of clamping pulse	45 LLC pulses	–	6.7	–	µs
CLAMPING PULSE						
V_{clamp}	clamping voltage level		4.0	4.5	5.0	V
I_{source}	source current		0.5	–	–	mA
t_W	pulse width	21 LLC pulses	–	3.1	–	µs
t_d	delay between middle sync of input and start of clamping pulse	note 2	3.5	3.7	3.9	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Colour matrix						
G_v	gain					
	from R to Y		–	0.43	–	
	from G to Y		–	0.84	–	
	from B to Y		–	0.16	–	
	from R to U_{out}		–	0.43	–	
	from G to U_{out}		–	0.84	–	
	from B to U_{out}		–	1.27	–	
	from R to V_{out}		–	1.00	–	
	from G to V_{out}		–	0.84	–	
	from B to V_{out}		–	0.16	–	
Output and input/output port						
O PORT (OPB/CLP MODE)						
V_{OH}	HIGH level output voltage		4.0	5.0	5.5	V
V_{OL}	LOW level output voltage		–	0.2	0.4	V
I_{sink}	sink current		100	–	–	μA
I_{source}	source current		100	–	–	μA
I/O PORT (OPB/CLP MODE)						
V_{OH}	HIGH level output voltage		–	–	V_{SUP}	V
V_{OL}	LOW level output voltage		–	0.2	0.4	V
I_{sink}	sink current		2	–	–	mA
V_{IH}	HIGH level input voltage		2.0	–	–	V
V_{IL}	LOW level input voltage		–	–	0.6	V
YUV switches (note 3)						
RGB INPUTS (NOTE 3)						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	note 4	–	0.7	1.0	V
Z_I	input impedance		3	–	–	MΩ
UV INPUTS (NOTE 3)						
$V_{I(p-p)}$	U input voltage (peak-to-peak value)	note 3	–	1.33	1.90	V
$V_{I(p-p)}$	V input voltage (peak-to-peak value)		–	1.05	1.50	V
Z_I	input impedance (both inputs)		3	–	–	MΩ
Y OUTPUT						
$V_{O(p-p)}$	U output voltage (peak-to-peak value)	note 4; top sync-to-white	–	1.43	–	V
Z_O	output impedance		–	–	250	Ω
V_O	DC output voltage level	top sync	–	2.5	–	V
S/N	signal-to-noise ratio		–	tbf	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
YUV switches (note 3)						
RGB INPUTS (NOTE 3)						
$V_{I(p\text{-}p)}$	input voltage (peak-to-peak value)	note 4	–	0.7	1.0	V
Z_I	input impedance		3	–	–	MΩ
UV INPUTS (NOTE 3)						
$V_{I(p\text{-}p)}$	U input voltage (peak-to-peak value)	note 3	–	1.33	1.90	V
$V_{I(p\text{-}p)}$	V input voltage (peak-to-peak value)		–	1.05	1.50	V
Z_I	input impedance (both inputs)		3	–	–	MΩ
Y OUTPUT						
$V_{O(p\text{-}p)}$	U output voltage (peak-to-peak value)	note 4; top sync-to-white	–	1.43	–	V
Z_O	output impedance		–	–	250	Ω
V_O	DC output voltage level	top sync	–	2.5	–	V
S/N	signal-to-noise ratio		–	tbf	–	dB
UV OUTPUTS (NOTE 3)						
$V_{O(p\text{-}p)}$	U output voltage (peak-to-peak value)		–	1.33	1.90	V
$V_{O(p\text{-}p)}$	V output voltage (peak-to-peak value)		–	1.05	1.50	V
Z_O	output impedance (both outputs)		–	–	250	Ω
V_O	DC output voltage level		–	2.7	–	V
GENERAL						
V_{diff}	difference between black levels of YUV outputs in RGB mode and YUV mode	sync locked	–	–	10	mV
NL	non-linearity	any input to any output	–	–	5	%
B	bandwidth	any input to any output	–	7	–	MHz
CT	crosstalk between RGB and UV_{in} signals on UV_{out}	f = 0 to 5 MHz	–	–	–50	dB
FAST SWITCH SELECT INPUT (PIN 18)						
V_{IH}	HIGH level input voltage	RGB switched on	0.9	–	3.0	V
V_{IL}	LOW level input voltage	UV switched on	0	–	0.5	V
G_v	gain					
	from U_{in} to U_{out}		–	1	–	
	from V_{in} to V_{out}		–	1	–	
t_d	switching delay	between pin 18 and YUV	–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INPUT CLAMP (PIN 17)						
V_{IH}	HIGH level input voltage	clamping	2.4	–	5.5	V
V_{IL}	LOW level input voltage	no clamping	0	–	0.6	V
t_W	clamping pulse width		1.8	3.5	–	µs
V_{os}	clamping offset voltage on UV outputs		–	–	10	mV
Z_I	input impedance	STM = 1	3	–	–	MΩ

Notes to the characteristics

1. All oscillator specifications are measured with the Philips crystal series 4322 143/144. If the spurious response of the reference crystal is less than –3 dB with respect to the fundamental frequency for a damping resistance of 1 kΩ, oscillation at the fundamental frequenct is guaranteed. The spurious response of the second crystal must be less than –3 dB with respect to the fundamental frequency for a damping resistance of 1.5 kΩ.

   The catching and detuning range are measured for nominal crystal parameters. These are:

   load resonance frequency f_0 (C_L = 20 pF) = 4.433619 MHz, (second crystal: 3.579545 MHz)

   motional capacitance C_M = 20.6 fF, (second crystal: 14.7 fF)

   parallel capacitance C_0 = 5.5 pF, (second crystal: 4.5 pF).

   The actual load capacitance in the application should be C_L = 18 pF to account for parasitic capacitances on and off chip.
2. This delay is caused by the low pass filter at the sync separator input.
3. The output signals of the demodulator are called –(R–Y) and –(B–Y). The colour difference input and output signals of the YUV switch are called UV signals. However, these signals do not have the amplitude correction factor of real UV signals. They are called UV signals and not –(R–Y) and –(B–Y) to prevent confusion between the colour difference signals of the demodulator and the colour difference signals of the YUV switch.
4. This value refers to signals including a sync pulse. For Y signals composed ot the RGB inputs this output voltage is 30% lower, as there is no sync pulse on such signals.

QUALITY SPECIFICATION

Quality level in accordance with URV 4-2-59/601.

TEST AND APPLICATION INFORMATION

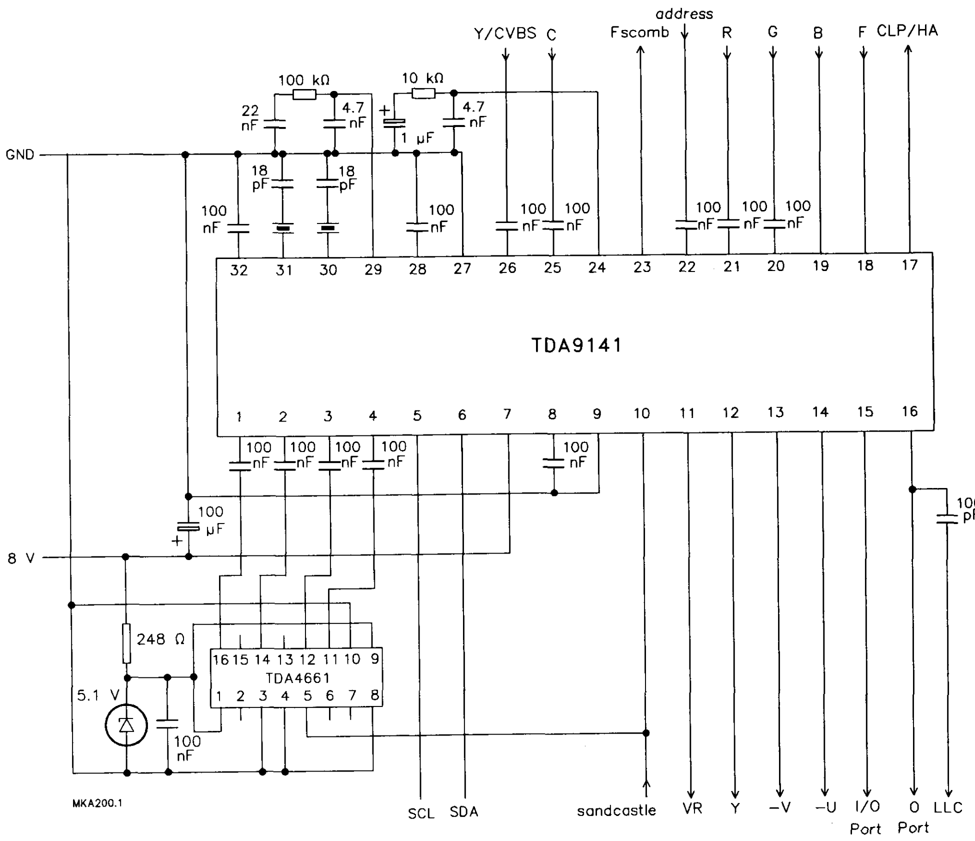


Fig.8 Application diagram.

Notes to figure 8

1. Pins 28 and 32 are sensitive to leakage current.
2. The analog and digital ground currents should be completely separated.
3. The decoupling capacitor connected between pins 8 and 9 must be placed as close to the IC as possible.

8-bit high-speed analog-to-digital converter

TDF8704

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- Extended temperature range (−40 to +85 °C)
- High signal-to-noise ratio over a large analog input frequency range (7.4 effective bits at 4.43 MHz full-scale input at f_{CLK} = 50 MHz)
- Binary 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Stable internal reference voltage regulator included
- Power dissipation only 360 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

- General purpose high-speed analog-to-digital conversion for extended temperature applications
- Automotive
- RF, satellite and GPS
- Medical
- General industrial
- Digital video (VCR, TV and satellite).

GENERAL DESCRIPTION

The TDF8704T is an 8-bit high-speed analog-to-digital converter (ADC) for general industrial applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are TTL compatible, although a low-level AC clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	37	tbf	mA
I_{CCD}	digital supply current		–	18	tbf	mA
I_{CCO}	output stages supply current		–	17	tbf	mA
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
AILE	AC integral linearity error	note 1	–	–	±2	LSB
f_{CLK}	maximum conversion rate		50	–	–	MHz
P_{tot}	total power dissipation		–	360	tbf	mW

Note

1. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK} = 50 MHz).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				
	PINS	PIN POSITION	MATERIAL	CODE	SAMPLING FREQUENCY (MHz)
TDF8704T/2	24	SO24	plastic	SOT137A	20
TDF8704T/4	24	SO24	plastic	SOT137A	40
TDF8704T/5	24	SO24	plastic	SOT137A	50

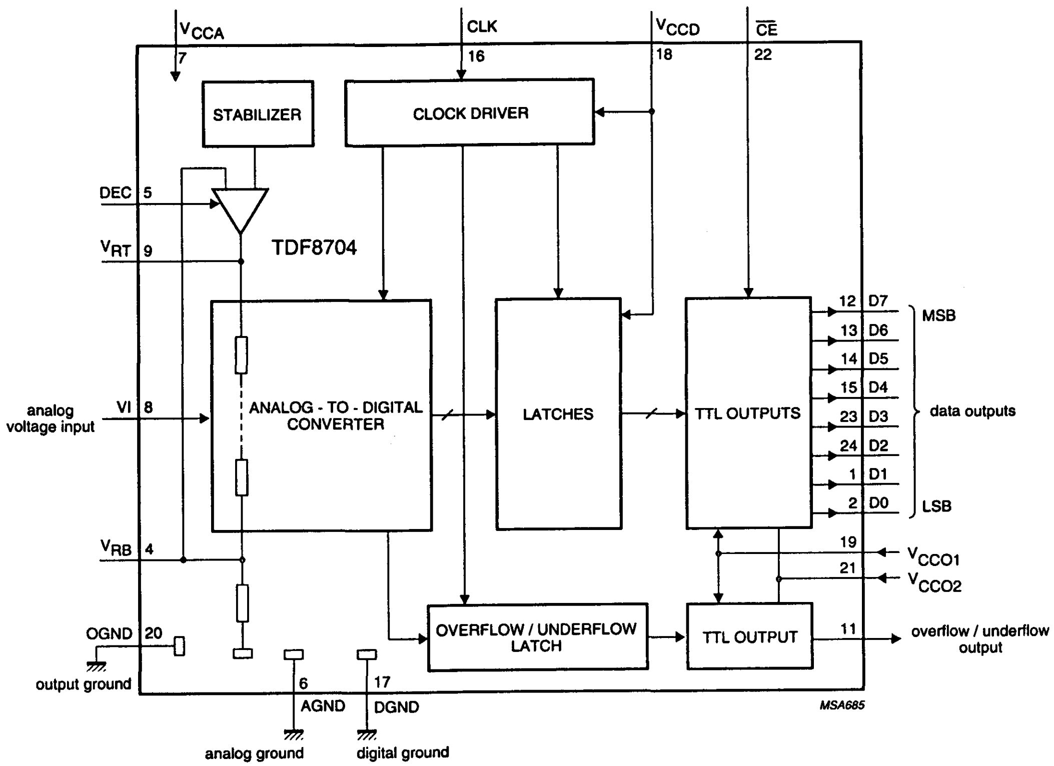


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output; bit 0 (LSB)
n.c.	3	not connected
V_{RB}	4	reference voltage bottom (decoupling)
DEC	5	decoupling input (internal stabilization loop decoupling)
AGND	6	analog ground
V_{CCA}	7	positive supply voltage for analog circuits (+5 V)
VI	8	analog voltage input
V_{RT}	9	reference voltage top (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output; bit 7 (MSB)
D6	13	data output; bit 6
D5	14	data output; bit 5
D4	15	data output; bit 4
CLK	16	clock input
DGND	17	digital ground
V_{CCD}	18	positive supply voltage for digital circuits (+5 V)
V_{CCO1}	19	positive supply voltage for output stages 1 (+5 V)
OGND	20	output ground
V_{CCO2}	21	positive supply voltage for output stages 2 (+5 V)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output; bit 3
D2	24	data output; bit 2

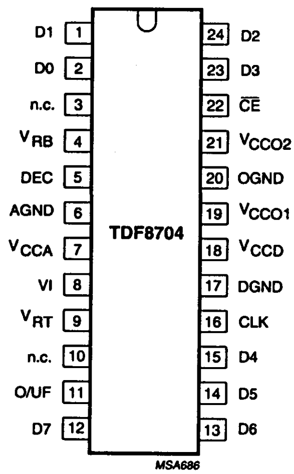


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		−0.3	7.0	V
V_{CCD}	digital supply voltage		−0.3	7.0	V
V_{CCO}	output stages supply voltage		−0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage differences		−1.0	1.0	V
V_{VI}	input voltage range	referenced to AGND	−0.3	7.0	V
$V_{CLK(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	−	V_{CCD}	V
I_O	output current		−	+10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
T_j	junction temperature		−	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	75 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7 - V_6$ = 4.75 V to 5.25 V; $V_{CCD} = V_{18} - V_{20}$ = 4.75 V to 5.25 V; $V_{CCO} = V_{19} - V_{20}$ = 4.75 V to 5.25 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD}$ = −0.25 V to +0.25 V; $V_{CCO} - V_{CCD}$ = −0.25 V to +0.25 V; $V_{CCA} - V_{CCD}$ = −0.25 V to +0.25 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO1} = V_{CCO2}$ = 5 V and T_{amb} = 25 °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	37	tbf	mA
I_{CCD}	digital supply current		–	18	tbf	mA
I_{CCO}	output stage supply current	all outputs LOW	–	17	tbf	mA
Inputs						
Clock input; CLK (referenced to DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	−400	–	–	µA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	µA
		$V_{CLK} = V_{CCD}$	–	–	300	µA
Z_i	input impedance	f_{CLK} = 50 MHz	–	2	–	kΩ
C_i	input capacitance	f_{CLK} = 50 MHz	–	4.5	–	pF
Input $\overline{CE}$ (referenced to DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.2	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{IL} = 0.4 V	−400	–	–	µA
I_{IH}	HIGH level input current	V_{IH} = 2.7 V	–	–	20	µA
VI (analog input voltage referenced to AGND) (see Figs 3 and 4)						
$V_{VI(B)}$	input voltage (bottom)		tbf	1.23	tbf	V
$V_{VI(0)}$	input voltage	output code = 0	tbf	1.46	tbf	V
$V_{OS(B)}$	offset voltage (bottom)	$V_{VI(0)} - V_{VI(B)}$	tbf	–	tbf	V
$V_{VI(T)}$	input voltage (top)		tbf	3.41	tbf	V
$V_{VI(255)}$	input voltage	output code = 255	tbf	3.31	tbf	V
$V_{OS(T)}$	offset voltage (top)	$V_{VI(T)} - V_{VI(255)}$	tbf	–	tbf	V
$V_{VI(p-p)}$	input voltage amplitude (peak-to-peak value)		tbf	1.85	tbf	V
I_{IL}	LOW level input current	V_{VI} = 1.23 V	–	0	–	µA
I_{IH}	HIGH level input current	V_{VI} = 3.41 V	60	150	300	µA
Z_i	input impedance	f_i = 4.43 MHz	–	10	–	kΩ
C_i	input capacitance	f_i = 4.43 MHz	–	14	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference resistance						
R_{ref}	reference resistance	V_{RT} to V_{RB}	–	220	–	Ω
Outputs						
Digital outputs (D7 - D0) (referenced to DGND)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = −0.4 mA	2.7	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	–	+20	μA
Switching characteristics (note 1; see Fig.3)						
f_{CLK}	maximum clock frequency	TDF8704T/2	20	–	–	MHz
		TDF8704T/4	40	–	–	MHz
		TDF8704T/5	50	–	–	MHz
t_{CPH}	clock pulse width HIGH		7	–	–	ns
t_{CPL}	clock pulse width LOW		7	–	–	ns
Analog signal processing (f_{CLK} = 50 MHz)						
G_d	differential gain	note 2	–	0.6	–	%
ϕ_d	differential phase	note 2	–	0.8	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz	–	−60	–	dB
SVRR1	supply voltage ripple rejection	note 3	–	−28	−25	dB
SVRR2	supply voltage ripple rejection	note 3	–	1	2.5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
AILE	AC integral linearity error	note 4	–	–	±2	LSB
Effective bits; note 5						
EB	TDF8704T/2 (f_{CLK} = 20 MHz)	f_i = 2.5 MHz	–	7.7	–	bits
		f_i = 4.43 MHz	–	7.6	–	bits
	TDF8704T/4 (f_{CLK} = 40 MHz)	f_i = 4.43 MHz	–	7.5	–	bits
		f_i = 7.5 MHz	–	7.3	–	bits
	TDF8704T/5 (f_{CLK} = 50 MHz)	f_i = 4.43 MHz	–	7.4	–	bits
		f_i = 7.5 MHz	–	7.2	–	bits

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (note 6; see Figs 3 to 5; f_{CLK} = 50 MHz)						
t_{ds}	sampling delay		–	–	2	ns
t_{HD}	output hold time		5	–	–	ns
t_d	output delay time		–	12	15	ns
t_{dZH}	3-state output delay times	enable-to-HIGH	–	19	tbf	ns
t_{dZL}	3-state output delay times	enable-to-LOW	–	16	tbf	ns
t_{dHZ}	3-state output delay times	disable-to-HIGH	–	14	tbf	ns
t_{dLZ}	3-state output delay times	disable-to-LOW	–	9	tbf	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
3. Supply voltage ripple rejection:
   - SVRR1; variation of the input voltage producing output code 127 for supply voltage variation of 1 V: SVRR1 = 20 log ($\Delta V_{VI(127)}$ / ΔV_{CCA})
   - SVRR2; relative variation of the full-scale range of analog input for a supply voltage variation of 1 V: SVR2 = $\{\Delta(V_{VI(0)} - V_{VI(255)}) / (V_{VI(0)} - V_{VI(255)})\} \div \Delta V_{CCA}$.
4. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK} = 50 MHz).
5. Effective bits are obtained via a Fast Fourier Transformer (FFT) treatment taking 4K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to SNR: SNR (dB) = EB x 6.02 + 1.76.
6. Output data acquisition:
   - Output data is available after the maximum delay of t_d.

Table 1 Output coding and input voltage (typical values; referenced to AGND).

			BINARY OUTPUT BITS							
STEP	$V_{VI(p-p)}$	O/UF	D7	D6	D5	D4	D3	D2	D1	D0
underflow	< 1.46	1	0	0	0	0	0	0	0	0
0	1.46	0	0	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
254	•	0	1	1	1	1	1	1	1	0
255	3.31	0	1	1	1	1	1	1	1	1
overflow	> 3.316	1	1	1	1	1	1	1	1	1

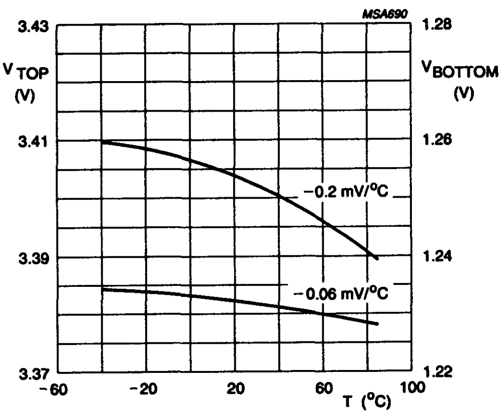


Fig.3 Influence of ambient temperature on V_{TOP} and V_{BOTTOM} under 5 V supply.

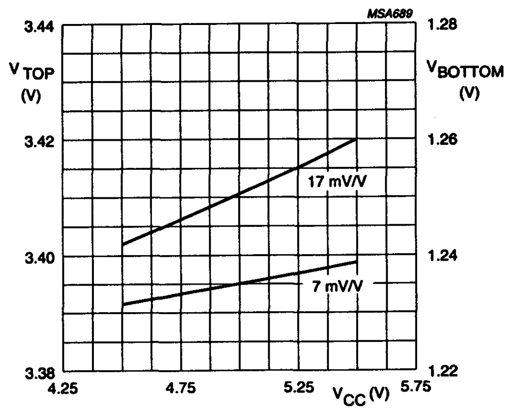


Fig.4 Influence of supply voltage on V_{TOP} and V_{BOTTOM} under 25 °C ambient temperature.

Table 2 Mode selection.

$\overline{CE}$	D7 to D0	O/UF
1	high impedance	high impedance
0	active; binary	active

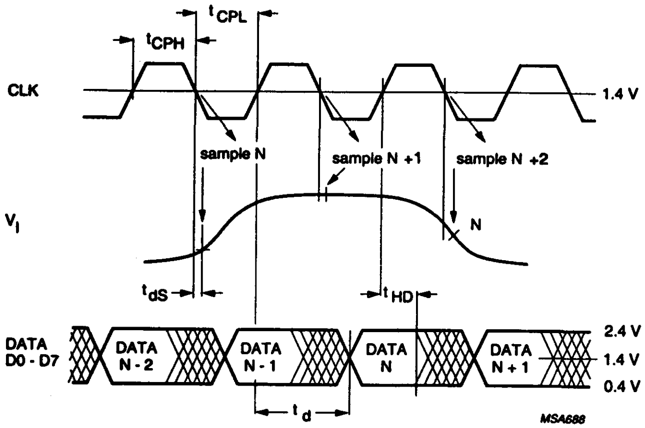


Fig.5 Timing diagram.

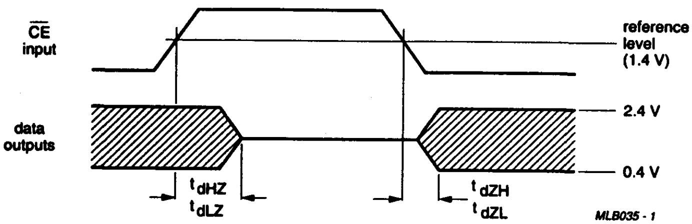


Fig.6 3-state delay timing diagram.

INTERNAL PIN CONFIGURATIONS

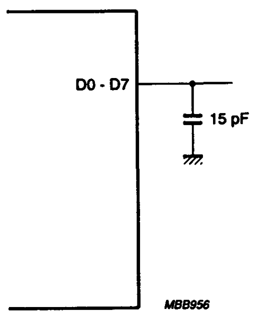


Fig.7 Load circuit for timing measurement.

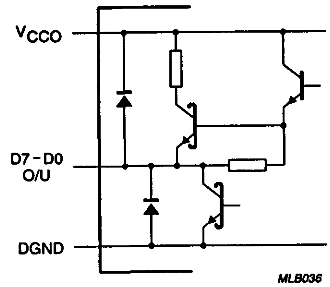


Fig.8 TTL data and overflow/underflow outputs.

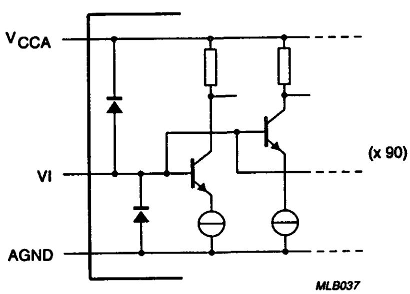


Fig.9 Analog inputs.

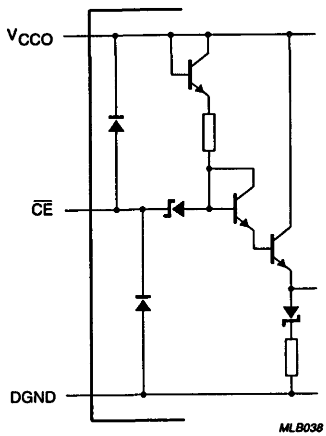


Fig.10 $\overline{CE}$ (3-state) input.

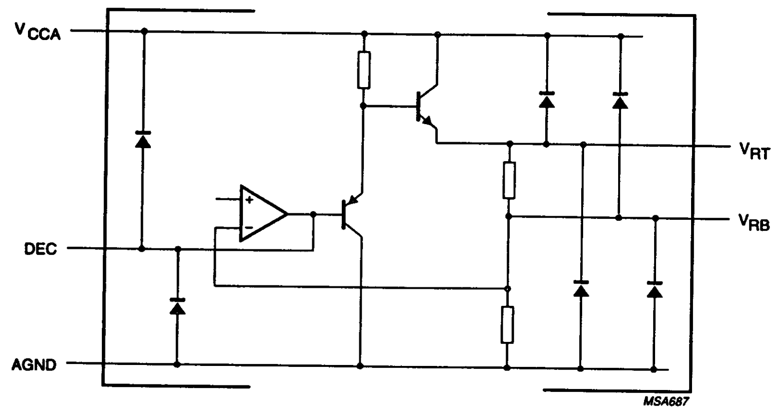


Fig.11 V_{RB}, V_{RT} and DEC.

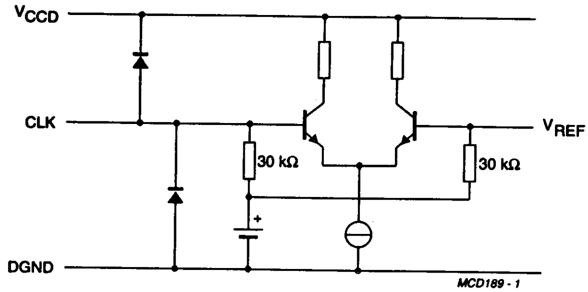


Fig.12 CLK input.

APPLICATION INFORMATION

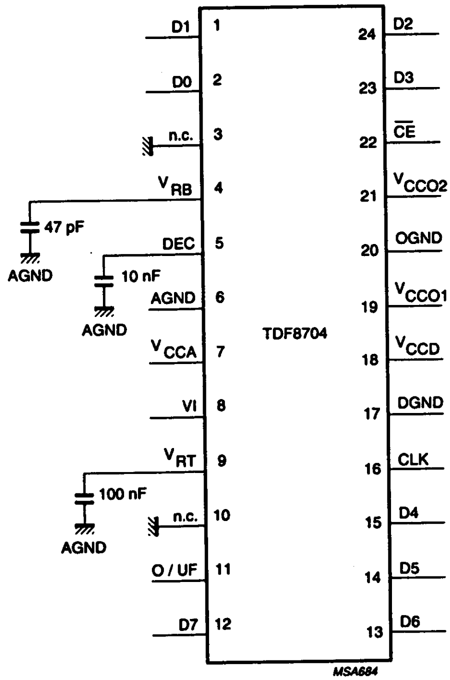


Fig.13 Application diagram.

Notes to Fig.13

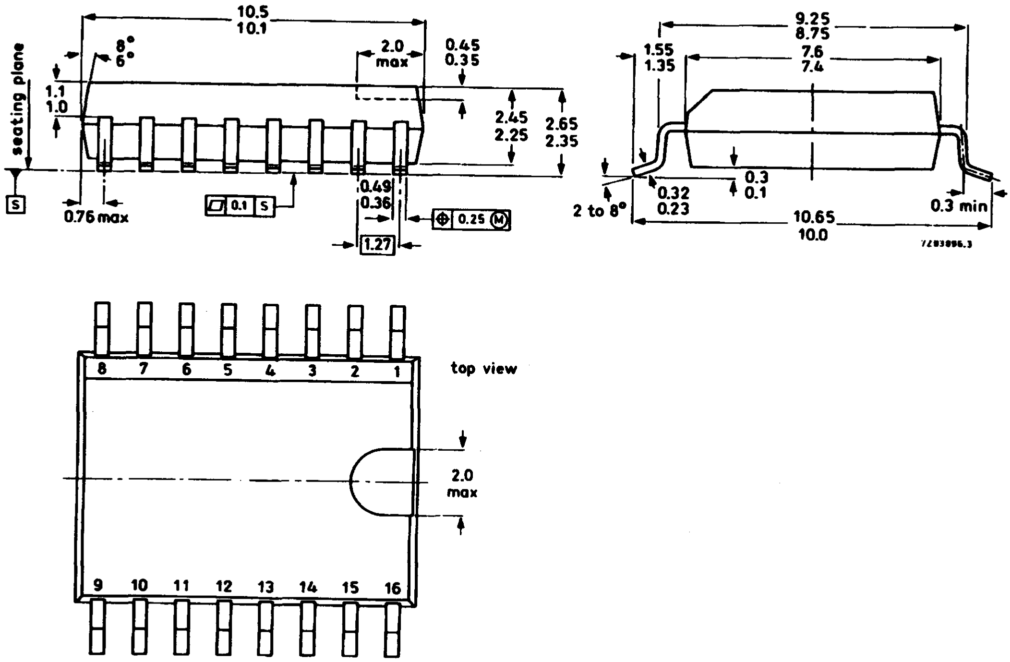
1. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder; do not draw current from these pins in order to achieve good linearity.
2. Analog and digital supplies should be separated and decoupled.
3. Pins 3 and 10 should be connected to DGND in order to prevent noise influence.

Section 4
Package Outline Drawings

CONTENTS

Package Outline Drawings

SOT162A 16-PIN PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D/T) PACKAGE



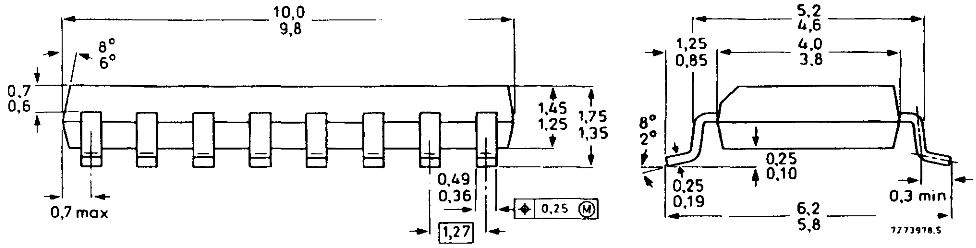
(1) Dimensions in mm.

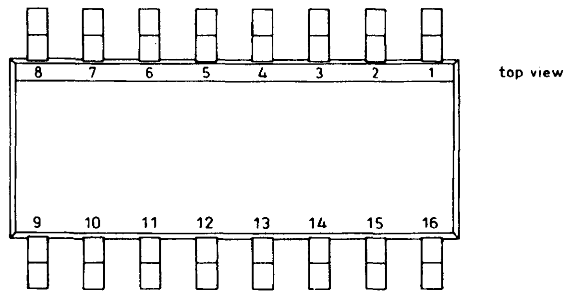
SOT 162A

7Z83896.3

Package Outline Drawings

SOT109A 16-PIN PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D/T) PACKAGE





Dimensions in mm

⊕ Positional accuracy.

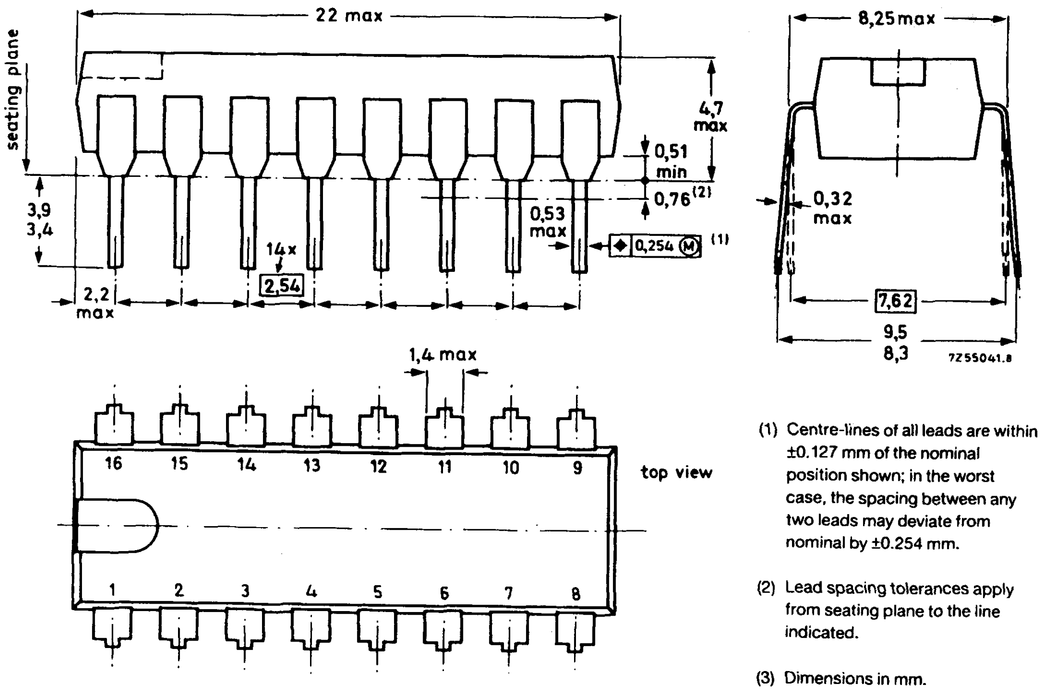
Ⓜ Maximum Material Condition.

SOT 109A

7Z73978 5

Package Outline Drawings

SOT38 16-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE



(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

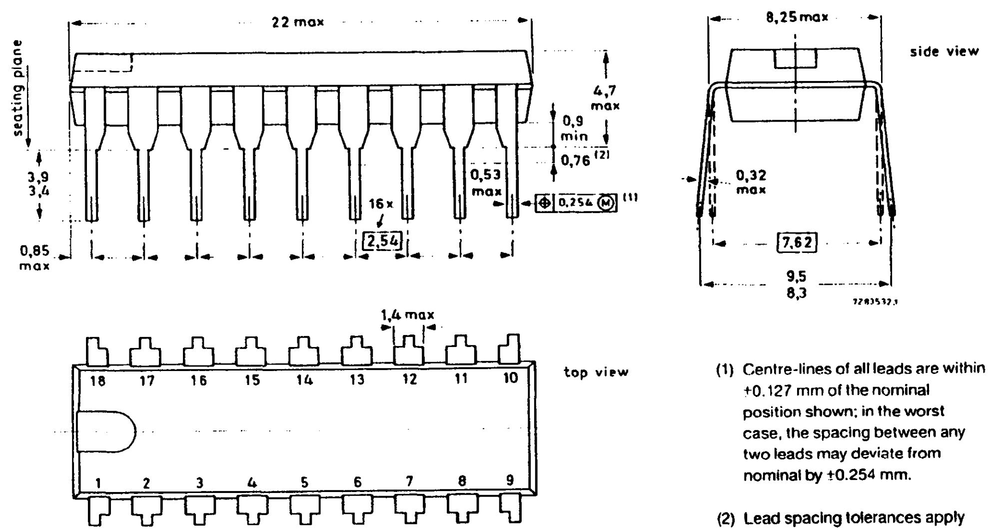
(3) Dimensions in mm.

SOT 38

7Z55041.8

Package Outline Drawings

SOT102 18-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE WITH INTERNAL HEATSPREADER



(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

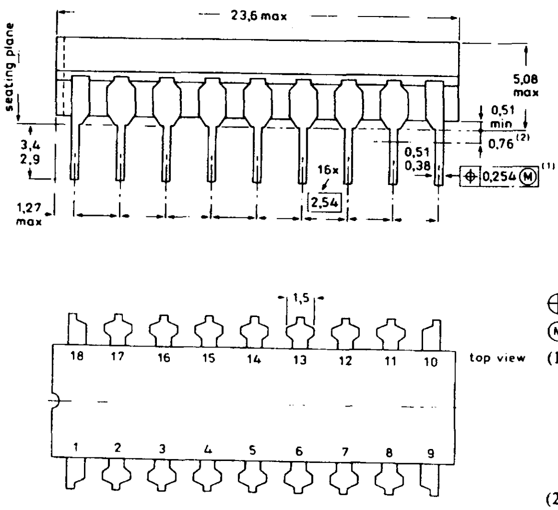
(3) Dimensions in mm.

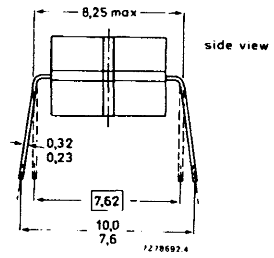
SOT 102

7Z83532.1

Package Outline Drawings

SOT133BH3 18-PIN CERAMIC DUAL IN-LINE (F) PACKAGE





Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

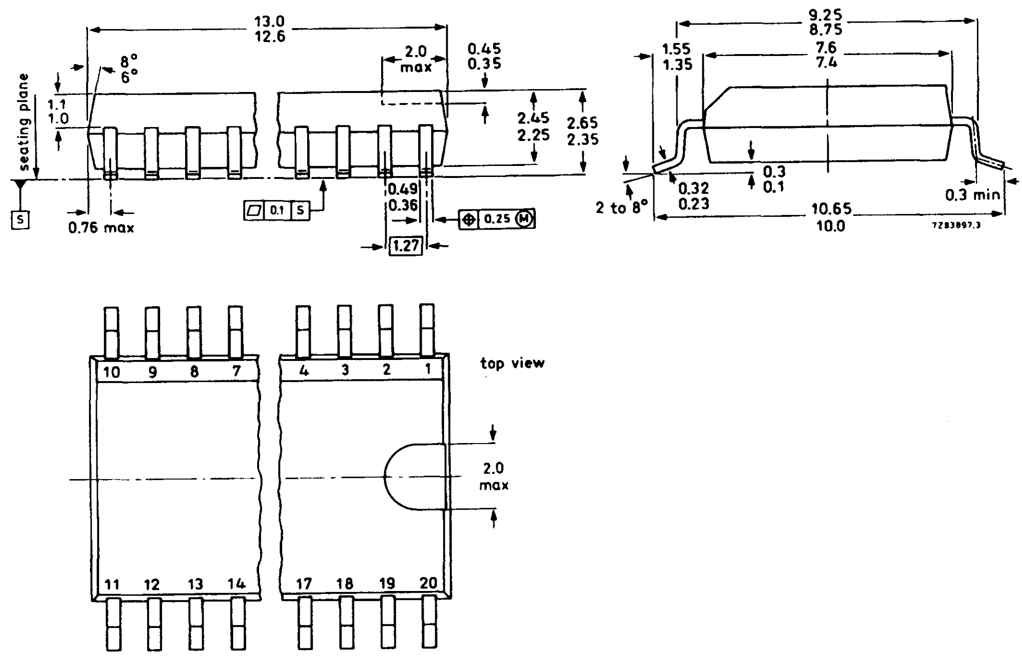
Fig.9 18-lead dual in-line; ceramic (cerdip) (SOT133BH3).

SOT133BH3

7Z78692.4

Package Outline Drawings

SOT163A 20-PIN PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D/T) PACKAGE



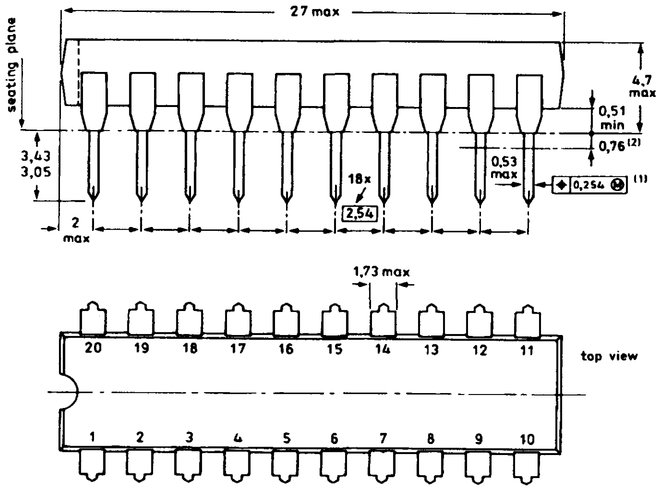
(1) Dimensions in mm.

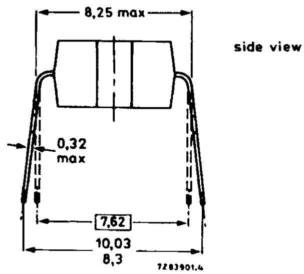
SOT 163A

7Z83897.3

Package Outline Drawings

SOT146 20-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE





(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

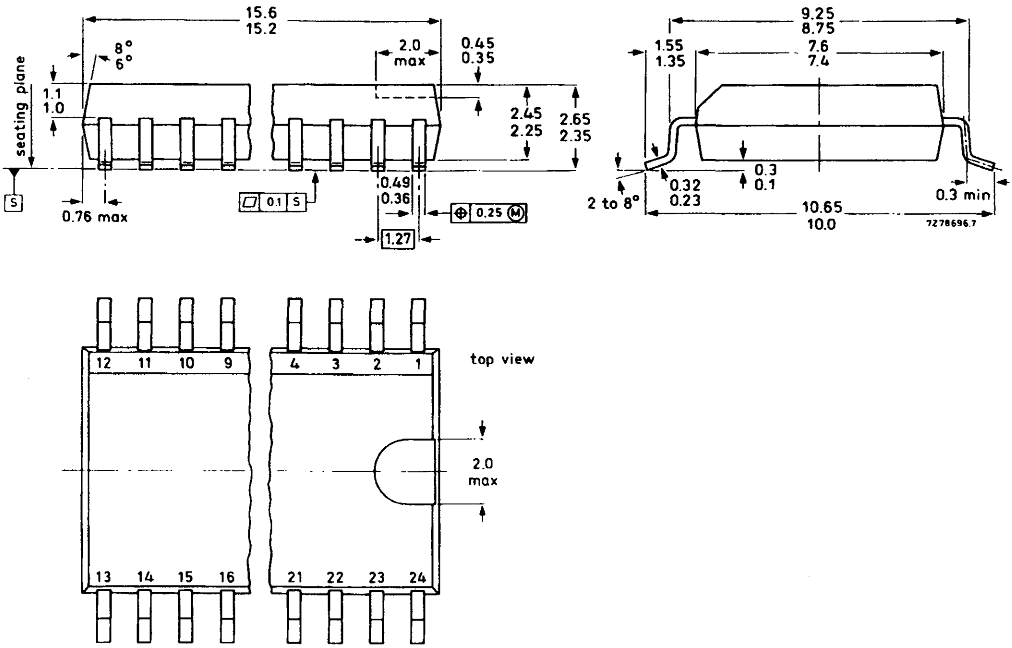
(3) Dimensions in mm.

SOT 146

7Z83901.4

Package Outline Drawings

SOT137A 24-PIN PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D/T) PACKAGE



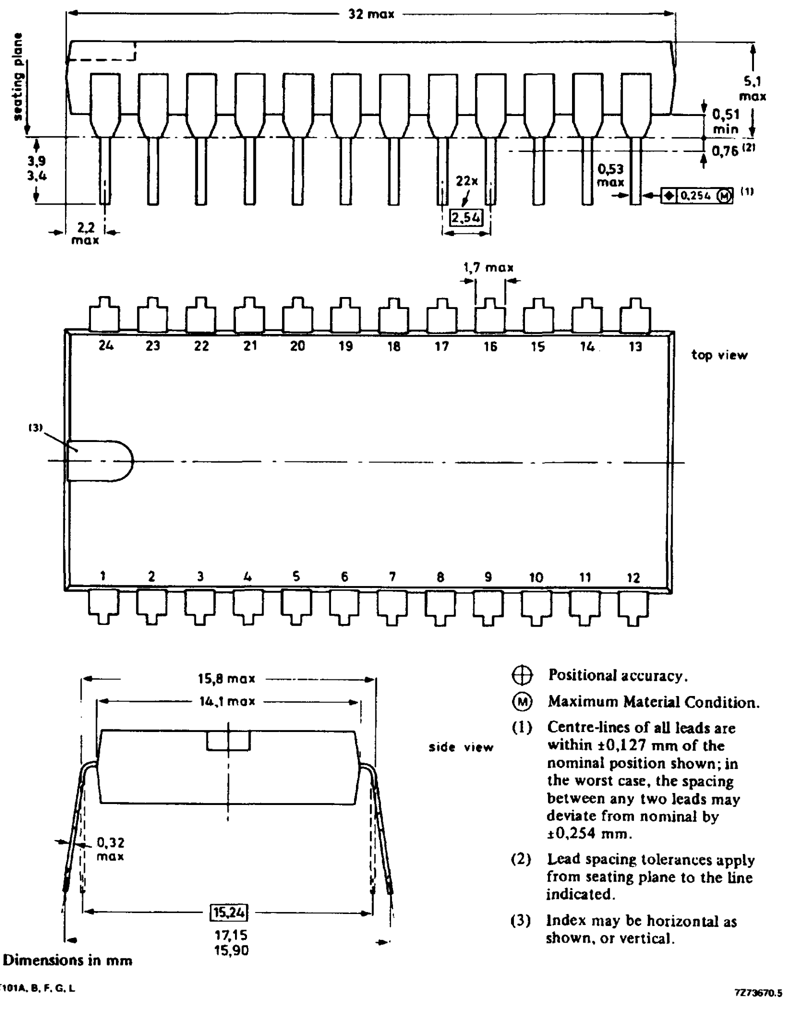
(1) Dimensions in mm.

SOT 137A

7Z78696.7

Package Outline Drawings

SOT101 24-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE WITH INTERNAL HEATSPREADER



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

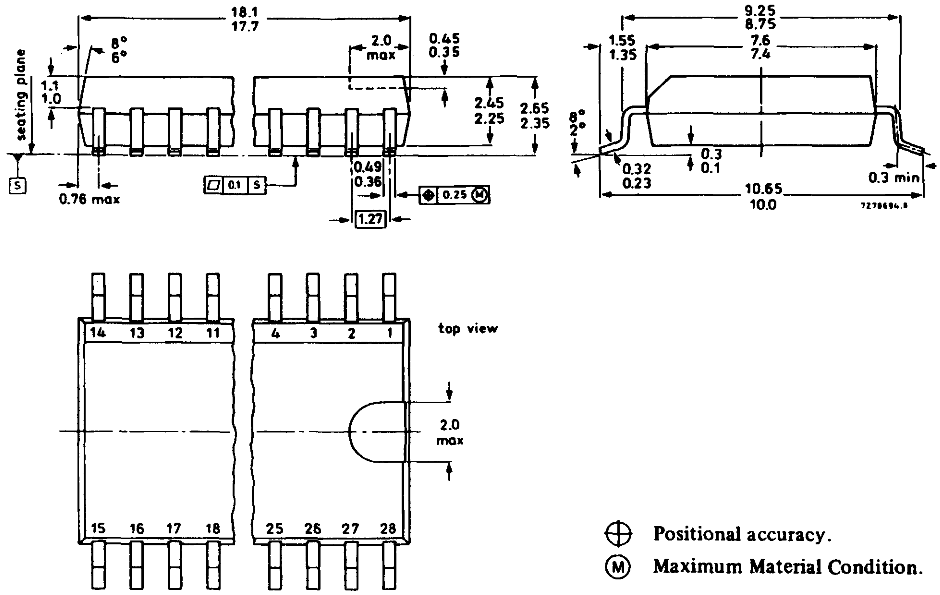
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Package Outline Drawings

SOT136A 28-PIN PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D/T) PACKAGE



⊕ Positional accuracy.

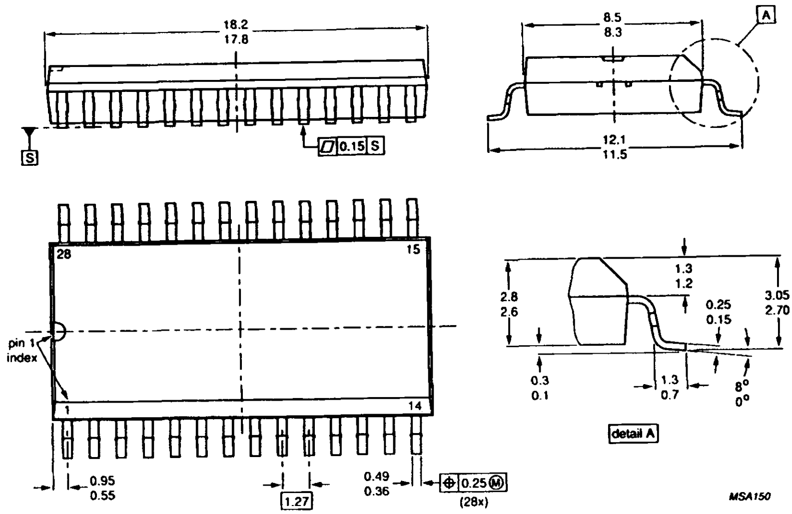
Ⓜ Maximum Material Condition.

Dimensions in mm

SOT136A

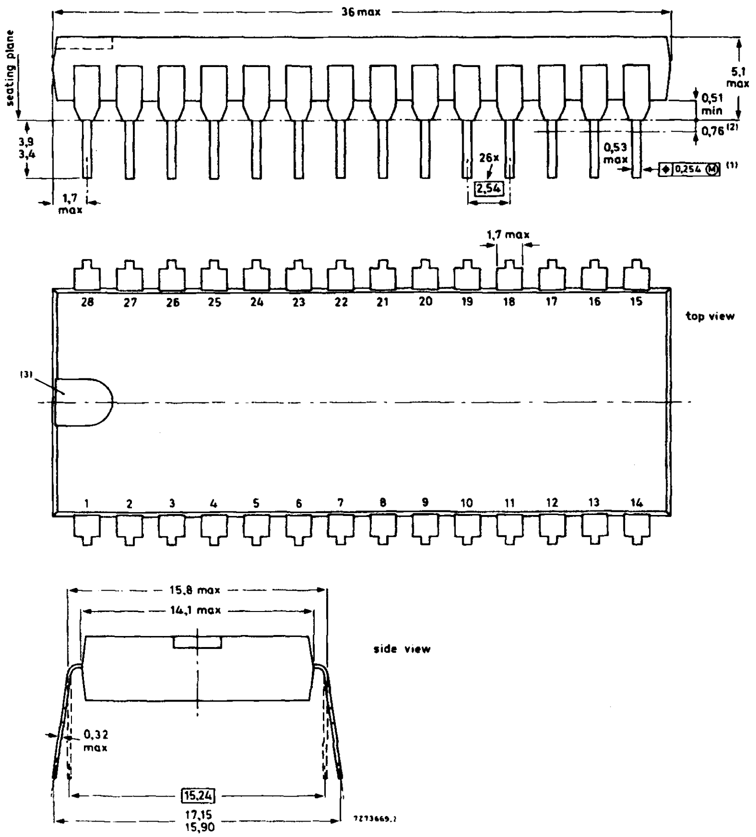
Package Outline Drawings

SOT213 28-PIN SOL (SMALL OUTLINE LARGE) PLASTIC DUAL IN-LINE (D/T) PACKAGE



Package Outline Drawings

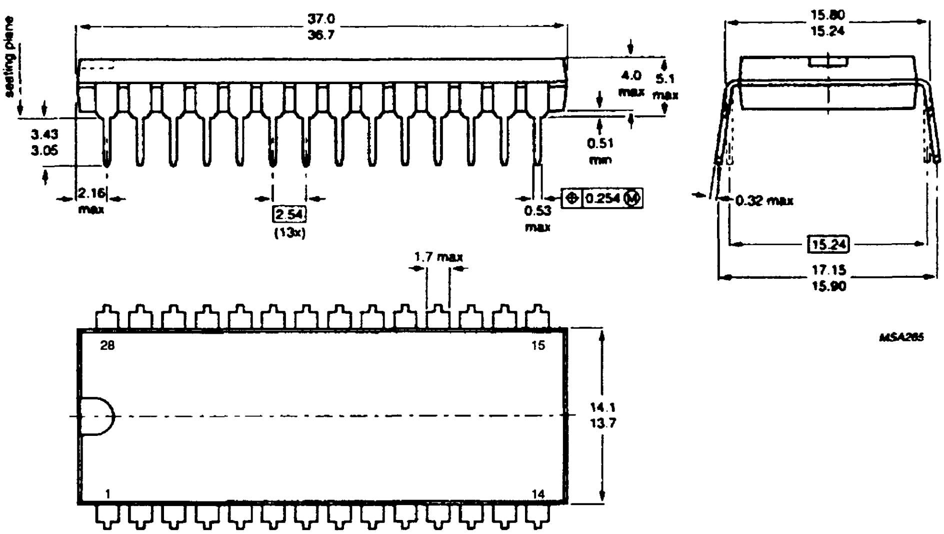
SOT117 28-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE



SOT117

Package Outline Drawings

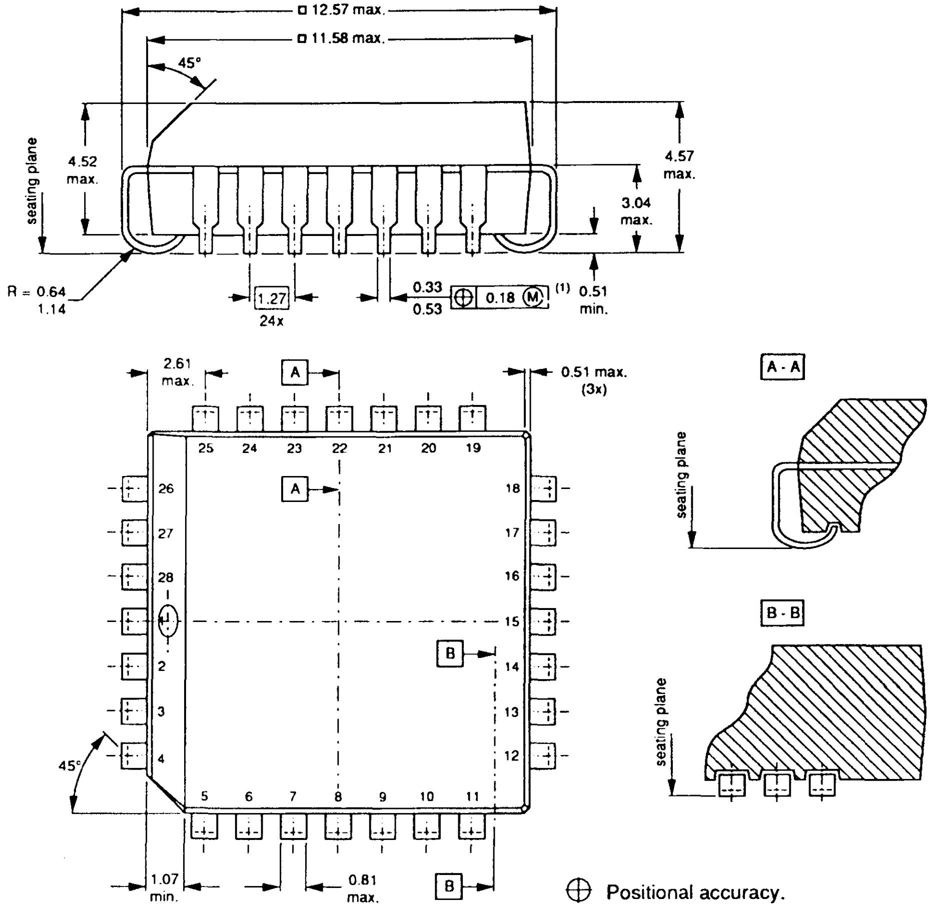
SOT107 28-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE WITH INTERNAL HEATSPEAKER



Dimensions in mm.

Package Outline Drawings

SOT261 28-PIN PLASTIC LEADED CHIP CARRIER (A) PACKAGE



⊕ Positional accuracy.

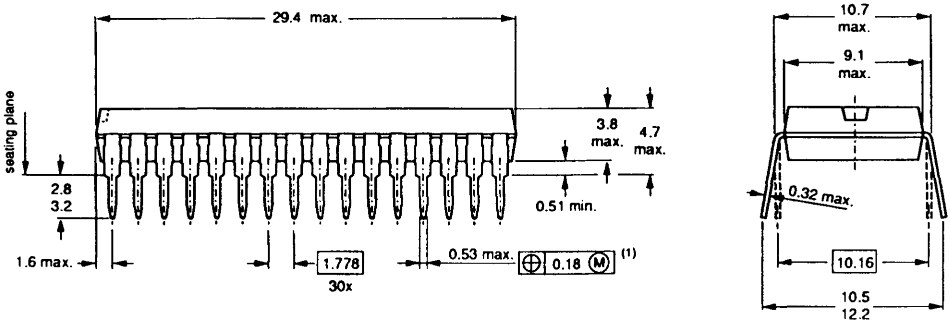
Ⓜ Maximum Material Condition.

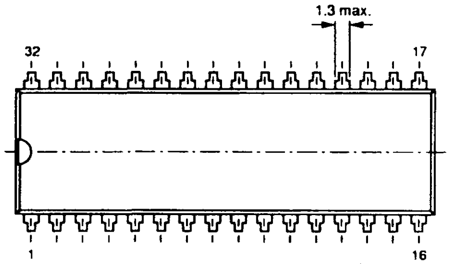
(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.18 mm.

Dimensions in mm

Package Outline Drawings

SOT232 32-PIN PLASTIC SHRINK DUAL IN-LINE (N/P) PACKAGE





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

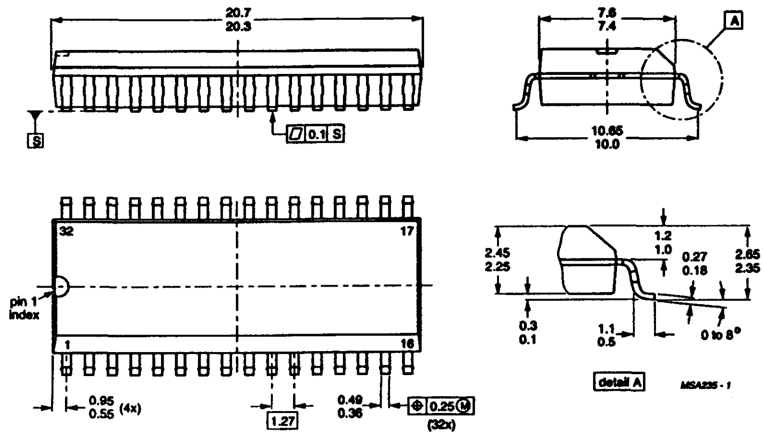
(1) Centre-lines of all leads are within ±0.09 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.18 mm.

Dimensions in mm

OT232

Package Outline Drawings

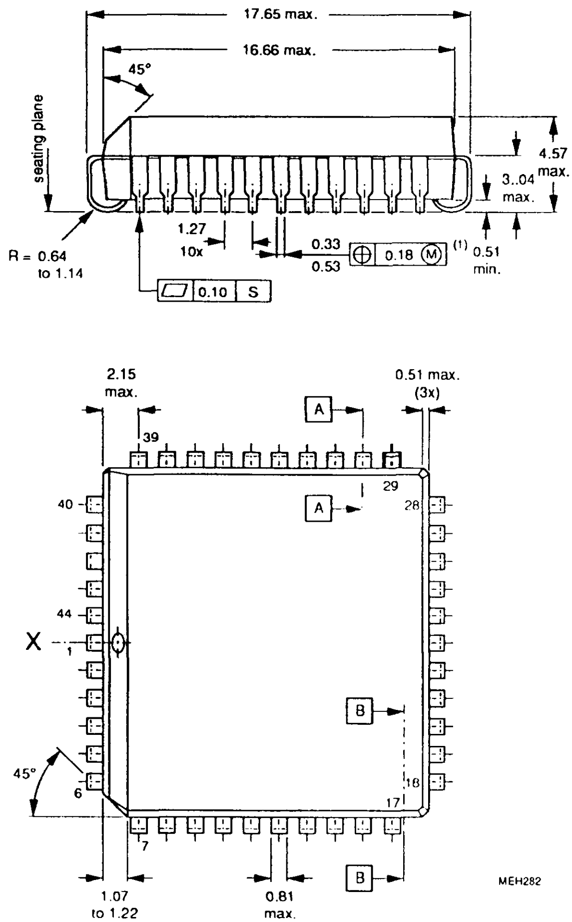
SOT287 32-PIN PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D/T) PACKAGE

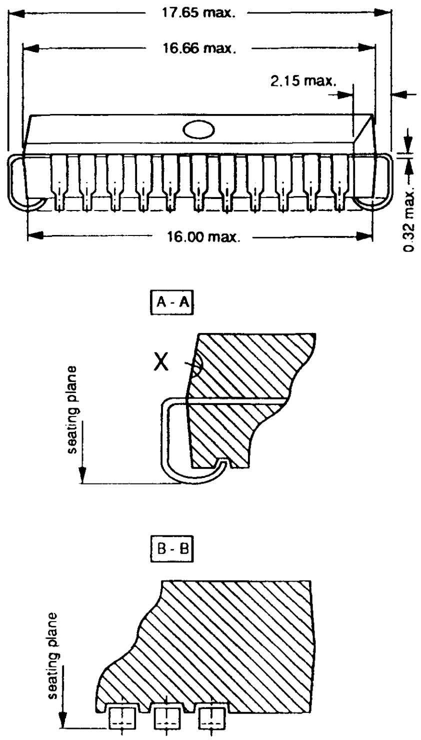


Dimensions in mm.

Package Outline Drawings

SOT187 44-PIN PLASTIC LEADED CHIP CARRIER; POCKET VERSION (A) PACKAGE





Dimensions in mm

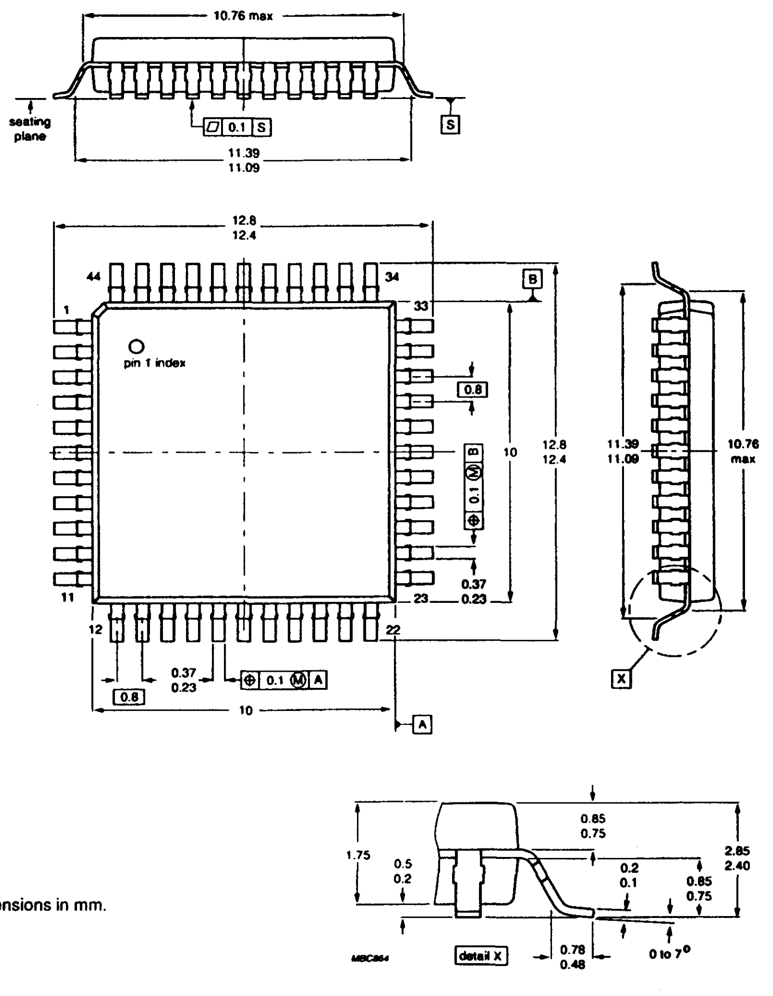
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may may deviate from nominal by ±0.18 mm.

Package Outline Drawings

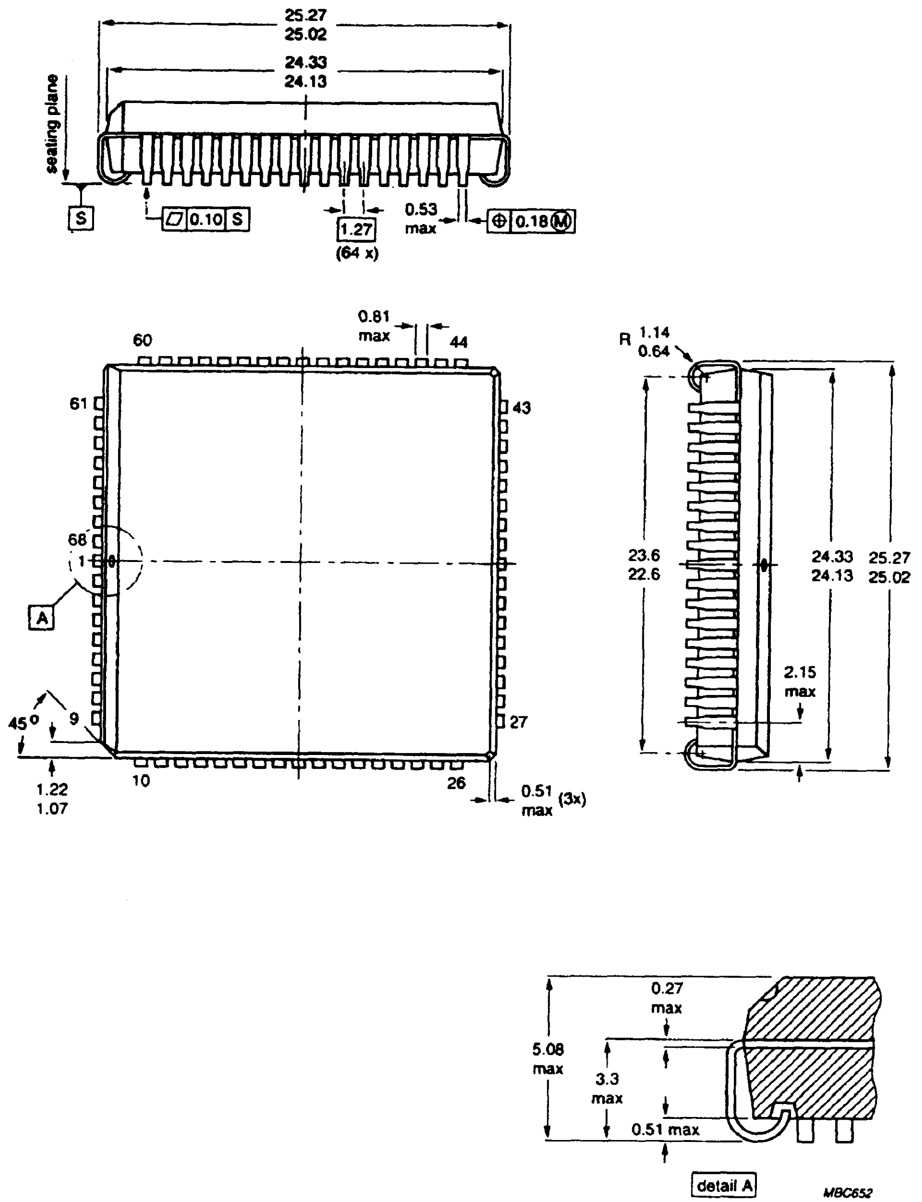
SOT307 44-PIN PLASTIC QUAD FLAT PACK (B) PACKAGE



Dimensions in mm.

Package Outline Drawings

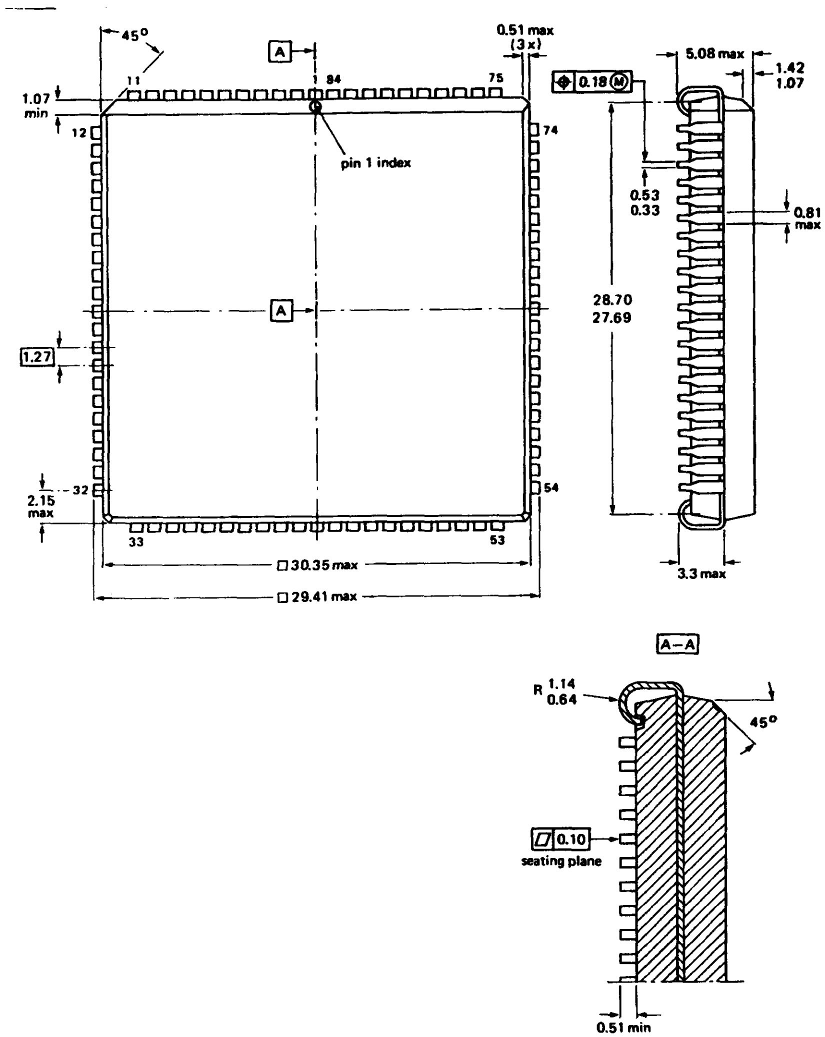
SOT188AA 68-PIN PLASTIC LEADED CHIP CARRIER; POCKET VERSION (A) PACKAGE



Dimensions in mm

Package Outline Drawings

SOT189CG 84-PIN PLASTIC LEADED CHIP CARRIER (A) PACKAGE

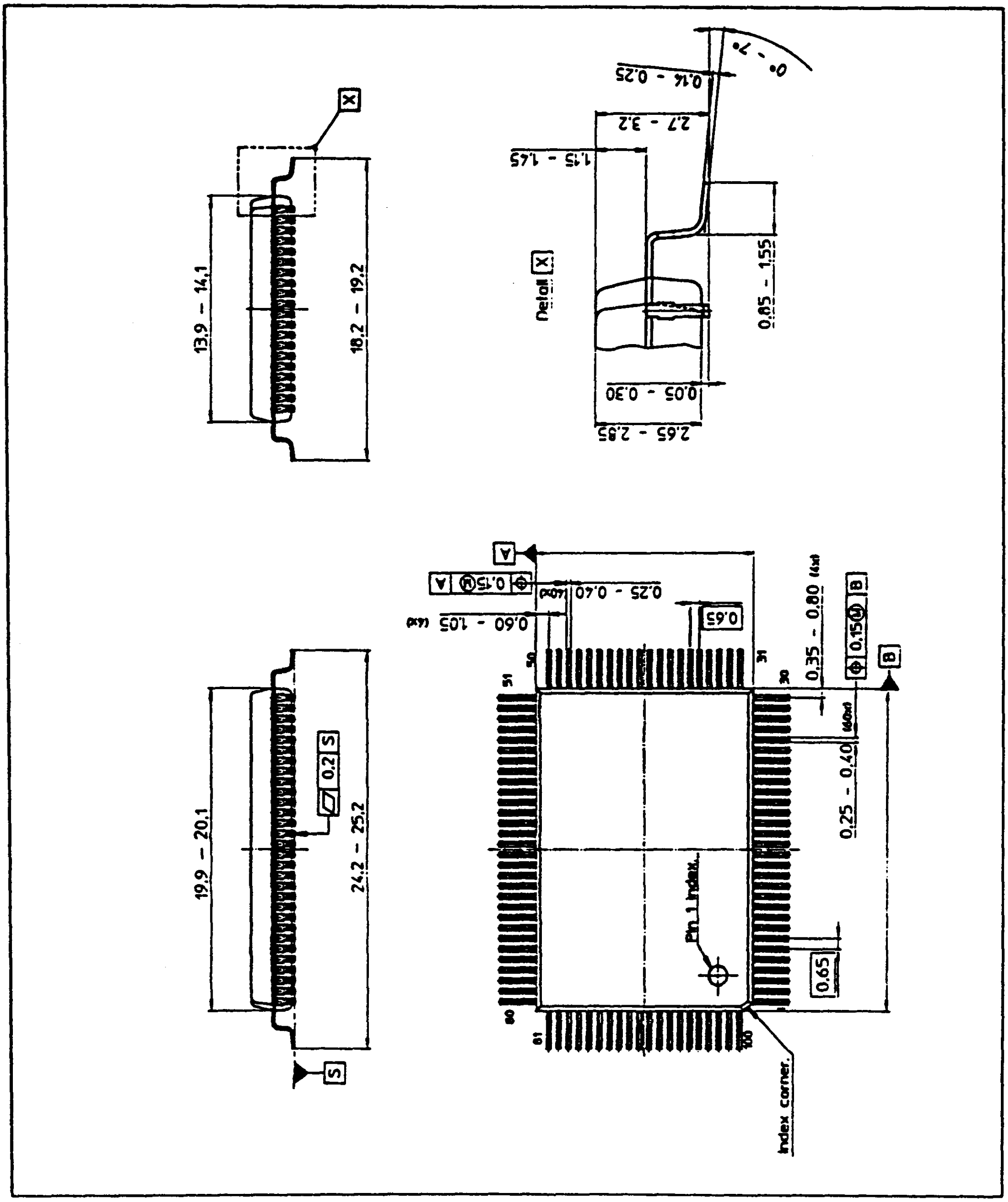


SOT189CG, AGA

7Z25140.1

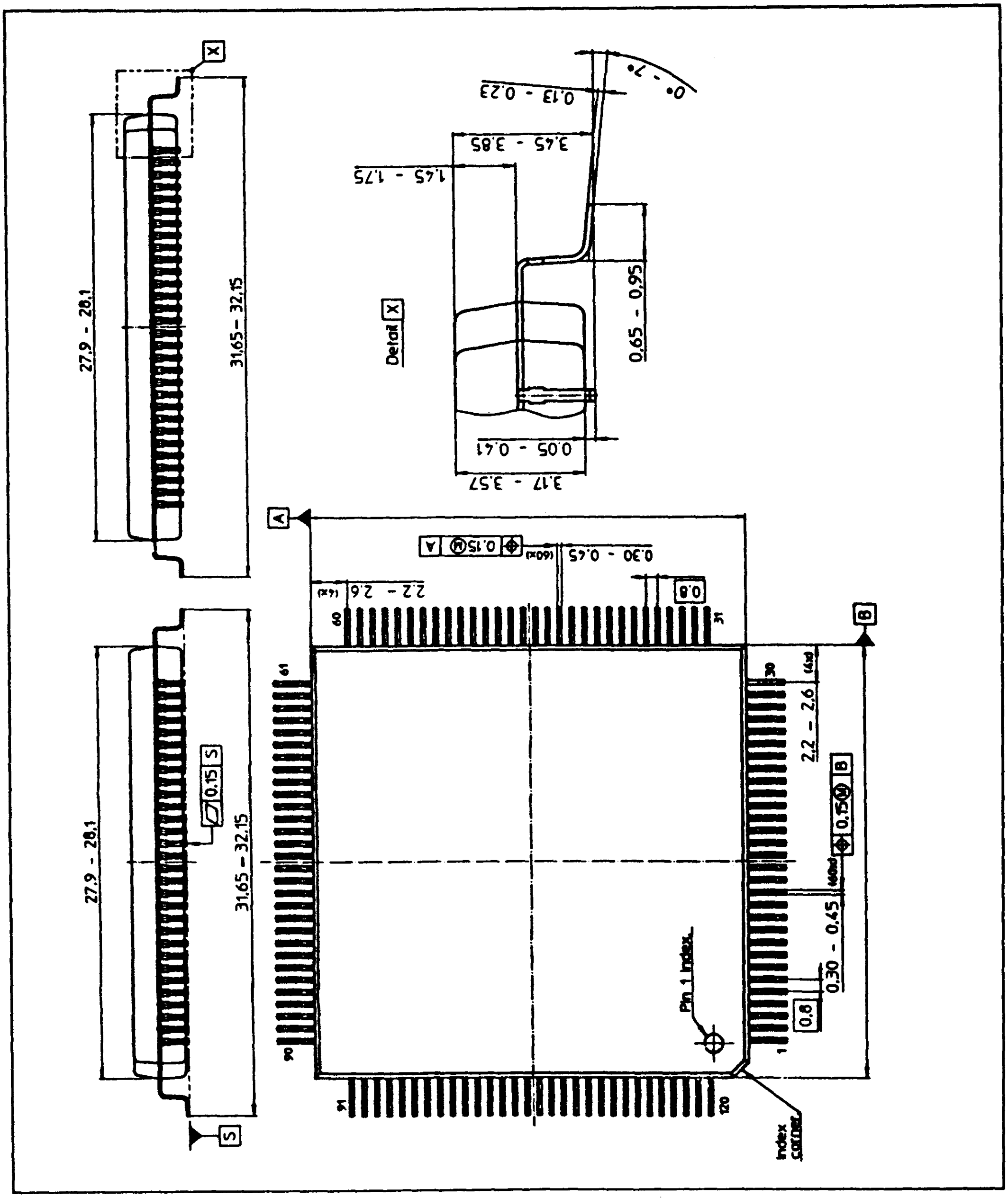
Package Outline Drawings

SOT317 100-PIN PLASTIC QUAD FLAT PACK (B) PACKAGE



Package Outline Drawings

SOT349 120-PIN PLASTIC QUAD FLAT PACK (B) PACKAGE



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4/15/93

Data handbook system

Appendix A

INTRODUCTION

Philips Semiconductors' data handbook system is comprised of 37 books. The handbooks are classified into two series:

INTEGRATED CIRCUITS and
DISCRETE SEMICONDUCTORS.

Data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogs are available for selected product ranges (some catalogs are also on floppy discs).

For more information about data handbooks, catalogs and subscriptions, contact one of the organizations listed on the back cover of this handbook. Product specialists are at your service and inquiries are answered promptly.

INTEGRATED CIRCUITS

IC01	Semiconductors for Radio and Audio Systems
IC02a	Semiconductors for Television and Video Systems
IC02b	Semiconductors for Television and Video Systems
IC03a	Semiconductors for Telecom Systems
IC03b	Semiconductors for Telecom Systems
IC04	CMOS HE4000B Logic Family
IC05	Advanced Low-power Schottky (ALS) Logic Series
IC06	High-speed CMOS Logic Family
IC08	ECL 100K Logic Families
IC10	Memories
IC11	General-purpose/Linear ICs
IC12	Display Drivers and Microcontroller Peripherals
IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-Bit Microcontrollers
IC15	FAST TTL Logic Series

INTEGRATED CIRCUITS (Continued)

IC16	ICs for Clocks and Watches
IC18	Semiconductors for In-car Electronics and General Industrial Applications
IC19	Semiconductors for Datacom: LANs, UARTs, Multi-protocol Controllers and Fiber Optics
IC20	80C51-based 8-Bit Microcontrollers
IC21	68000-based 16-Bit Microcontrollers
IC22	ICs for Multi-media Systems
IC23	QUBIC Advanced BiCMOS Bus Interface Logic ABT MULTIBYTE™
IC24	Low Voltage CMOS Logic

DISCRETE SEMICONDUCTORS

SC01	Diodes
SC02	Power Diodes
SC03	Thyristors and Triacs
SC04	Small Signal Transistors
SC05	Low-frequency Power Transistors and Hybrid IC Power Modules
SC06	High-voltage and Switching NPN Power Transistors
SC07	Small-signal Field-effect Transistors
SC08a	RF Power Bipolar Transistors
SC08b	RF Power MOS Transistors
SC09	RF Power Modules
SC10a	Surface Mounted Semiconductors
SC10b	Surface Mounted Semiconductors
SC12	Optocouplers
SC13	Power MOS Transistors
SC14	RF Wideband Transistors
SC15	Microwave Transistors
SC16	Wideband Hybrid IC Modules
SC17	Semiconductor Sensors

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